Pin Description

Pin #	Pin Name	Type	Pin Description
1, 4	VIN	Power/Input	With an internal 1.4 V $V_{IN(UVLO)}$ threshold, VIN supplies the power for the operation of the power switch, the internal control circuitry, and the source terminal of pFET. Bypass the VIN pin to GND with a 2.2 μF (or larger), low-ESR capacitor.
2, 3	ON	Input	A low-to-high transition on this pin initiates the operation of the power switch. ON is an asserted-HIGH, level-sensitive CMOS input with ON_V_{IL} < 0.3 V and ON_V_{IH} > 1 V. As the ON input circuitry does not have an internal pull-down resistor, connect the ON pin directly to a GPIO controller – do not allow this pin to be open circuited.
5, 8	VOUT	Output	Output and drain terminal of MOSFET.
6	$\overline{FAULT}$	Output	An open drain output, $\overline{FAULT}$ is asserted within $T\overline{FAULT}_{LOW}$ when a ($V_{OUT} + V_{REVERSE} > V_{IN}$) condition is detected. The $\overline{FAULT}$ output is deasserted within $T\overline{FAULT}_{HIGH}$ when the fault condition is removed. Connect an external 10 kΩ resistor from the $\overline{FAULT}$ pin to the system's local logic supply.
7	GND	GND	Ground connection. Connect this pin to system analog or power ground plane.

Ordering Information

Part Number	Type	Production Flow
SLG59M1649V	STDFN 8L	Industrial, -40 °C to 85 °C
SLG59M1649VTR	STDFN 8L (Tape and Reel)	Industrial, -40 °C to 85 °C

Absolute Maximum Ratings

Parameter	Description	Conditions	Min.	Typ.	Max.	Unit
V_{IN}	Power Switch Input Voltage		-0.3	--	6	V
T_S	Storage Temperature		-65	--	150	°C
ESD_{HBM}	ESD Protection	Human Body Model	2000	--	--	V
ESD_{CDM}	ESD Protection	Charged Device Model	1000	--	--	V
MSL	Moisture Sensitivity Level			1		
θ_{JA}	Thermal Resistance	1.0 x 1.6 mm 8L STDFN	--	82	--	°C/W
$T_{J,MAX}$	Maximum Junction Temperature		--	150	--	°C
MOSFET IDS_{CONT}	Continuous Current from VIN to VOUT	Each channel, T_J< 150°C	--	--	4	A
MOSFET IDS_{PK}	Peak Current from VIN to VOUT	Maximum pulsed switch current, pulse width < 1 ms, 1% duty cycle	--	--	4.5	A

Note: Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

Electrical Characteristics

1.5 V ≤ V_{IN} ≤ 5.5 V; C_{IN} = 2.2 µF; T_A = -40 °C to 85 °C unless otherwise noted. Typical values are at T_A = 25 °C.

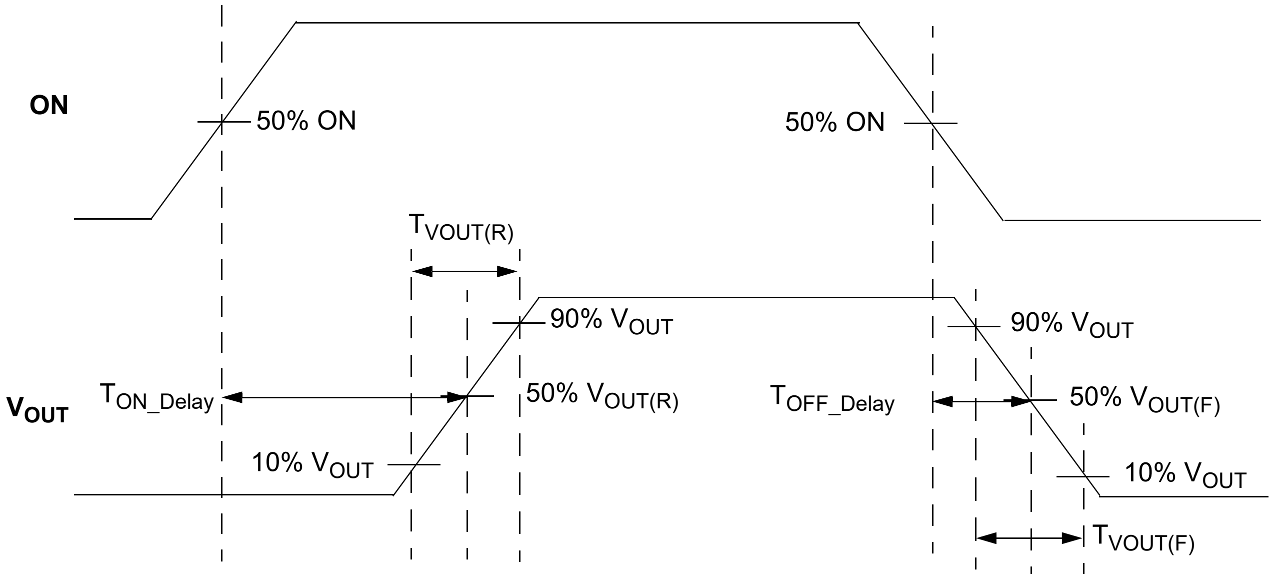
Parameter	Description	Conditions	Min.	Typ.	Max.	Unit
V_{IN}	Power Switch Input Voltage		1.5	--	5.5	V
$V_{IN(UVLO)}$	V_{IN} Undervoltage Lockout Threshold	V_{IN} ↑, V_{ON} = 0 V, R_{LOAD} = 10 Ω	--	--	1.4	V
		V_{IN} ↓, V_{ON} = 0 V, R_{LOAD} = 10 Ω	0.5	--	--	V
I_{IN}	Quiescent Power Switch Current	V_{IN} = 5.25 V, ON = HIGH, I_{DS} = 0 mA	--	6.6	11	µA
		V_{IN} = 1.5 V, ON = HIGH, I_{DS} = 0 mA	--	5	8	µA
$I_{IN(OFF)}$	OFF Mode Power Switch Current	V_{IN} = 5.25 V, ON = LOW, R_{LOAD} = 1 MΩ	--	2	3	µA
		V_{IN} = 1.5 V, ON = LOW, R_{LOAD} = 1 MΩ	--	0.8	2	µA
RDS_{ON}	ON Resistance	T_A = 25 °C, V_{IN} = 5.0 V, I_{DS} = -200 mA	--	23	28	mΩ
		T_A = 25 °C, V_{IN} = 2.5 V, I_{DS} = -200 mA	--	31	38	mΩ
		T_A = 25 °C, V_{IN} = 1.5 V, I_{DS} = -200 mA	--	42	50	mΩ
		T_A = 85 °C, V_{IN} = 5.0 V, I_{DS} = -200 mA	--	27	32	mΩ
		T_A = 85 °C, V_{IN} = 2.5 V, I_{DS} = -200 mA	--	37	44	mΩ
		T_A = 85 °C, V_{IN} = 1.5 V, I_{DS} = -200 mA	--	48	58	mΩ
MOSFET IDS	Current from VIN to VOUT	Continuous	--	--	4	A
$V_{REVERSE}$	Reverse-current Voltage Threshold		--	50	--	mV
$I_{REVERSE}$	Reverse-current Leakage Current after Reverse Current Event	$V_{OUT} - V_{IN} > V_{REVERSE}$; T_A = 25°C; ON = GND	--	1	--	µA
V_{ON}	ON Pin Voltage Range		0		V_{IN}	V
$I_{ON(Leakage)}$	ON Pin Leakage Current	1.4 V ≤ V_{ON} ≤ V_{IN} or V_{ON} = GND	--	--	1	µA
ON_V_{IH}	ON Pin Input High Voltage		1	--	V_{IN}	V

Electrical Characteristics (continued)

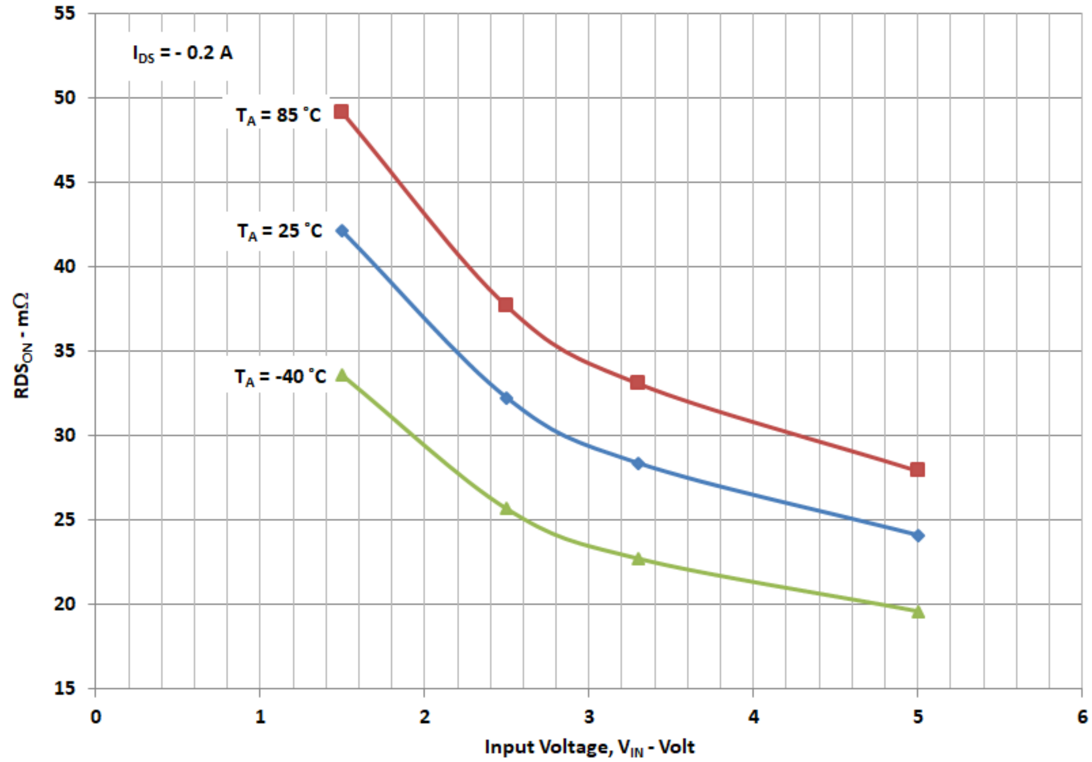
1.5 V ≤ V_{IN} ≤ 5.5 V; C_{IN} = 2.2 µF; T_A = -40 °C to 85 °C unless otherwise noted. Typical values are at T_A = 25 °C.

Parameter	Description	Conditions	Min.	Typ.	Max.	Unit
ON_V_{IL}	ON Pin Input Low Voltage		-0.3	0	0.3	V
ON_{HYS}	ON Hysteresis		--	60	--	mV
$R_{DISCHRG}$	Output Discharge Resistance	V_{IN} = 5 V; V_{OUT} < 0.4 V	50	80	120	Ω
T_{REV}	Reverse-current Detect Response Delay	V_{IN} = 5 V	--	10	--	µs
T_{REARM}	Reverse Detect Rearm Time		--	1.5	--	ms
T_{ON_Delay}	ON Delay Time	50% ON to 50% V_{OUT} ↑; T_A = 25°C, V_{IN} = 5 V; R_{LOAD} = 10 Ω, C_{LOAD} = 0.1 µF	--	180	235	µs
		50% ON to 50% V_{OUT} ↑; T_A = 25°C, V_{IN} = 1.5 V; R_{LOAD} = 10 Ω, C_{LOAD} = 0.1 µF	--	110	145	µs
$T_{VOUT(R)}$	V_{OUT} Rise Time	10% to 90% V_{OUT} ↑; T_A = 25°C, V_{IN} = 5 V; R_{LOAD} = 10 Ω, C_{LOAD} = 0.1 µF	--	130	170	µs
		10% to 90% V_{OUT} ↑; T_A = 25°C, V_{IN} = 1.5 V; R_{LOAD} = 10 Ω, C_{LOAD} = 0.1 µF	--	66	86	µs
$T_{VOUT(F)}$	V_{OUT} Fall Time	90% to 10% V_{OUT} ↓; T_A = 25°C, V_{IN} = 5 V; R_{LOAD} = 10 Ω, C_{LOAD} = 0.1 µF	--	2.2	3.6	µs
		90% to 10% V_{OUT} ↓; T_A = 25°C, V_{IN} = 1.5 V; R_{LOAD} = 10 Ω, C_{LOAD} = 0.1 µF	--	2.2	3.6	µs
T_{OFF_Delay}	OFF Delay Time	50% ON to 50% V_{OUT} ↓; T_A = 25°C, V_{IN} = 5 V; R_{LOAD} = 10 Ω, C_{LOAD} = 0.1 µF	--	3.5	5	µs
		50% ON to 50% V_{OUT} ↓; T_A = 25°C, V_{IN} = 1.5 V; R_{LOAD} = 10 Ω, C_{LOAD} = 0.1 µF	--	5	7	µs
$T\overline{FAULT}_{LOW}$	$\overline{FAULT}$ Assertion Time	Reverse-voltage Detection to $\overline{FAULT}$↓; 1.5 V ≤ V_{IN} ≤ 5 V; ON = Low	--	2	--	µs
		1.5 V ≤ V_{IN} ≤ 5 V; ON = High	--	0.5	--	µs
$T\overline{FAULT}_{HIGH}$	$\overline{FAULT}$ De-assertion Time	Delay to $\overline{FAULT}$↑ after fault condition is removed; 1.5 V ≤ V_{IN} ≤ 5 V; ON = Low	--	7	--	ms
		1.5 V ≤ V_{IN} ≤ 5 V; ON = High	--	2	--	ms
$\overline{FAULT}_{VOL}$	$\overline{FAULT}$ Output Low Voltage	$I_{\overline{FAULT}}$ = 1 mA	--	--	0.2	V

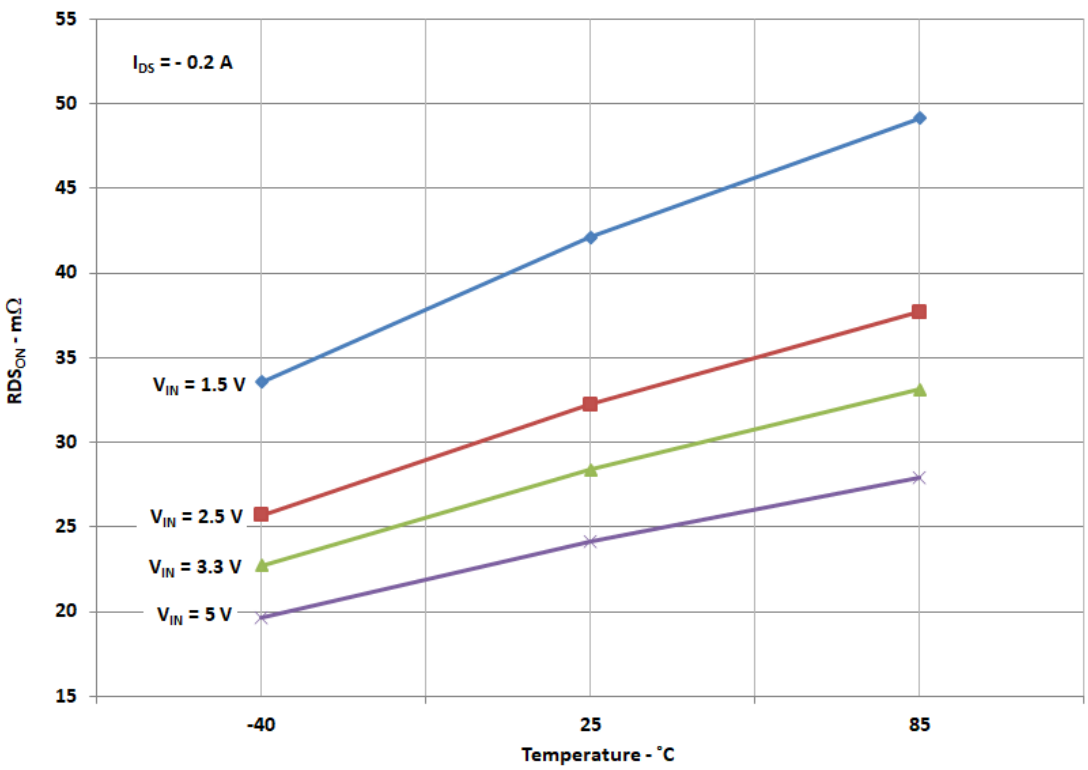
T_{ON_Delay}, $V_{OUT(SR)}$, and T_{Total_ON} Timing Details



RDS_{ON} vs. V_{IN} and Temperature



RDS_{ON} vs.Temperature and V_{IN}



V_{IN} Inrush Current Details

When the SLG59M1649V is enabled with ON ↑, the power switch closes to charge the VOUT output capacitor to V_{IN}. The charging current drawn from V_{IN} is commonly referred to as "V_{IN} inrush current" and can cause the input power source to collapse if the V_{IN} inrush current is too high.

Since the V_{OUT} rise time of the SLG59M1649V is fixed, V_{IN} inrush current is then a function of the output capacitance at VOUT. The expression relating V_{IN} inrush current, the SLG59M1649V V_{OUT} rise time, and C_{LOAD} is:

$$V_{IN}\text{ Inrush Current} = C_{LOAD} \times \frac{\Delta V_{OUT}(10\%\text{ to }90\%)}{T_{VOUT(R)}\,(10\%\text{ to }90\%)}$$

where in this expression ΔV_{OUT} is equivalent to V_{IN} if the initial SLG59M1649V's output voltages are zero.

In the table below are examples of V_{IN} inrush currents assuming zero initial charge on C_{LOAD} as a function of V_{IN}.

V_{IN} (V)	V_{OUT} Rise Time (µs)	C_{LOAD} (µF)	Inrush Current (mA)
1.5	66	0.1	1.8
5	130	0.1	3.1

Since the relationship is linear and if C_{LOAD} were increased to 1 µF, then the V_{IN} inrush currents would be 10x higher in either example. If a large C_{LOAD} capacitor is required in the application and depending upon the strength of the input power source, it may very well be necessary to increase the C_{IN}-to-C_{LOAD} ratio to minimize V_{IN} droop during turn-on.

For other V_{OUT} rise time options, please contact Dialog for additional information.

Power Dissipation

The junction temperature of the SLG59M1649V depends on factors such as board layout, ambient temperature, external air flow over the package, load current, and the RDS_{ON}-generated voltage drop across each power MOSFET. While the primary contributor to the increase in the junction temperature of the SLG59M1649V is the power dissipation of its power MOSFETs, its power dissipation and the junction temperature in nominal operating mode can be calculated using the following equations:

$$PD_{TOTAL} = RDS_{ON} \times I_{DS}^2$$

where:

PD_{TOTAL} = Total package power dissipation, in Watts (W)

RDS_{ON} = Power MOSFET ON resistance, in Ohms (Ω)

I_{DS} = Output current, in Amps (A)

and

$$T_J = PD_{TOTAL} \times \theta_{JA} + T_A$$

where:

T_J = Die junction temperature, in Celsius degrees (°C)

θ_{JA} = Package thermal resistance, in Celsius degrees per Watt (°C/W) – highly dependent on pcb layout

T_A = Ambient temperature, in Celsius degrees (°C)

Power Dissipation (continued)

In nominal operating mode, the SLG59M1649V's power dissipation can also be calculated by taking into account the voltage drop across each switch (V_{IN}-V_{OUT}) and the magnitude of that channel's output current (I_{DS}):

$$PD_{TOTAL} = (V_{IN} - V_{OUT}) \times I_{DS} \text{ or}$$

$$PD_{TOTAL} = (V_{IN} - (R_{LOAD} \times I_{DS})) \times I_{DS}$$

where:

PD_{TOTAL} = Total package power dissipation, in Watts (W)

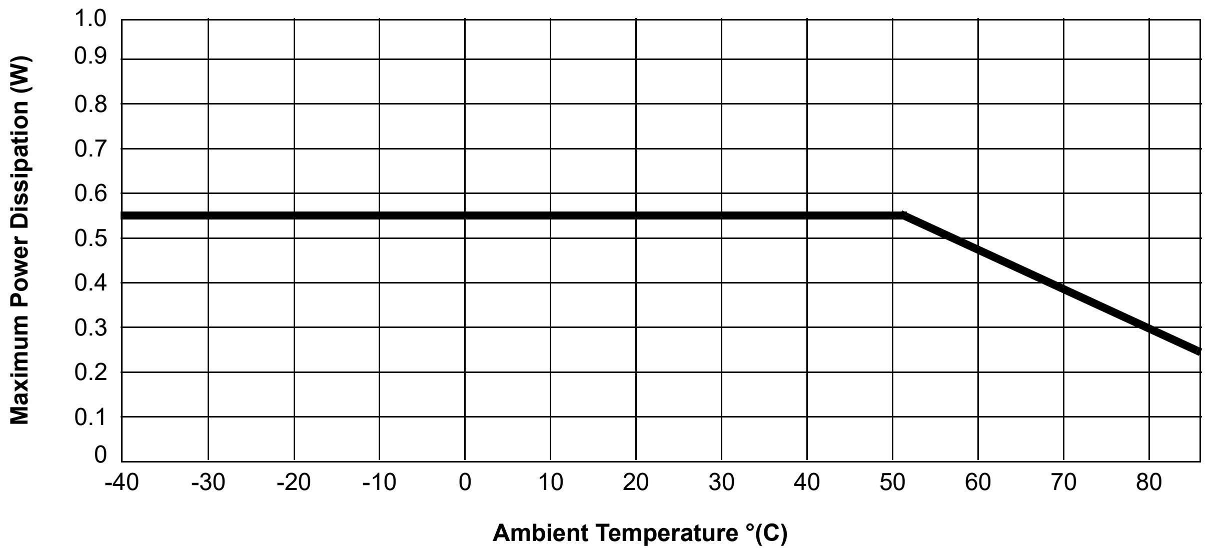
V_{IN} = Input Voltage, in Volts (V)

R_{LOAD} = Output Load Resistance, in Ohms (Ω)

I_{DS} = Output current, in Amps (A)

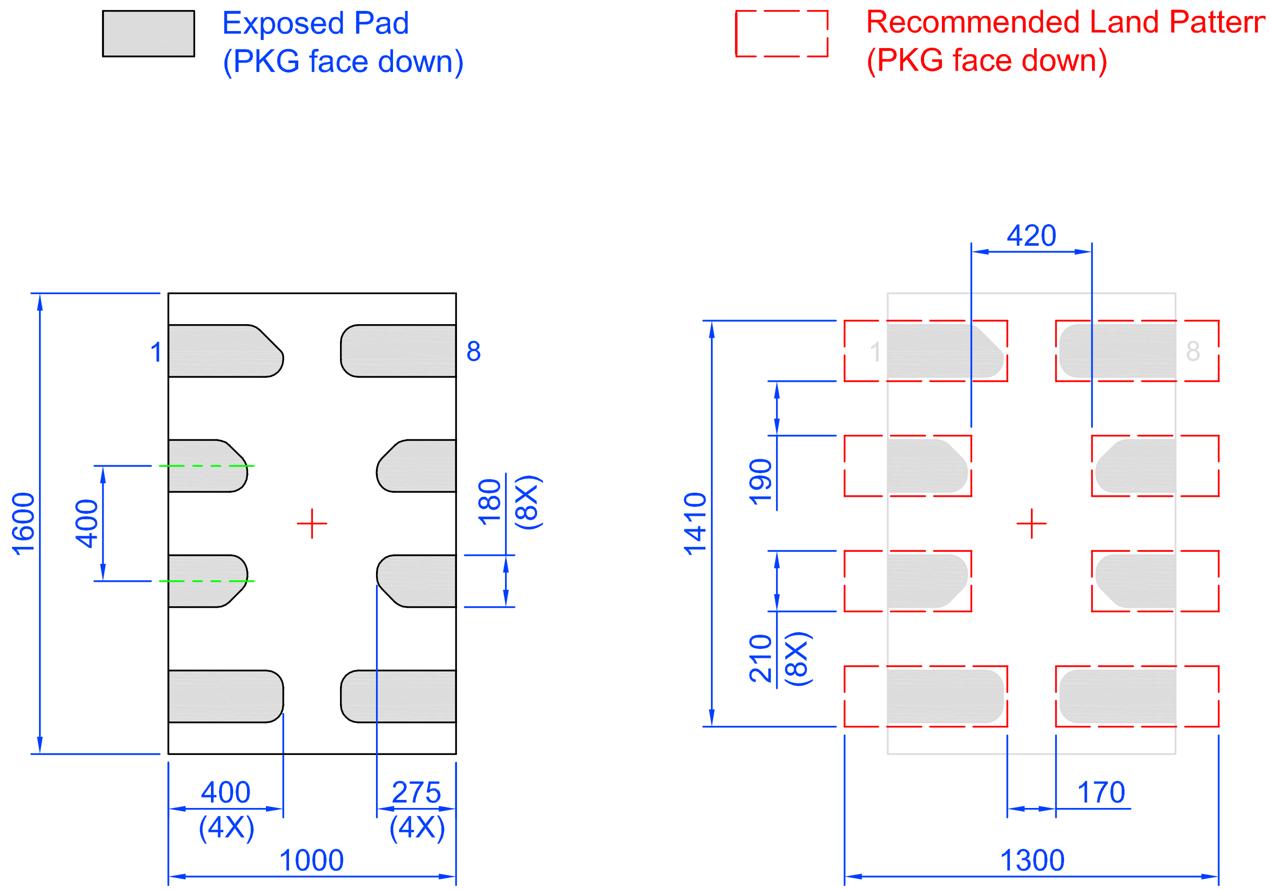
V_{OUT} = Output voltage, or $R_{LOAD} \times I_{DS}$

Power Dissipation Derating Curve



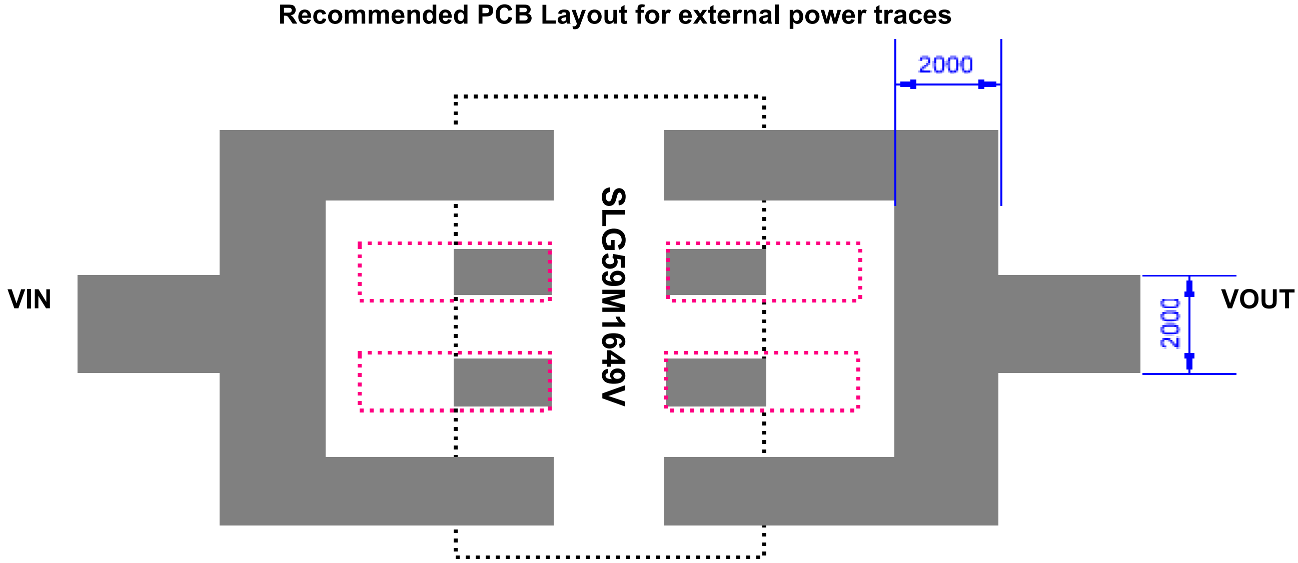
Note: Each V_{IN}, V_{OUT} = 1 in^2 1.2 oz. copper on FR4

SLG59M1649V Layout Suggestion



Note: All dimensions shown in micrometers (µm)

Recommended PCB Layout for external power traces



Note: All dimensions shown in µm (micrometers)

Layout Guidelines:

1. Since the VIN and VOUT pins dissipate most of the heat generated during high-load current operation, it is highly recommended to make power traces as short, direct, and wide as possible. A good practice is to make power traces with absolute minimum widths of 15 mils (0.381 mm) per Ampere. A representative layout, shown in Figure 1, illustrates proper techniques for heat to transfer as efficiently as possible out of the device;

2. To minimize the effects of parasitic trace inductance on normal operation, it is recommended to connect input C_{IN} and output C_{LOAD} low-ESR capacitors as close as possible to the SLG59M1649V's VIN and VOUT pins;

3. The GND pin should be connected to system analog or power ground plane.

4. 2 oz. copper is recommended for high current operation.

SLG59M1649V Evaluation Board:

A GFET3 Evaluation Board for SLG59M1649V is designed according to the statements above and is illustrated on Figure 1. Please note that evaluation board has D_Sense and S_Sense pads. They cannot carry high currents and dedicated only for RDS_{ON} evaluation.

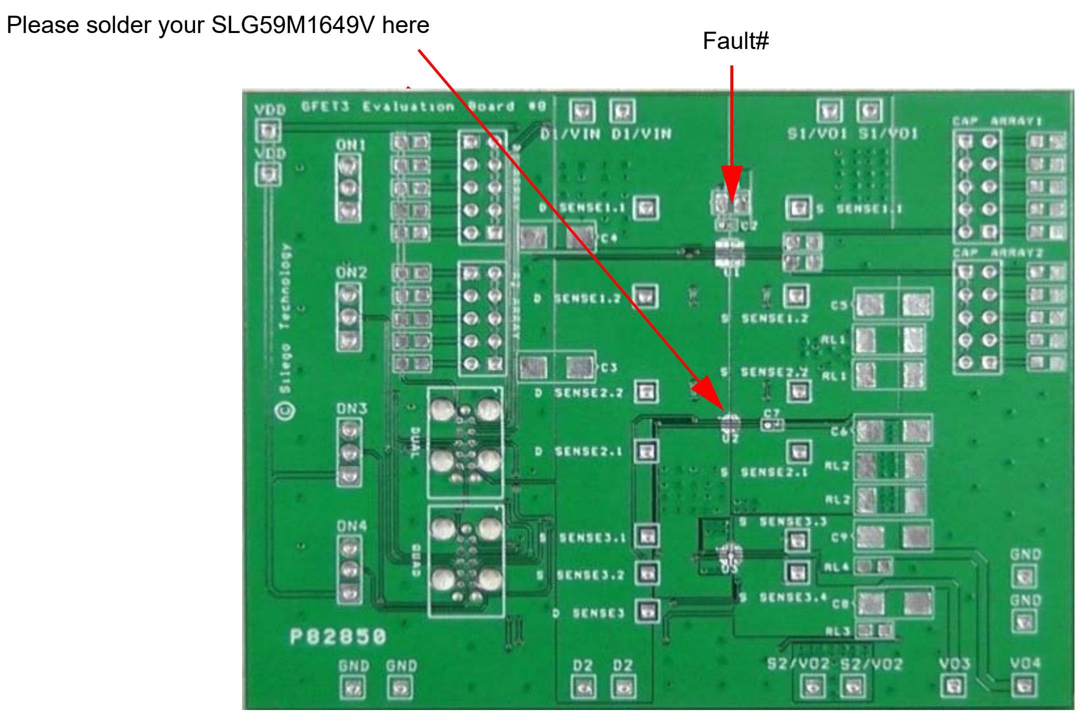


Figure 1. SLG59M1649V Evaluation Board.

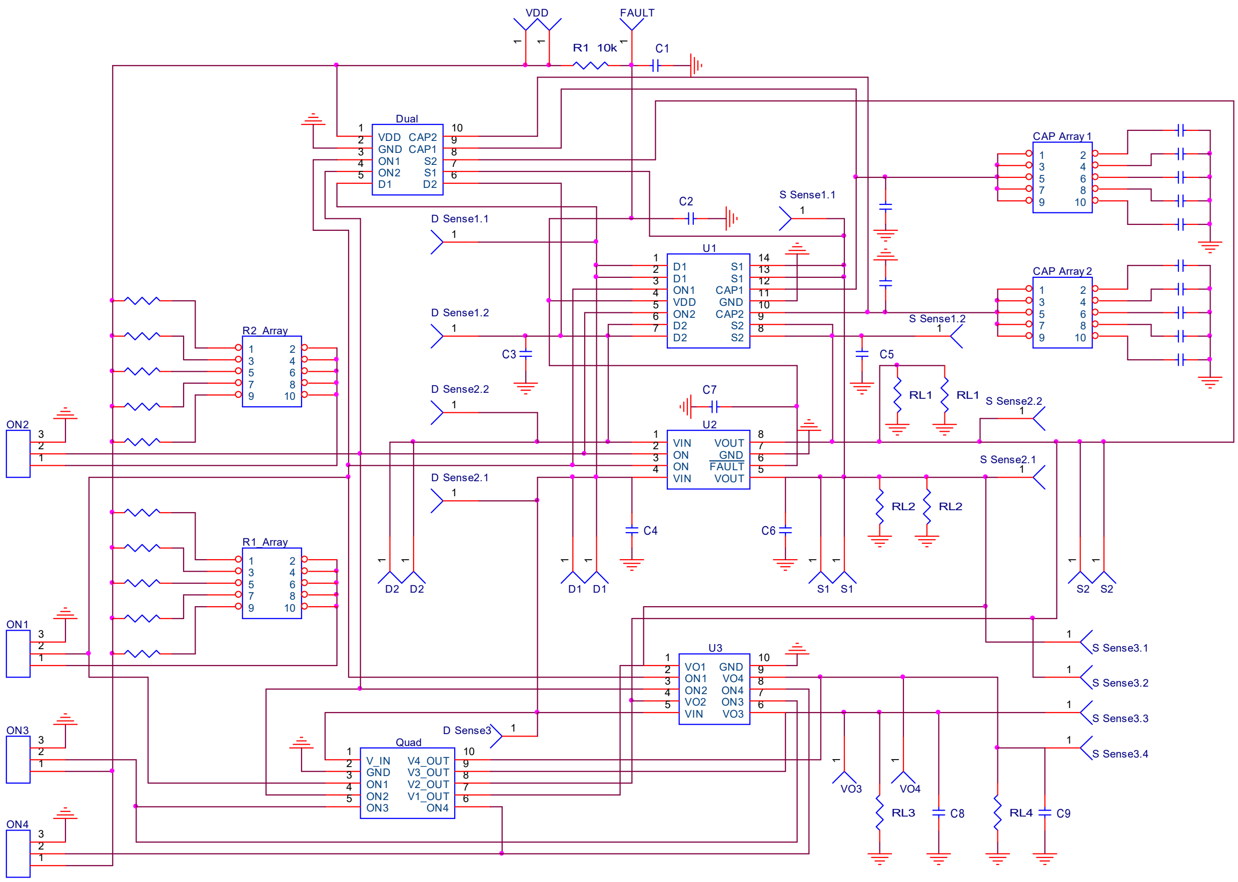


Figure 2. SLG59M1649V Evaluation Board Connection Circuit.

Basic Test Setup and Connections

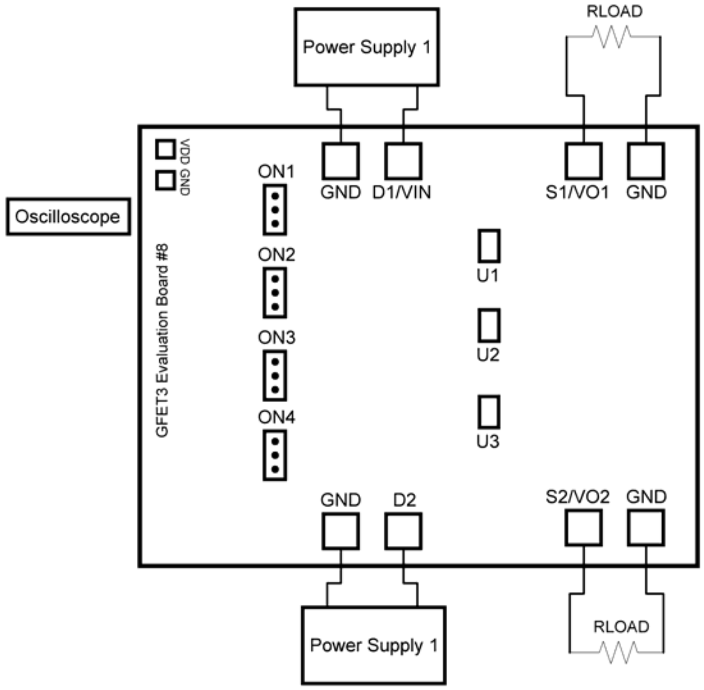


Figure 3. Typical connections for GFET3 Evaluation.

EVB Configuration

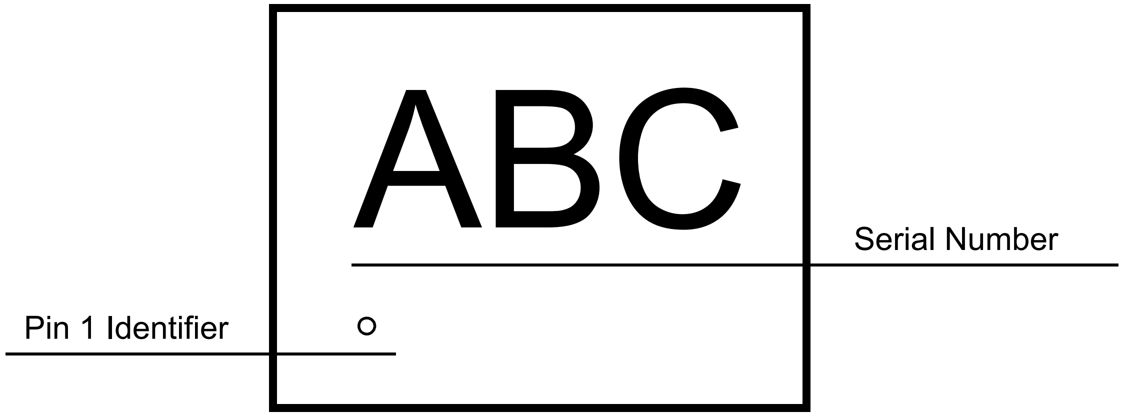
1. Connect oscilloscope probes to D1/VIN, D2, S1/VO1, S2/VO2, ON etc.;

2. Use VDD connector to have logic high level for FAULT and ON signals;

3. Turn on Power Supply 1 and set desired V_{IN} from 1.5 V…5.5 V range;

4. Toggle the ON signal High or Low to observe SLG59M1649V operation.

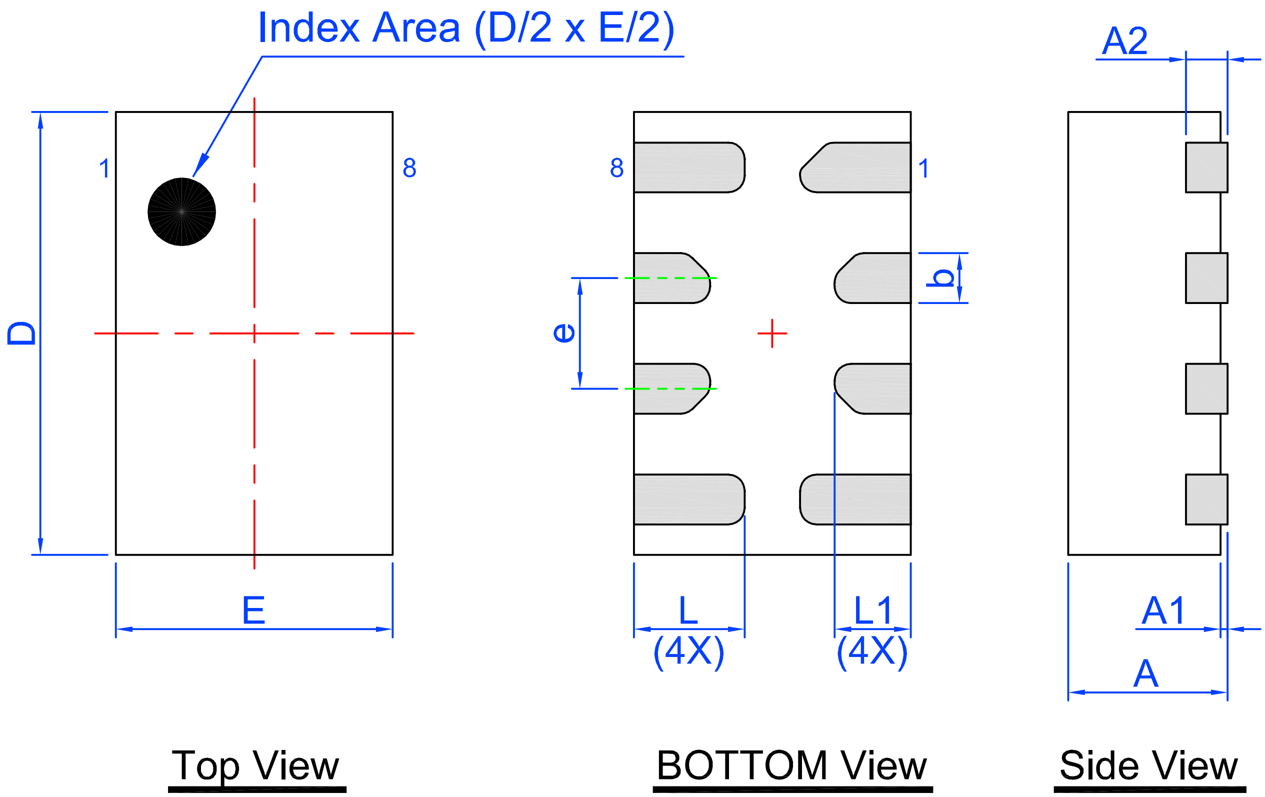
Package Top Marking System Definition



ABC - 3 alphanumeric Part Serial Number
where A, B, or C can be A-Z and 0-9

Package Drawing and Dimensions

8 Lead STDFN Package 1.0 x 1.6 mm



Unit: mm

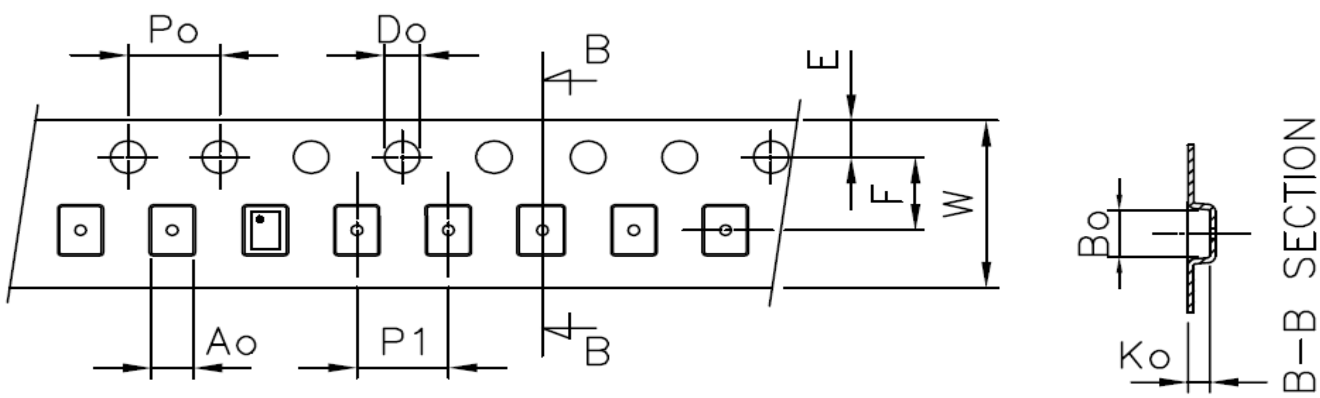
Symbol	Min	Nom.	Max	Symbol	Min	Nom.	Max
A	0.50	0.55	0.60	D	1.55	1.60	1.65
A1	0.005	-	0.050	E	0.95	1.00	1.05
A2	0.10	0.15	0.20	L	0.35	0.40	0.45
b	0.13	0.18	0.23	L1	0.225	0.275	0.325
e	0.40 BSC						

Tape and Reel Specifications

Package Type	# of Pins	Nominal Package Size [mm]	Max Units		Reel & Hub Size [mm]	Leader (min)		Trailer (min)		Tape Width [mm]	Part Pitch [mm]
			per Reel	per Box		Pockets	Length [mm]	Pockets	Length [mm]		
STDFN 8L 1x1.6mm 0.4P FCD Green	8	1.0 x 1.6 x 0.55	3,000	3,000	178 / 60	100	400	100	400	8	4

Carrier Tape Drawing and Dimensions

Package Type	Pocket BTM Length	Pocket BTM Width	Pocket Depth	Index Hole Pitch	Pocket Pitch	Index Hole Diameter	Index Hole to Tape Edge	Index Hole to Pocket Center	Tape Width
	A0	B0	K0	P0	P1	D0	E	F	W
STDFN 8L 1x1.6mm 0.4P FCD Green	1.12	1.72	0.7	4	4	1.55	1.75	3.5	8



Recommended Reflow Soldering Profile

Please see IPC/JEDEC J-STD-020: latest revision for reflow profile based on package volume of 0.88 mm^3 (nominal). More information can be found at www.jedec.org.

Revision History

Date	Version	Change
12/12/2018	1.01	Updated UVLO spec Updated Style and Formatting Updated Charts Added Layout Guidelines Fixed typos
2/23/2017	1.00	Production Release

