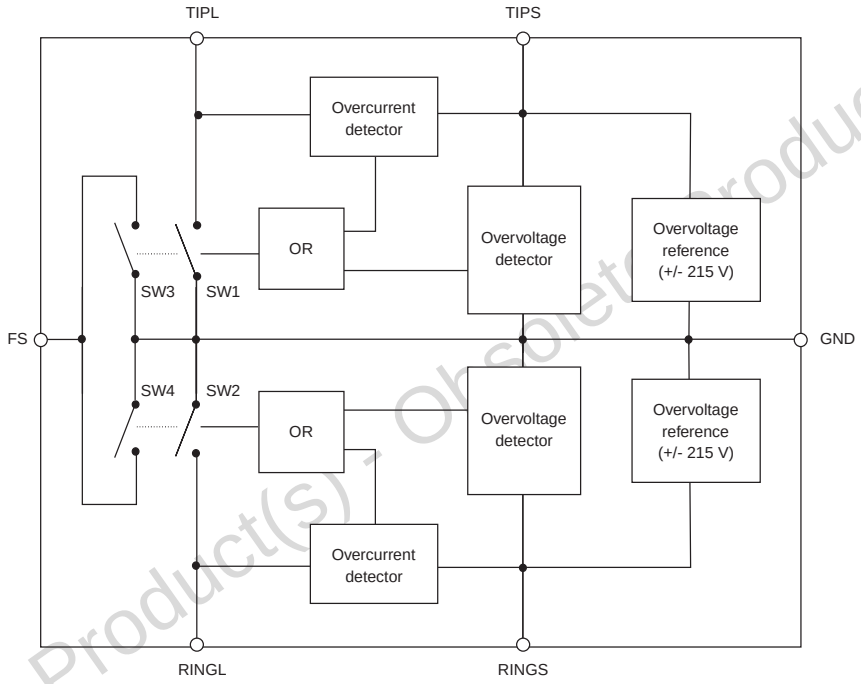
COMPLIES WITH THE FOLLOWING STANDARDS:	Peak Surge Voltage (V)	Voltage Waveform (µs)	Current Waveform (µs)	Admissible Ipp (A)	Necessary Resistor (Ω)
CCITT K20	6000	10/700	5/310	150	-
VDE0433	6000	10/700	5/310	150	-
VDE0878	4000	1.2/50	1/20	100	-
IEC61000-4-5	6000 4000	10/700 1.2/50	5/310 8/20	150 100	- -
FCC Part 68	1500 800	10/160 10/560	10/160 10/560	200 100	- -
BELLCORE TR-NWT-001089	2500 1000	2/10 10/1000	2/10 10/1000	500 100	- -

BLOCK DIAGRAM



Pin	Symbol	Description
1	FS	Failure Status
2	TIPS	TIP (SLIC side)
3 / 4 / 5	TIPL	TIP (Line side)
6 / 7 / 8	RINGL	RING (Line side)
9	RINGS	RING (SLIC side)
10	NC	Not connected
TAB	GND	Ground

APPLICATION NOTE

1. INTRODUCTION

The aim of this section is to show the behavior of our new telecom line protection device. This device includes a primary protection level and is suitable for main distribution frames and line cardsThis protection concept is explained and, in addition, the CLP200M performances are analysed when facing different surges as described in the CCITT recommendations.

Fig. 1 : Subscriber line protection topology

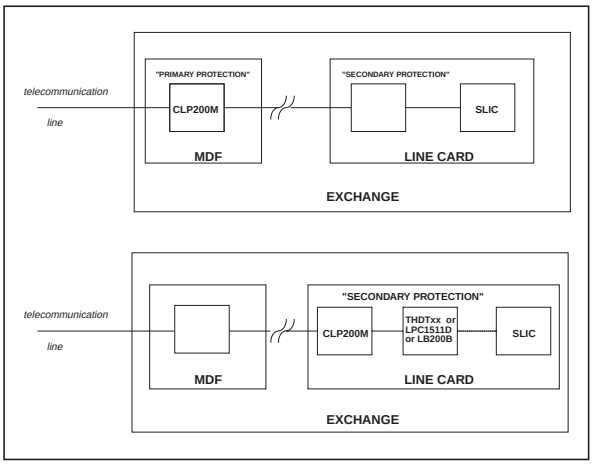


Figure 1 is a simplified block diagram of a subscriber line protection that is mainly used so far.

This shows two different things :

- A “primary protection” located on the Main Distribution Frame (MDF) eliminates coarsely the high energy environmental disturbances (lightning transients and AC power mains disturbances)
- A “secondary protection” located on the line card includes a primary protection level (first stage) and a residual protection (second stage) which eliminates finely the remaining transients that have not been totally suppressed by the first stage.

The CLP200M can be used both in MDFs and in line cards. In that case, any line card may be swapped from one MDF to another one without reducing the efficiency of the whole system protection.

The CCITT requirements are different for these two protection locations (MDFs and line cards). Concerning the “primary protection”, the CCITT requires a 4kV, 10/700µs surge test whereas the “secondary protection” has to withstand a 1kV, 10/700µs surge test.

The explanations which follow are basically covering the line card application.

2. STMicroelectronics CLP200M CONCEPT

2.1 Evolution of the SLIC protection

Over the years, the silicon protection performances have considerably changed.

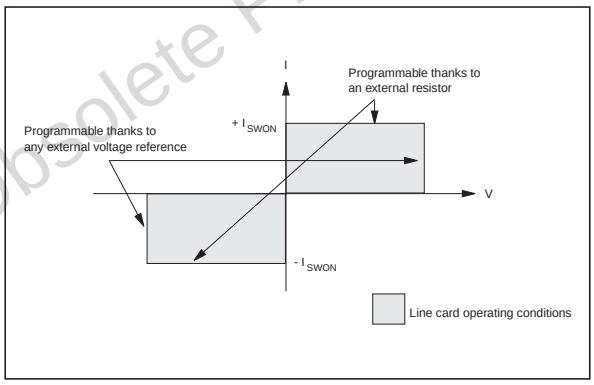
The first generation of products like SMTHBTxx and SMTHDTxx offered fixed overvoltage protection against surges on either TIP or RING line in four packages.

The following generation like THBTxx and THDTxx still offered fixed overvoltage protection against surges on both TIP and RING lines in two packages.

The next step was the introduction of the LCP1511D which brought the advantage of full programmable voltage.

Today, the CLP200M combines the features of all the previous generations. In addition to that, it offers an overcurrent detection when operating in speech mode and also a Failure Status output signal.

Fig. 2 : Line card protection



The figure 2 summarizes the performance of the CLP200M which basically holds the SLIC inside its correct voltage and current values.

APPLICATION CIRCUIT : CLP200M in line card

Fig. 3 : CLP200M in line card

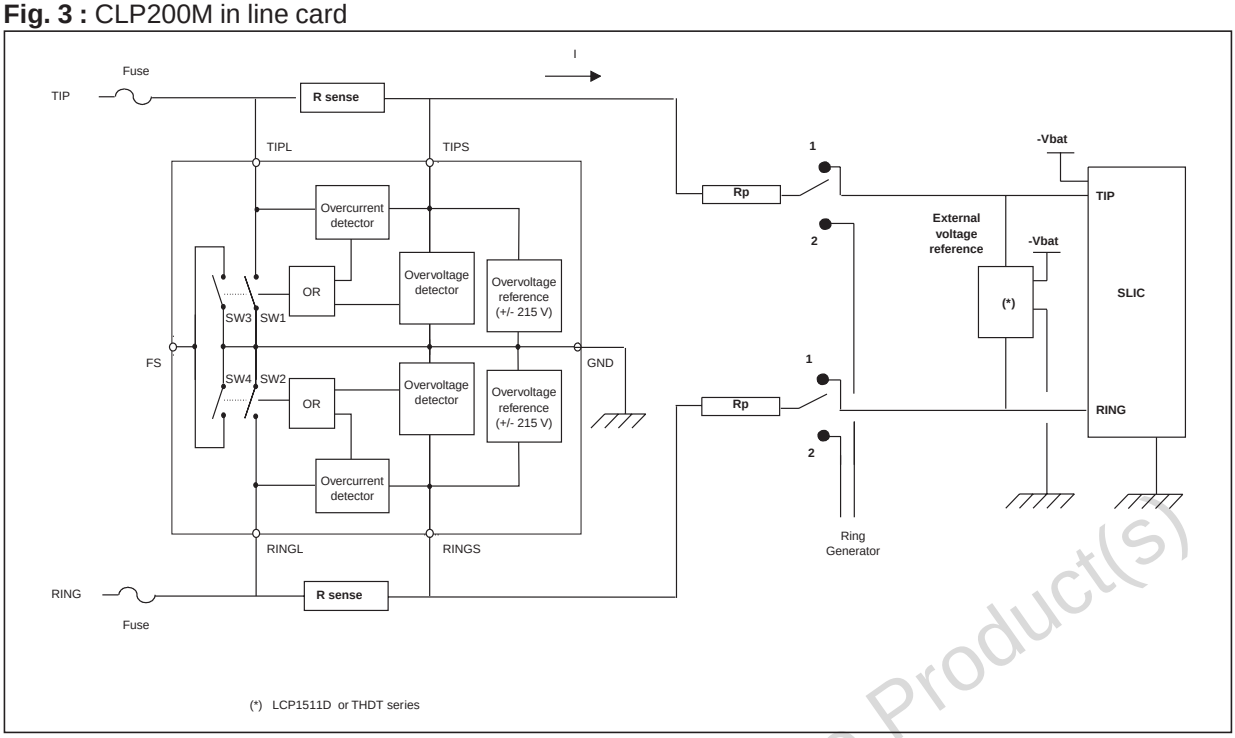


Figure 3 above shows the topology of a protected analog subscriber line at the exchange side. The CLP200M is connected to the ring relay via two balanced Rp resistors, and to the Subscriber Line Interface Circuit. A second device is located near the SLIC : it can be either a LCP1511D or a THDT series.

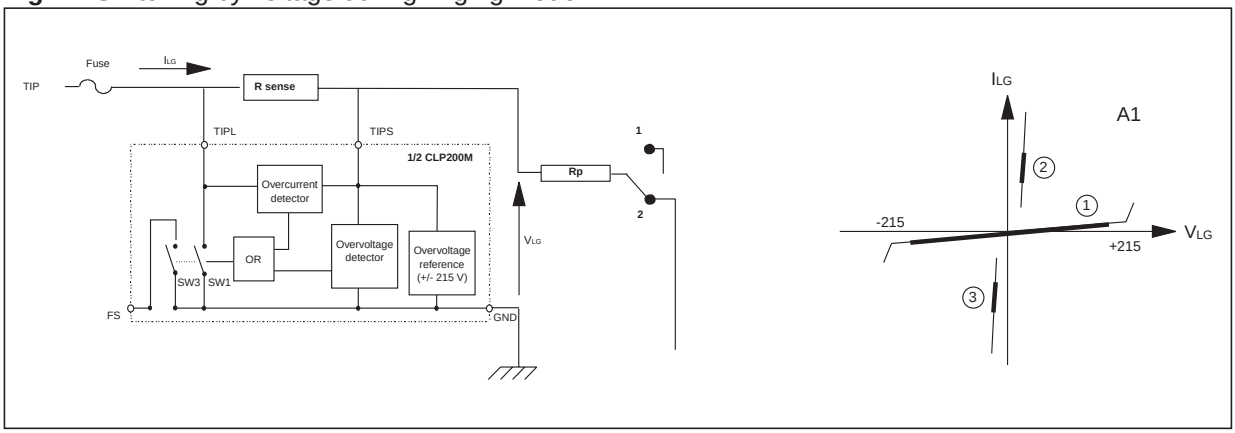
These two devices are complementary and their functions are explained below :

- The first stage based on CLP200M manages the high power issued from the external surges. When used in ringing mode, the CLP200M operates in voltage mode and provides a symmetrical and bidirectional overvoltage protection at +/-215 V on both TIP and RING lines. When used in speech mode, the CLP200M operates in current mode and the activation current of the CLP200M is adjusted by R_{SENSE}.
- The second stage is the external voltage reference device which defines the firing threshold voltage during the speech mode and also assumes a residual power overvoltage suppression. This protection stage can be either a fixed or programmable breakover device. The THDTxx family acts as a fixed breakover device while the LCP1511D operates as a programmable protection.

Thanks to this topology, the surge current in the line is reduced after the CLP200M. Because the remaining surge energy is low, the power ratings of Rp, the ring relay contacts and the external voltage reference circuit may be downsized. This results in a significant cost reduction.

2.3 Ringing mode

Fig. 4 : Switching by voltage during ringing mode.



In ringing mode (Ring relay in position 2), the only protection device involved is the CLP200M.

In normal conditions, the CLP200M operates in region 1 of **A1** curve, and is idle.

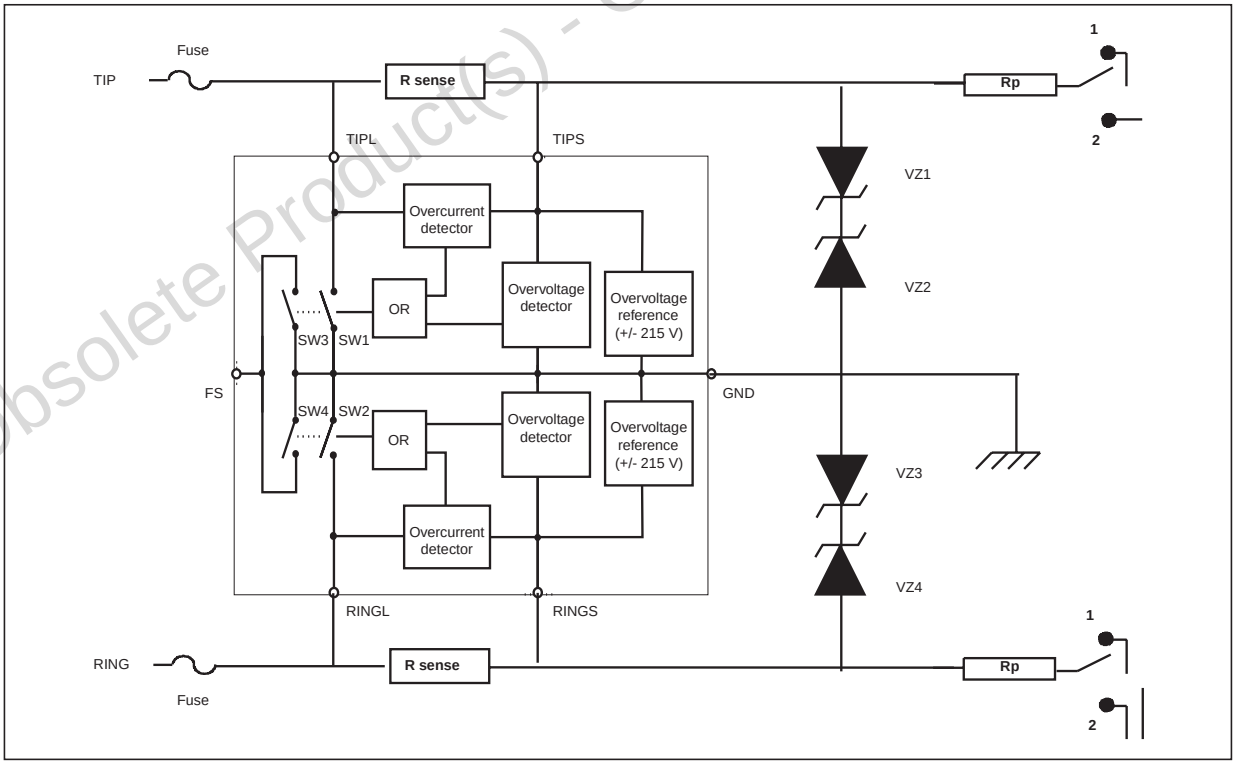
If an overvoltage occuring between TIP (or RING) and GND reaches the internal overvoltage refe-rence (+/- 215V), the CLP200M acts and the line is short-circuited to GND. At this time the operating point moves to region 2 for positive surges (region 3 for negative surges). Once the surge current disappears, the device returns to its initial state (region 1).

For surges occuring between TIP and RING, the CLP200M acts in the same way. This means that the CLP200M ensures a tripolar protection.

When used alone, the CLP200M acts at the internal overvoltage reference level (+/- 215V). Furthermore, it is possible to adjust this threshold level to a lower voltage by using :

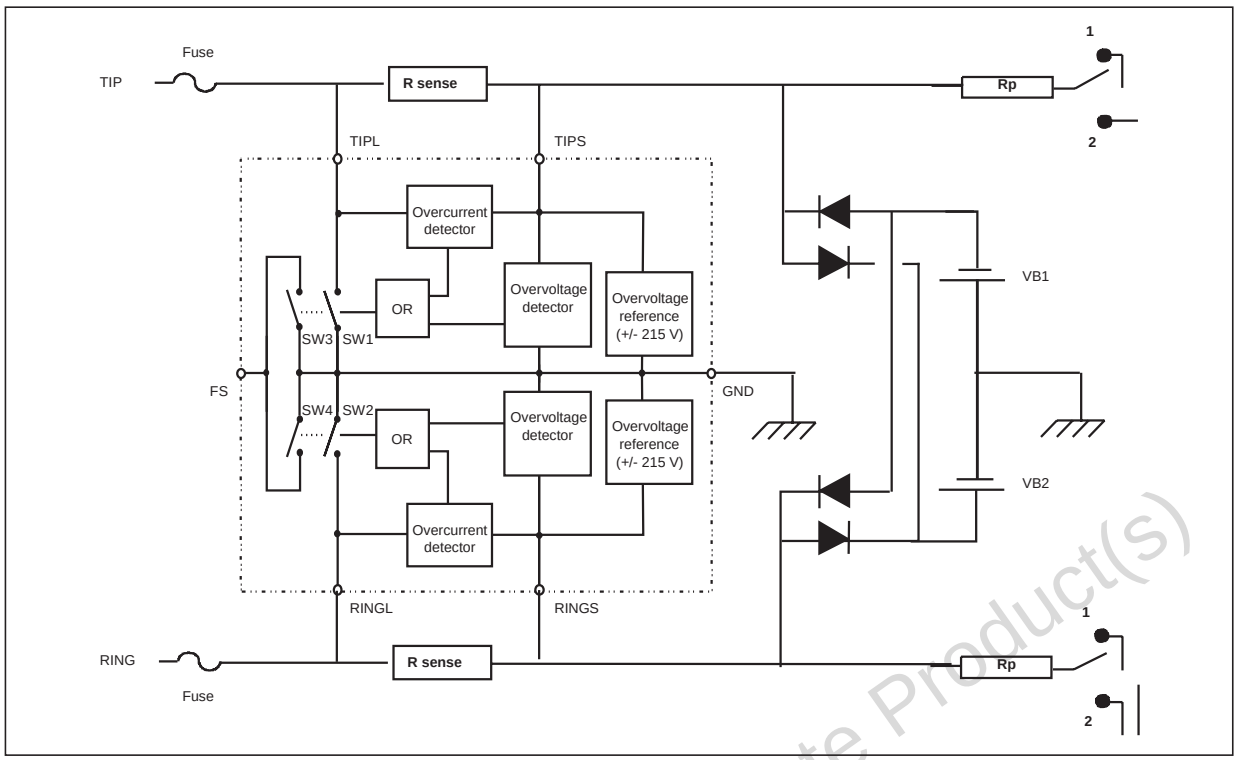
- up to 4 fixed external voltage reference (V_{Z1} to V_{Z4}) (see fig.5a).

Fig. 5a : Method to adjust the reference voltage**.**



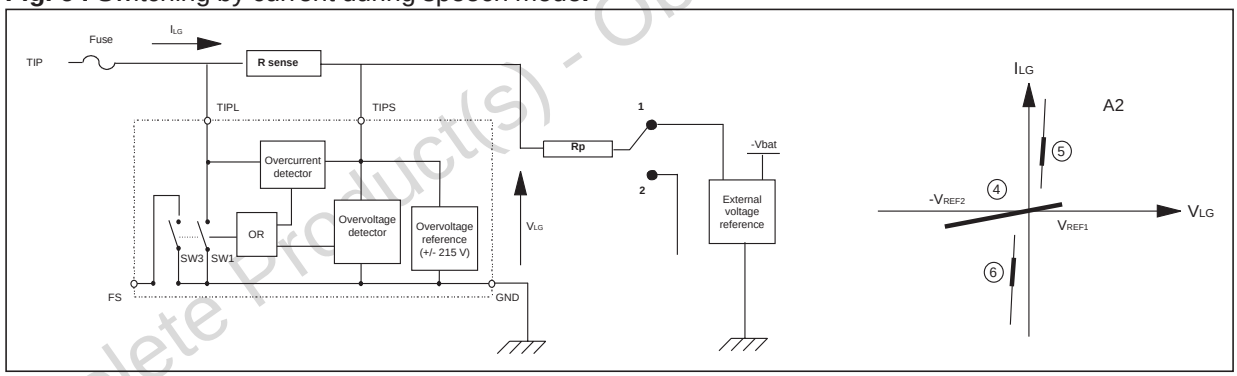
- external reference supplies, V_{b1} and V_{b2} (see fig.5b)..

Fig. 5b : Method to adjust the reference voltage.



2.4 Speech mode

Fig. 6 : Switching by current during speech mode.



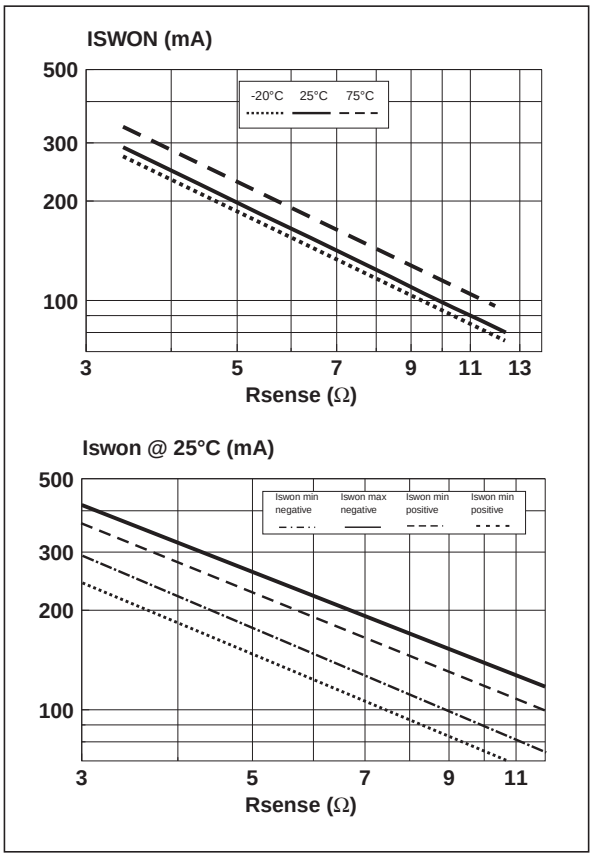
In speech mode (Ring relay in position 1), the protection is provided by the combination of both CLP200M and the external voltage reference device.
In normal conditions, the working point of this circuit is located in region 4 of **A2** curve : the CLP200M is idle.
When a surge occurs on the line, the external voltage reference device clamps at GND or $-V_{bat}$ respectively for positive and negative surges.
This generates a current which is detected by R_{SENSE} and causes the protection to act : the line is short-circuited to GND.

The operating point moves to region 5 for positive surges or region 6 for negative surges.
Once the surge current falls below the switching-off current I_{SWOFF}, the CLP200M returns to its initial state (region 4).

Furthermore, the CLP200M switches when an overvoltage, either positive or negative, occurs either :

- simultaneously on both TIP and RING lines versus GND.
- between TIP and RING.
- on TIP (or RING) versus GND.

Fig. 7a and 7b : Switching-on current versus R_{SENSE}.



The choice of the switching-on current is function of the R_{SENSE} resistors.

In normal operating condition, only the negative current of the signal is of interest. This current (typically below -150 mA) should not activate the protection device CLP200M. Therefore the level of activation is to be chosen just above this limit (typically -200 mA). This level is adjusted through R_{SENSE}.

Figures 7a and 7b enable the designers to choose the right R_{SENSE} value.

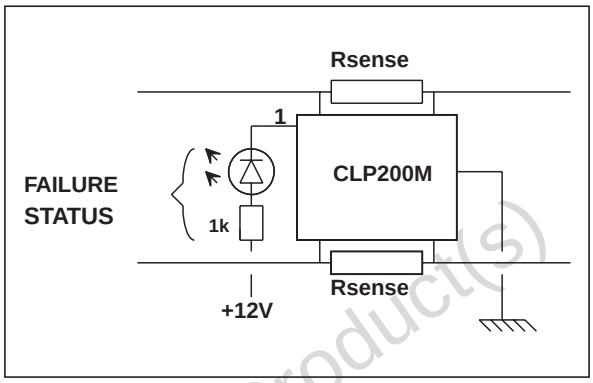
EXAMPLE :

The choice of R_{SENSE} = 4 Ω ensures a negative triggering of -220 mA min and -320 mA max. In this case, the positive triggering will be 180mA min and 280 mA max.

2.5 . Failure Status

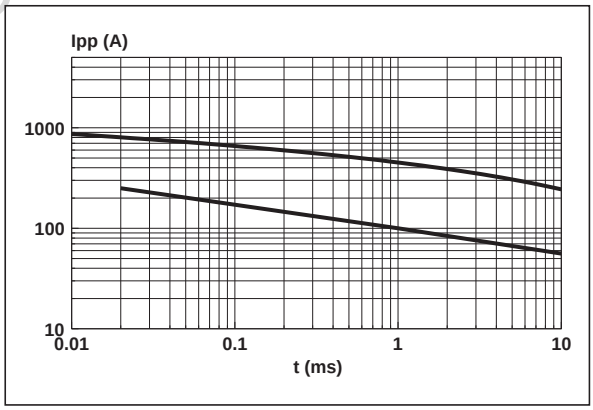
The CLP200M has an internal feature that allows the user to get a Failure Status (FS) indication. When the CLP200M is short-circuiting the line to GND, a signal can be managed through pin 1. This signal can be used to turn a LED on in order to provide a surge indication. It may also be used with a logic circuitry to count the number of disturbances appearing on the lines.

Fig. 8 : Failure Status circuit and diagnostic.



If a surge exceeding the maximum ratings of the CLP200M occurs on the line, the device will fail in a short-circuit state.

Fig. 9 : Operation limits and destruction zone of the CLP200M.



The figure 9 shows two different curves :

- The lower one indicates the maximum guaranted working limits of the CLP200M.
- The upper curve shows the limit above which the CLP200M is completely destructed . In this case, the Fail Diagnostic pin is on.

3. CLP200M TESTS RESULTS ACCORDING TO CCITT K20 RECOMMENDATIONS

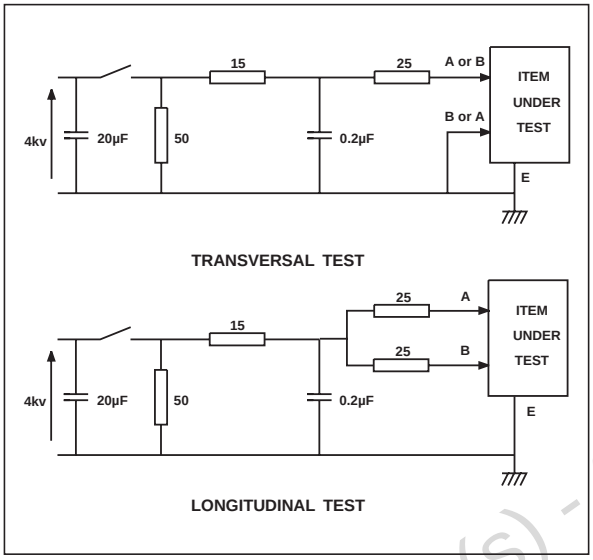
3.1 CCITT K20 Recommendations

In respect with the CCITT recommendations, the CLP200M has to withstand three kinds of disturbances.

3.1.1. Lightning simulation (Test 2, table 2/K20)

This test shall be done in transversal and longitudinal modes as shown in figure 10.

Fig. 10 : Transversal and longitudinal test topologies.



The test generator is the 10/700µs with 4kV of peak voltage.

3.1.2. Power induction (Test 3a and 3b, table 2/K20)

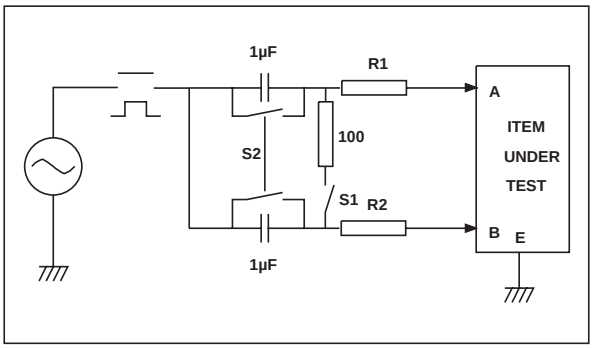
Two kinds of tests using the same circuit topology (see fig.11) are defined in the CCITT K20.

- Test 3a :
  Vac(max) = $300V_{RMS}$, R1 = R2 = 600Ω
  S2 operating and test duration = 200 ms.

- Test 3b :
  Vac(max) = $300V_{RMS}$ (*), R1 = R2 = 200Ω
  S2 operating and test duration not defined.

(*) Recommended value.

Fig. 11 : Power induction test circuit.

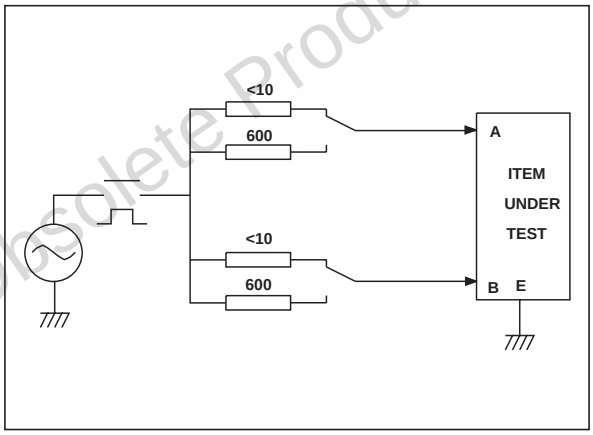


3.1.3. Power contact (Test 3, table 1/K20)

This test shall be done with the test circuit of figure 12.

Vac(max) = $220V_{RMS}$, with switch S in each position and duration 15 min.

Fig. 12 : Power contact test circuit.



3.1.4. Acceptance criteria and number of tests

For the tests described in chapter 3.1.1., 3.1.2. and 3.1.3. two criteria are defined :

A: Equipment shall withstand the test without damage and shall operate properly within the specified limits.

B: A fire hazard should not occur in the equipment as a result of the tests.

The criteria are affected to the different tests as mentioned in the table 1.

Table 1 : Acceptance criteria and number of tests.

TEST	ACCEPTANCE CRITERIA	NUMBER TO TESTS
2	A	10 for longitudinal A 10 for longitudinal B and 10 for transversal
3a	A	5
3b	B	1
3	B	1 for each position of s

3.2. Ringing mode

3.2.1. Lightning simulation test

Lightning phenomena are the most common surge causes. The purpose of this test is to check the robustness of the CLP200M against these lightning strikes.

Fig. 13 : Lightning simulation test.

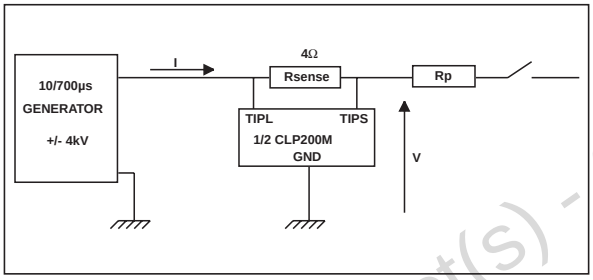


Fig. 14 : CLP200M response to a positive surge.

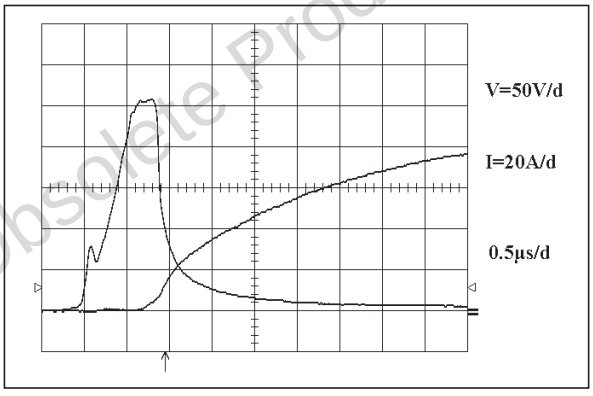
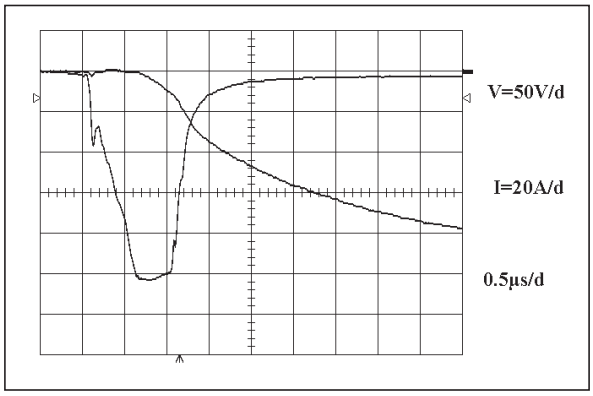


Fig. 15 : CLP200M response to a negative surge.



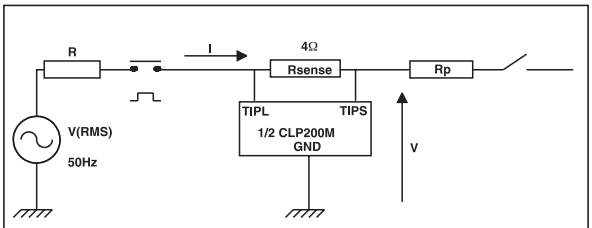
Figures 14 and 15 show that the remaining overvoltage does not exceed +/- 260 V. The CLP200M switches on within 0.7 µs and withstands the 100 A given by the CCITT K20 generator.

Consequently, the CLP200M totally fulfills this test.

3.2.2 Power induction (Test 3a and 3b table 2/K20)

Surges of long duration with medium voltage value are mainly produced by the proximity of a subscriber line with an AC mains line or equipment. The purpose of this test is to check the robustness of the CLP200M against these capacitive coupling disturbances.

Fig. 16 : Power inductance test.



TEST	$V_{(RMS)}$	R(Ω)	Duration
3a	300	600	0.2s
3b	300	200	?

Fig. 17 : CLP200M response to the induction test (Test 3a).

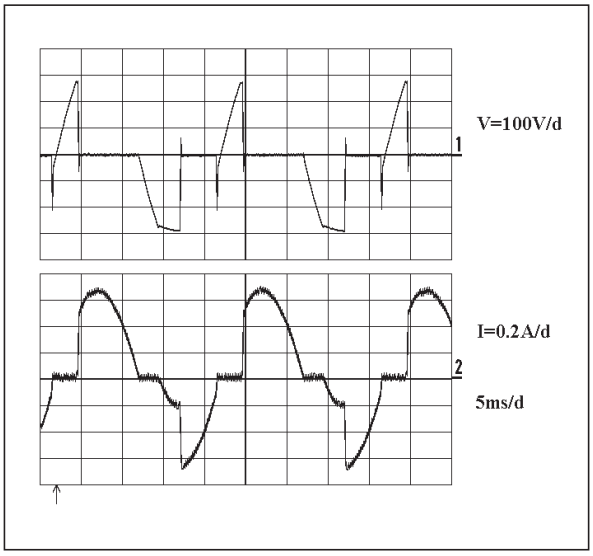
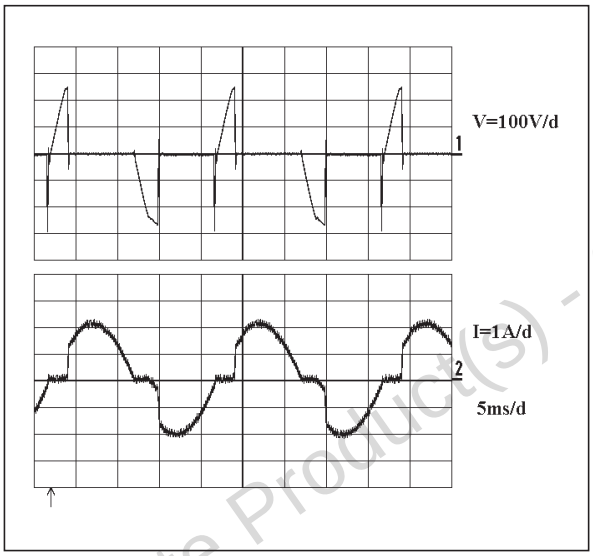


Fig. 18 : CLP200M reponse to the induction test (Test 3b).



Figures 17 and 18 show that the remaining voltage does not exceed 270 V.
Consequently, the CLP200M totally fulfills this test.

The test duration is not specified in test 3b. If the duration exceeds 5s we do suggest to follow the soldering and mounting recommendations given on page 17 of this document.

3.2.3 Power contact (Test 3 table 1/K20)

This long duration surge is produced when connecting a subscriber line to an AC mains line or equipment. The purpose of this test is to check the robustness of the CLP200M against these disturbances.

The test 3 of CCITT K20 requires a serial PTC (or fuse) which is inserted in the test circuit to limit the current rate. This PTC acts like an open-circuit in a non-instantaneous way when a surge occurs on the line. Meanwhile, the CLP200M has to withstand the surge.

Fig. 19 : Power contact test.

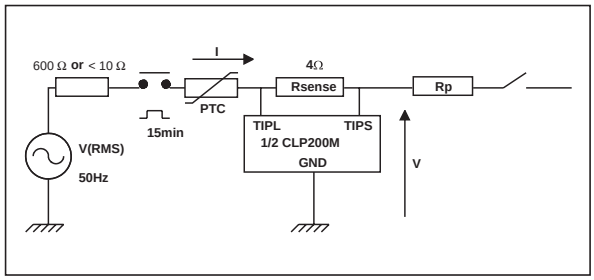


Fig. 20 : Power contact test 3 (With 10Ω series).

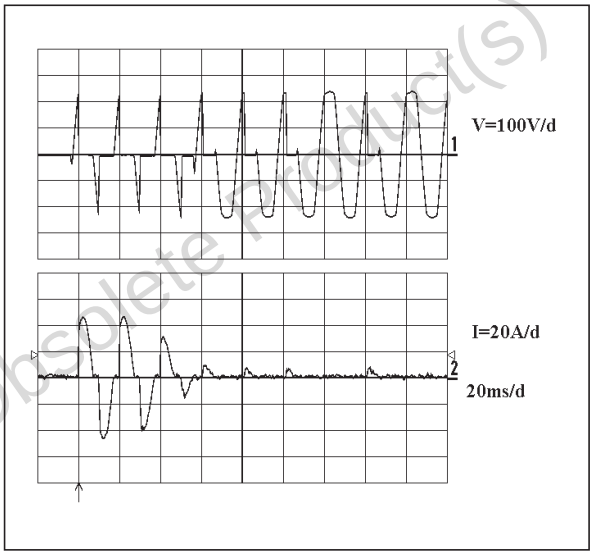


Figure 20 shows that the remaining overvoltage does not exceed 250 V and shows that the PTC acts like an open-circuit after 60 ms.
Consequently, the CLP200M totally fulfills this test.

3.3. Speech mode

3.3.1. Lightning simulation test (Test 2, table 2/K20)

Fig. 21: Lightning test in speech mode.

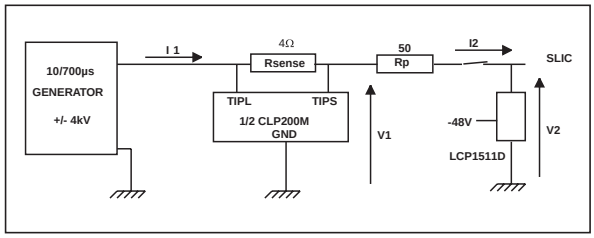


Fig. 22 : CLP200M response to a positive surge.

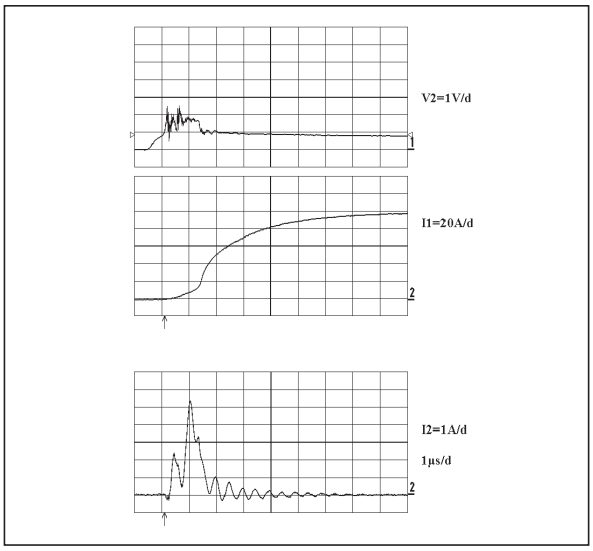
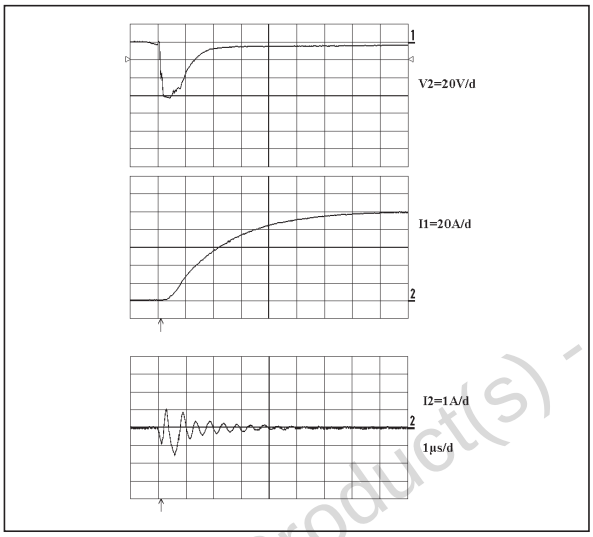


Fig. 23 : CLP200 M response to a negative surge.



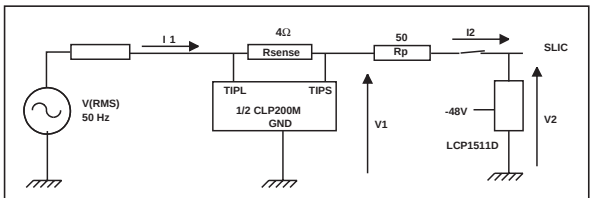
Figures 22 and 23 give the voltage and current behavior during positive and negative 4kV, 10/700µs, surge tests using a LCP1511D as second stage protection device. The firing threshold values are now adjusted to GND and to -Vbat (-48V) by the action of the second stage protection which acts as an external voltage reference.

As shown on these figures, the maximum remaining voltage does not exceed +2.5V for positive surges and -60V for negative surges.

Consequently, the CLP200M totally fulfills this test.

3.3.2 Power induction test (Test 3a and 3b, table 2/K20)

Fig. 24 : Power induction test.



TEST	$V_{(RMS)}$	R(Ω)	Duration
3a	300	600	0.2s

Figures 25 and 26 show that the maximum remaining voltage does not exceed +2V for positive surges and -55V for negative surges.
Consequently, the CLP200M totally fulfills this test.

The test duration is not specified in test 3b. If the duration exceeds 5s we do suggest to follow the soldering and mounting recommendations given on page 17 of this document.

Fig. 25 : Induction test behavior (Test 3a).

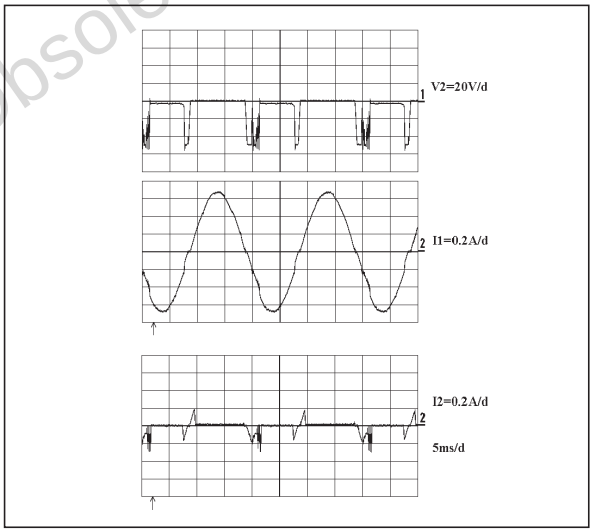
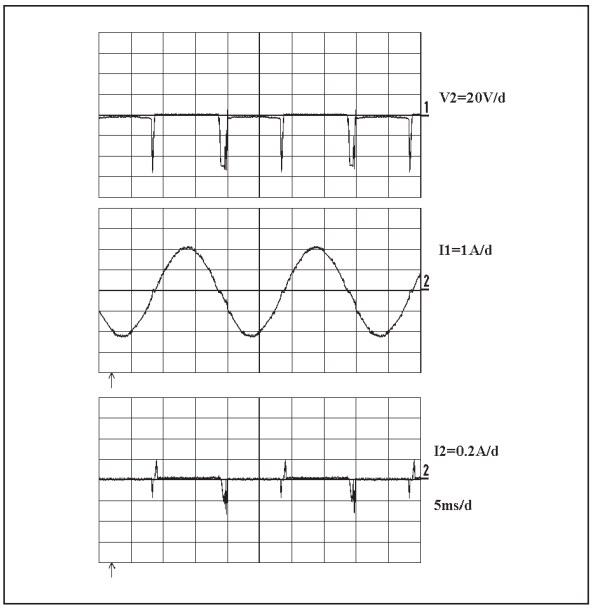


Fig. 26 : Induction test behavior (Test 3b).



3.3.3 - Power contact test (Test 3 table 1/K20)

The test 3 of CCITT K20 requires a serial PTC (or fuse) which is inserted in the test circuit to limit the current rate. This PTC acts like an open-circuit after 60 ms when a surge occurs on the line. Meanwhile, the CLP200M has to withstand the surge.

The protection device CLP200M totally fulfills this test.

Fig. 27 : Power contact test.

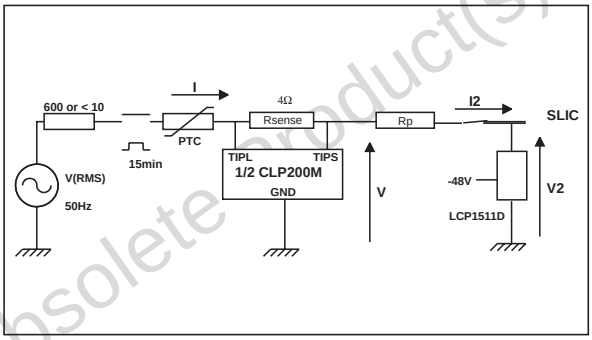
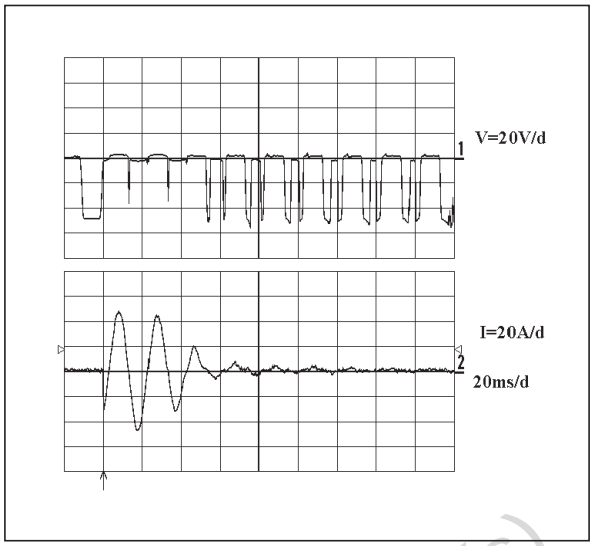


Fig. 28 : Power contact test 3 (with R ® 10 Ω series).



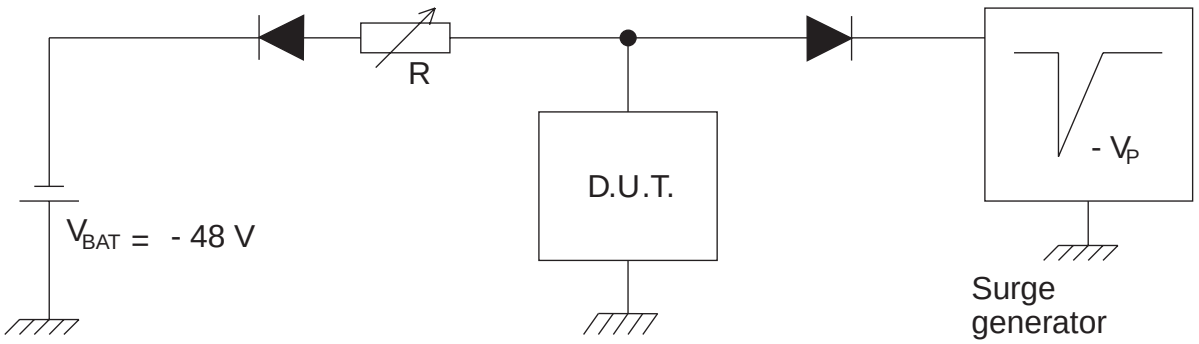
ABSOLUTE MAXIMUM RATINGS (R_{SENSE} = 4 Ω, and T_{amb} = 25 °C)

Symbol	Parameter	Test Conditions	Value	Unit
I_{PP}	Line to GND peak surge current	10/1000µs (open circuit voltage wave shape 10/1000µs)	100	A
		5/310µs (open circuit voltage wave shape 10/700µs)	150	A
I_{TSM}	Mains power induction current	V_{RMS} = 300V, R = 600Ω t = 200ms	0.5	A
	Mains power contact current	V_{RMS} = 220V, R = 10Ω (failure status threshold) t = 200 ms	22	A
		V_{RMS} = 220V, R = 600Ω t = 15 mn	0.30	A
T_{stg} T_j	Storage temperature range Maximum junction temperature		- 40 to + 150 150	°C
T_L	Maximum lead temperature for soldering during 10 s		260	°C

ELECTRICAL CHARACTERISTICS (R_{SENSE} = 4 Ω, and T_{amb} = 25°C)

Symbol	Parameter	Test Conditions	Value		Unit
			Min.	Max.	
I_{LGL}	Line to GND leakage current	. V_{LG} = 200 V . Measured between TIP (or RING) and GND		10	µA
V_{ref}	Overvoltage internal reference	. I_{LG} = 1 mA . Measured between TIP (or RING) and GND	215		V
V_{SWON}	Line to GND voltage at SW1 or SW2 switching-on	. Measured at 50 Hz between TIPL (or RINGL) and GND		290	V
I_{SWOFF}	Line to GND current at SW1 or SW2 switching-off	. Refer to test circuit page 14	150		mA
I_{SWON}	Line current at SW1 or SW2 switching-on	. Positive pulse . Negative pulse	180 220	280 320	mA
C	Line to GND capacitance	. V_{LG} = -1 V + 1V_{RMS} . F = 1 MHz		200	pF

TEST CIRCUIT FOR I_{SWOFF} PARAMETER : GO-NO GO TEST



This is a GO-NO GO test which allows to confirm the switch-off (I_{SWOFF}) level in a functional test circuit.

TEST PROCEDURE :

- Adjust the current level at the I_{SWOFF} value by short circuiting the D.U.T.
- Fire the D.U.T. with a surge current : I_{PP} = 10A, 10/1000µs.
- The D.U.T. will come back to the OFF-state within a duration of 50ms max.

Fig. 29 : Typical variation of switching-on current (positive or negative) versus R_{SENSE} resistor and junction temperature (see test condition Fig 31).

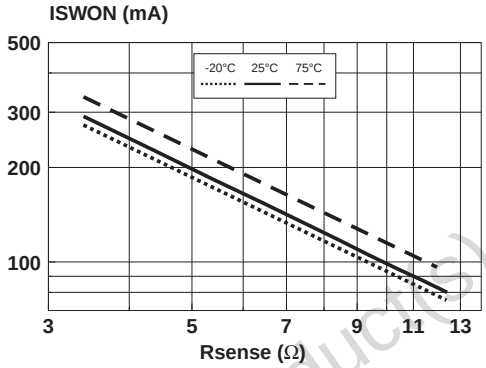


Fig. 30 : Variation of switching-on current versus R_{SENSE} at 25°C.

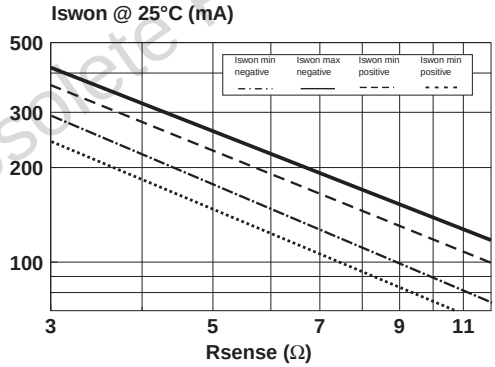


Fig. 31 : I_{SWON} MEASUREMENT

- Iswon = I1 when the CLP200M switches on (I1 is progressively increased using R)
- Both TIP and RING sides of the CLP200M are checked
- R_L = 10 Ω.

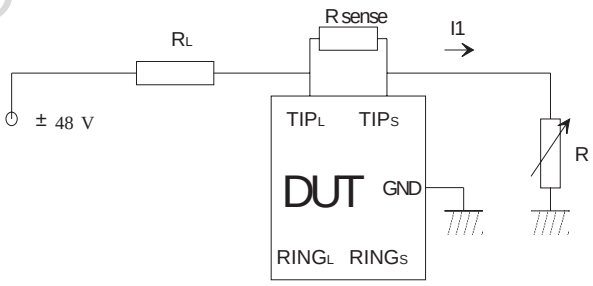


Fig. 32 : Relative variation of switching-off current versus junction temperature for R_{SENSE} between 3 and 10 Ω.

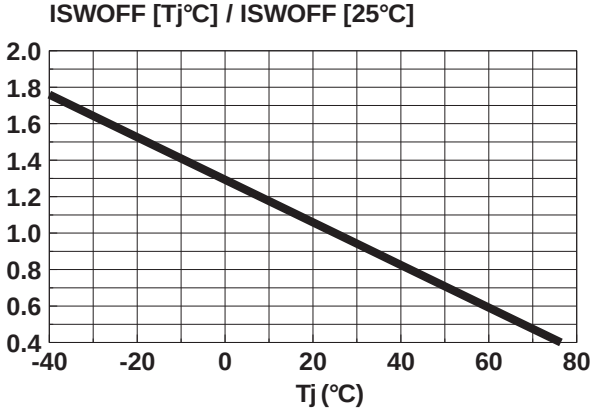


Fig. 33 : Relative variation of switching-off current versus R_{SENSE} (between 3 and 10 Ω).

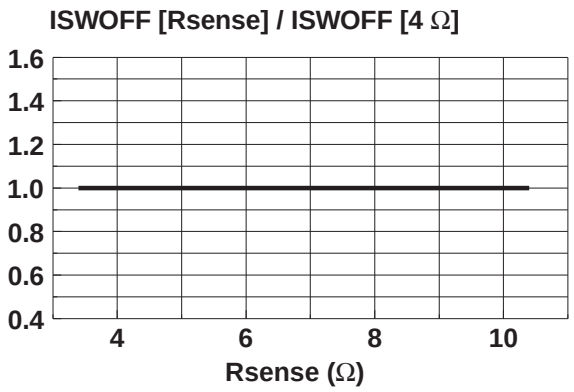


Fig. 34 : Residual current I1 after the CLP200M. The residual current I1 is defined by its peak value (I_P) and its duration (τ) @ I_P/2 .

Current surge input		Residual current after the CLP200M	
waveform(µs) I_{PP}(A)		Peak current I_P (A)	waveform t(µs)
5/310 130A	positive surge negative surge	4.2 1.1	1 0.5

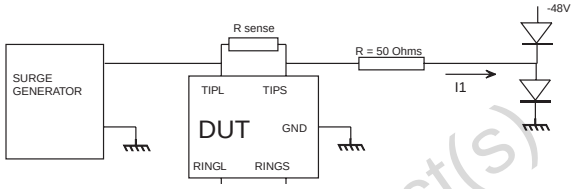


Fig. 35 : Relative variation of switching-on voltage versus dV/dt with an external resistor of 4 Ω.

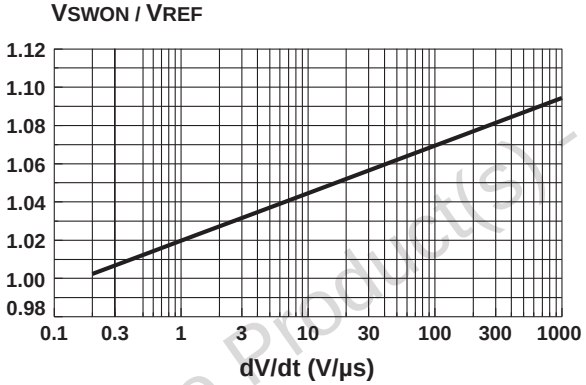


Fig. 36 : Relative variation of internal reference voltage versus junction temperature (I_{LG}=1mA).

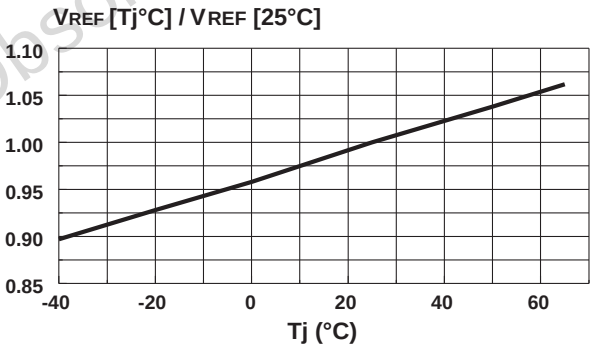


Fig. 37 : Junction capacitance (TIPL/GND) versus applied voltage

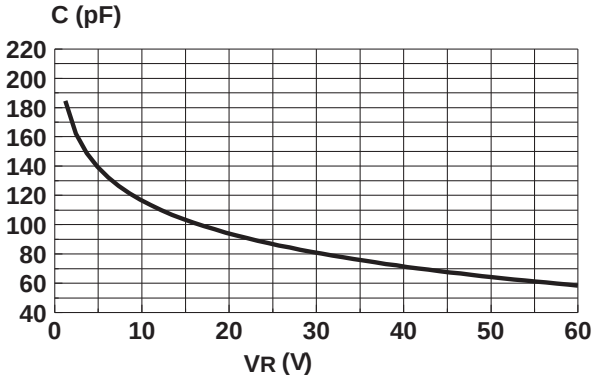


Fig. 38 : Typical and maximal capacitance between TIPL, RINGL and GND.

V TIPL = - 48 V
V RINGL # 0 V
V GND = 0 V

	Capacitance between RINGL and GND	Capacitance between TIPL and GND	Capacitance between TIPL and RINGL
Typ.	195	62	57
Max.	200		

Fig. 39 : Maximum non repetitive surge RMS on state current versus overload duration (with 50Hz sinusoidal wave and initial junction temperature equal to 25°C)

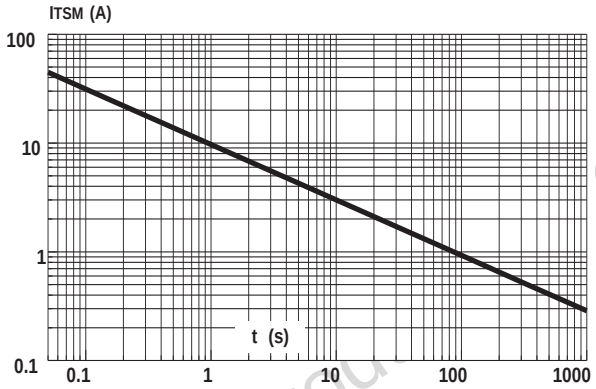
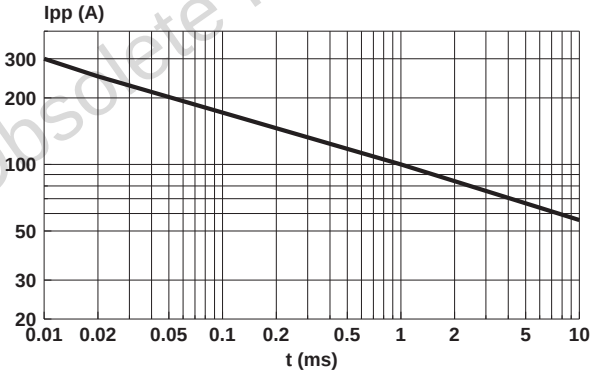


Fig. 40 : Maximum peak pulse current versus surge duration



SOLDERING RECOMMENDATION

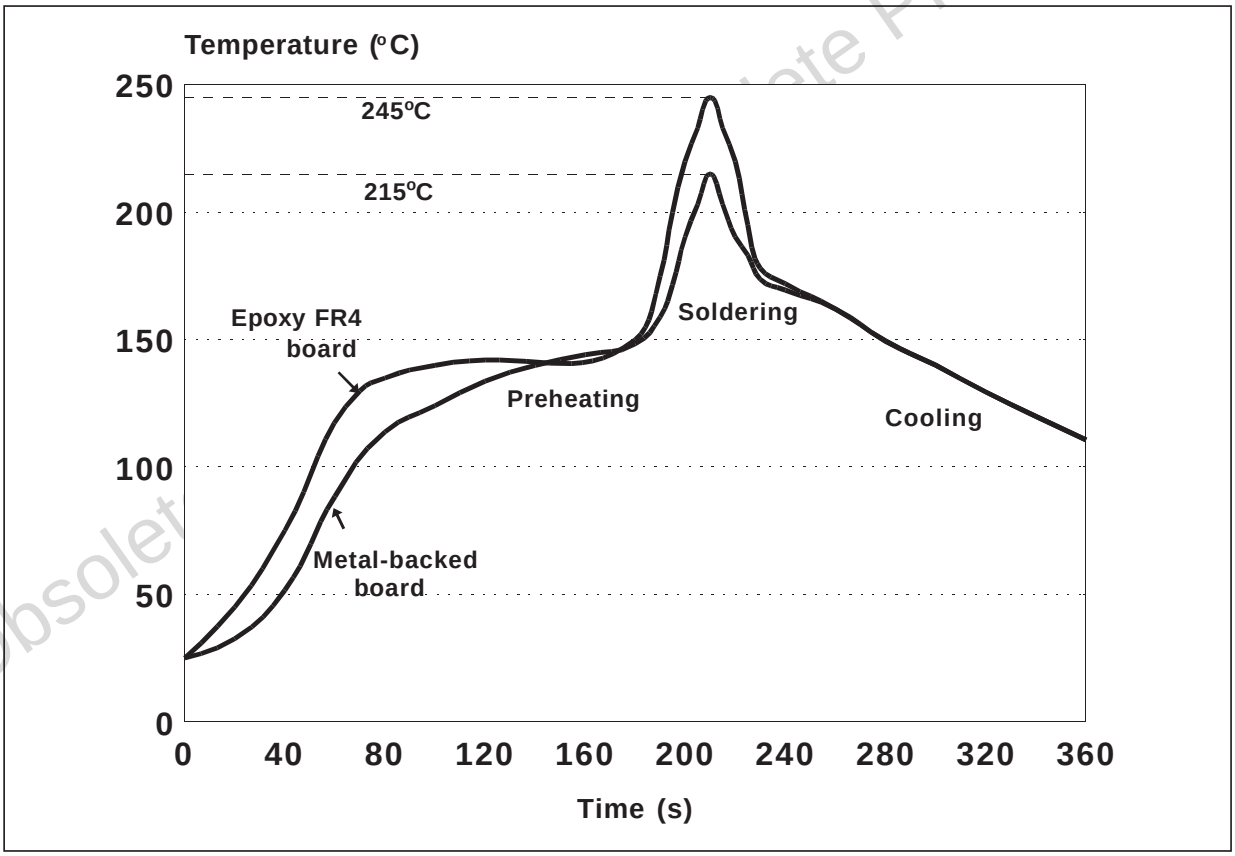
The soldering process causes considerable thermal stress to a semiconductor component. This has to be minimized to assure a reliable and extended lifetime of the device. The PowerSO-10™ package can be exposed to a maximum temperature of 260°C for 10 seconds. However a proper soldering of the package could be done at 215°C for 3 seconds. Any solder temperature profile should be within these limits. As reflow techniques are most common in surface mounting, typical heating profiles are given in Figure 1,either for mounting on FR4 or on metal-backed boards. For each particular board, the appropriate heat profile has to be adjusted experimentally. The present proposal is just a starting point. In any case, the following precautions have to be considered :

- always preheat the device
- peak temperature should be at least 30 °C higher than the melting point of the solder alloy chosen
- thermal capacity of the base substrate

Voids pose a difficult reliability problem for large surface mount devices. Such voids under the package result in poor thermal contact and the high thermal resistance leads to component failures. The PowerSO-10 is designed from scratch to be solely a surface mount package, hence symmetry in the x- and y-axis gives the package excellent weight balance. Moreover, the PowerSO-10 offers the unique possibility to control easily the flatness and quality of the soldering process. Both the top and the bottom soldered edges of the package are accessible for visual inspection (soldering meniscus).

Coplanarity between the substrate and the package can be easily verified. The quality of the solder joints is very important for two reasons : (I) poor quality solder joints result directly in poor reliability and (II) solder thickness affects the thermal resistance significantly. Thus a tight control of this parameter results in thermally efficient and reliable solder joints.

Fig 1 : Typical reflow soldering heat profile



SUBSTRATES AND MOUNTING INFORMATION

The use of epoxy FR4 boards is quite common for surface mounting techniques, however, their poor thermal conduction compromises the otherwise outstanding thermal performance of the PowerSO-10. Some methods to overcome this limitation are discussed below.

One possibility to improve the thermal conduction is the use of large heat spreader areas at the copper layer of the PC board. This leads to a reduction of thermal resistance to 35 °C for 6 cm^2 of the board heatsink (see fig. 2).

Use of copper-filled through holes on conventional FR4 techniques will increase the metallization and decrease thermal resistance accordingly. Using a configuration with 16 holes under the spreader of the package with a pitch of 1.8 mm and a diameter of 0.7 mm, the thermal resistance (junction - heatsink) can be reduced to 12°C/W (see fig. 3). Beside the thermal advantage, this solution allows multi-layer boards to be used. However, a drawback of this traditional material prevent its use in very high power, high current circuits. For instance, it is not advisable to surface mount devices with currents greater than 10 A on FR4 boards. A Power Mosfet or Schottky diode in a surface mount power package can handle up to around 50 A if better substrates are used.

Fig 2 : Mounting on epoxy FR4 head dissipation by extending the area of the copper layer

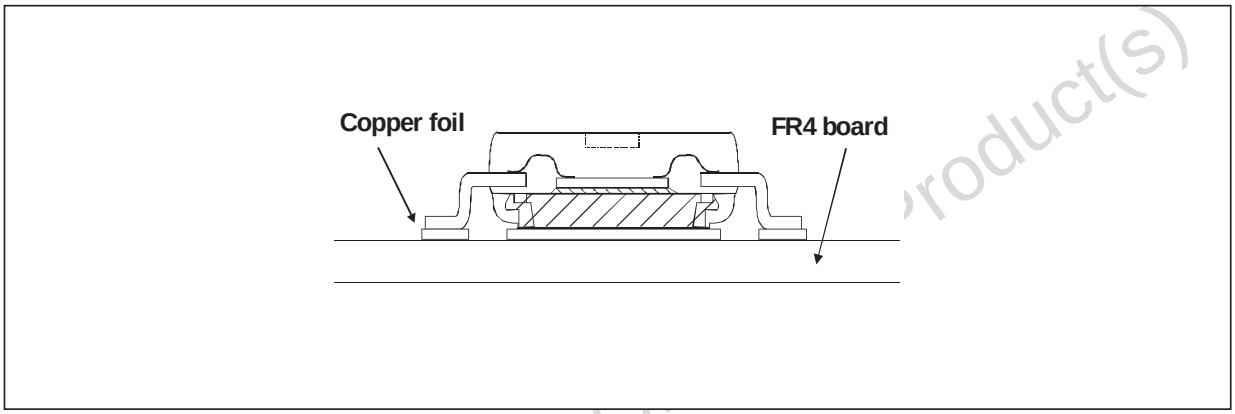
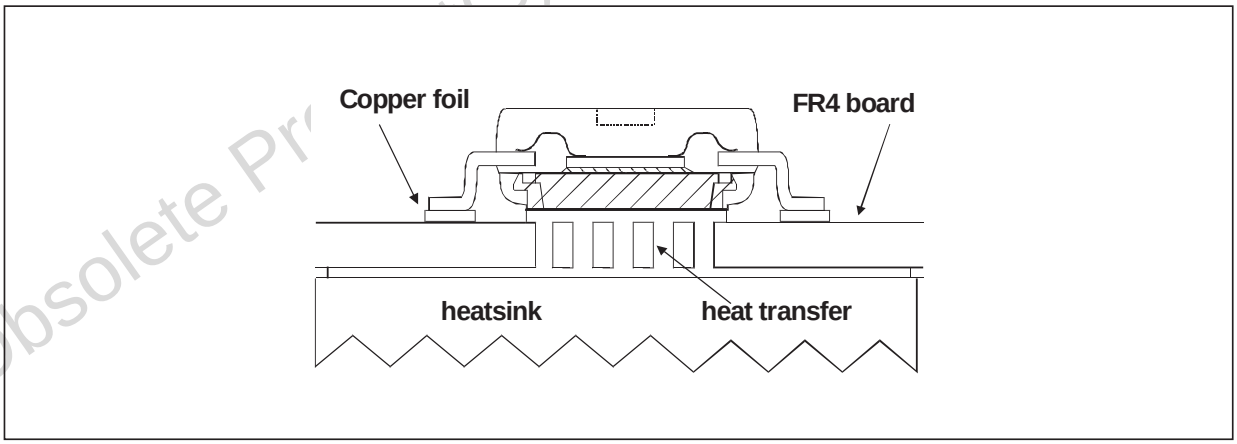


Fig 3 : Mounting on epoxy FR4 by using copper-filled through holes for heat transfer



A new technology available today is IMS - an Insulated Metallic Substrate. This offers greatly enhanced thermal characteristics for surface mount components. IMS is a substrate consisting of three different layers, (I) the base material which is available as an aluminium or a copper plate, (II) a thermal conductive dielectrical layer and (III) a copper foil, which can be etched as a circuit layer. Using this material a thermal resistance of 8°C/W with 40 cm^2 of board floating in air is achievable (see fig. 4). If even higher power is to be dissipated an external heatsink could be applied which leads to an R_{th}(j-a) of 3.5°C/W (see Fig. 5), assuming that R_{th} (heatsink-air) is equal to R_{th} (junction-heatsink). This is commonly applied in practice, leading to reasonable heatsink dimensions. Often power devices are defined by considering the maximum junction temperature of the device. In practice , however, this is far from being exploited. A summary of various power management capabilities is made in table 1 based on a reasonable delta T of 70°C junction to air.

Fig 4 : Mounting on metal backed board

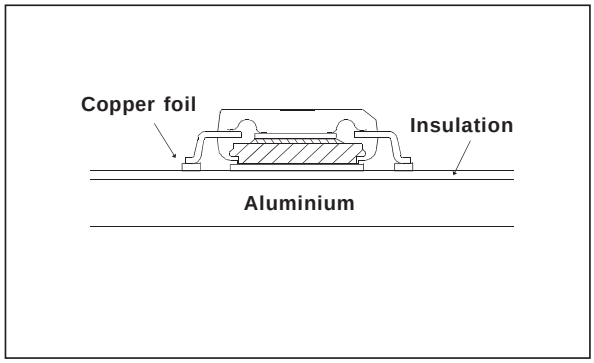
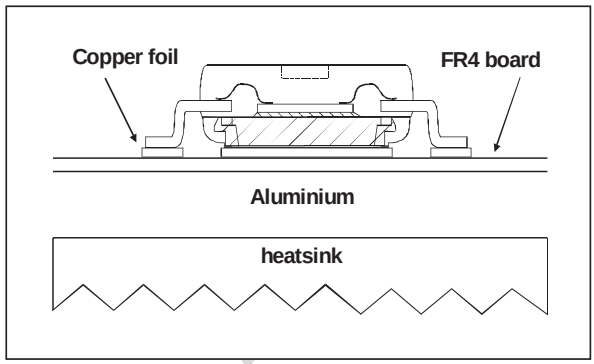


Fig 5 : Mounting on metal backed board with an external heatsink applied



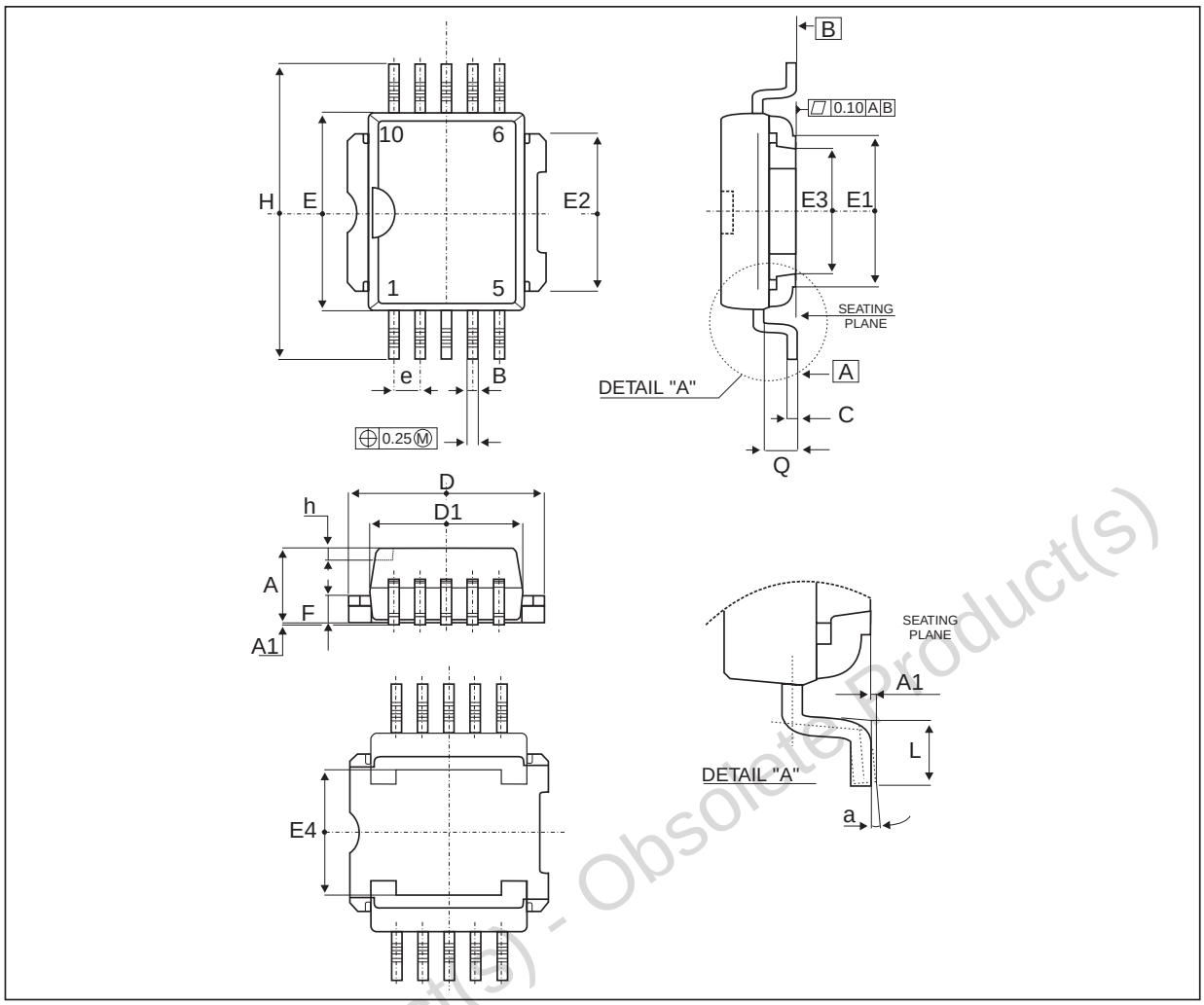
The PowerSO-10 concept also represents an attractive alternative to C.O.B. techniques. PowerSO-10 offers devices fully tested at low and high temperature. Mounting is simple - only conventional SMT is required - enabling the users to get rid of bond wire problems and the problem to control the high temperature soft soldering as well. An optimized thermal management is guaranteed through PowerSO-10 as the power chips must in any case be mounted on heat spreaders before being mounted onto the substrate.

TABLE 1 : THERMAL IMPEDANCE VERSUS SUBSTRATE

PowerSo-10 package mounted on	R_{th} (j-a)	P Diss (*)
1.FR4 using the recommended pad-layout	50 °C/W	1.5 W
2.FR4 with heatsink on board (6cm^2)	35 °C/W	2.0 W
3.FR4 with copper-filled through holes and external heatsink applied	12 °C/W	5.8 W
4. IMS floating in air (40 cm^2)	8 °C/W	8.8 W
5. IMS with external heatsink applied	3.5 °C/W	20 W

(*) Based on a delta T of 70 °C junction train.

PACKAGE MECHANICAL DATA



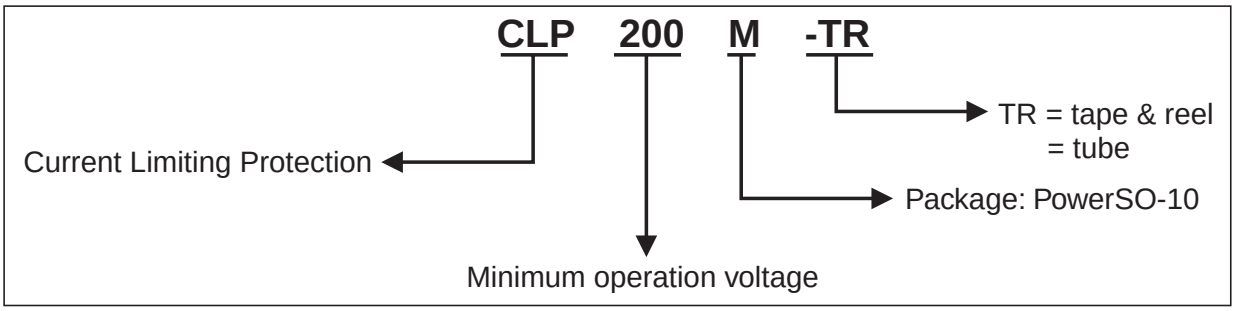
REF.	DIMENSIONS					
	Millimeters			Inches		
	Min.	Typ.	Max.	Min.	Typ.	Max.
A	3.35		3.65	0.131		0.143
A1	0.00		0.10	0.00		0.0039
B	0.40		0.60	0.0157		0.0236
C	0.35		0.55	0.0137		0.0217
D	9.40		9.60	0.370		0.378
D1	7.40		7.60	0.291		0.299
E	9.30		9.50	0.366		0.374
E1	7.20		7.40	0.283		0.291
E2	7.20		7.60	0.283		0.299

REF.	DIMENSIONS					
	Millimeters			Inches		
	Min.	Typ.	Max.	Min.	Typ.	Max.
E3	6.10		6.35	0.240		0.250
E4	5.90		6.10	0.232		0.240
e		1.27			0.05	
F	1.25		1.35	0.0492		0.0531
H	13.80		14.40	0.543		0.567
h		0.50			0.019	
L	1.20		1.80	0.0472		0.0708
Q		1.70			0.067	

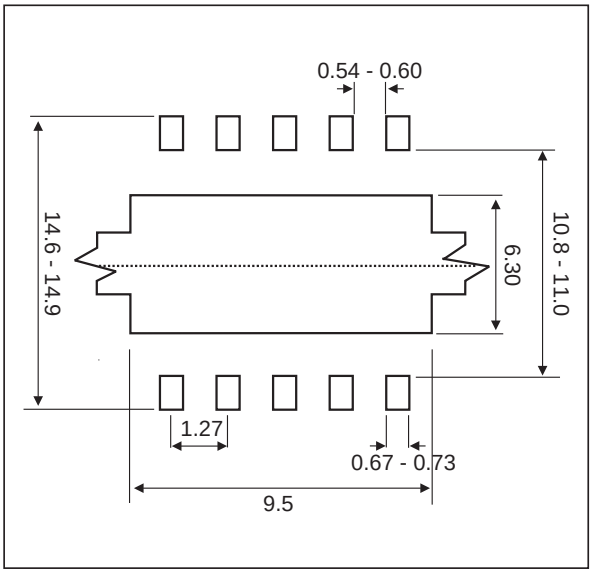
MARKING

Package	Type	Marking
Power SO-10™	CLP200M	CLP200M

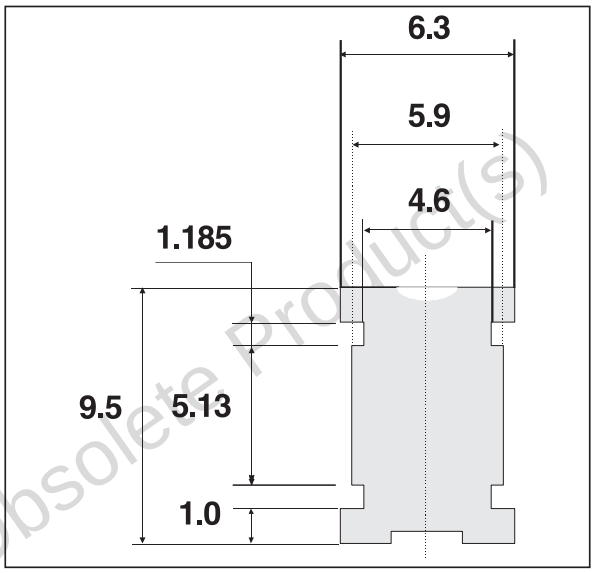
ORDER CODE



FOOT PRINT
MOUNTING PAD LAYOUT RECOMMENDED

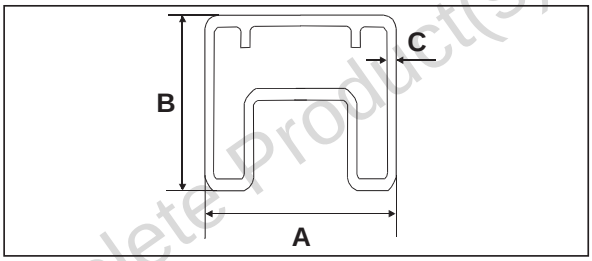


HEADER SHAPE



Dimensions in millimeters

SHIPPING TUBE



	DIMENSIONS (mm)
	TYP
A	18
B	12
C	0,8
Length tube	532
Quantity per tube	50

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