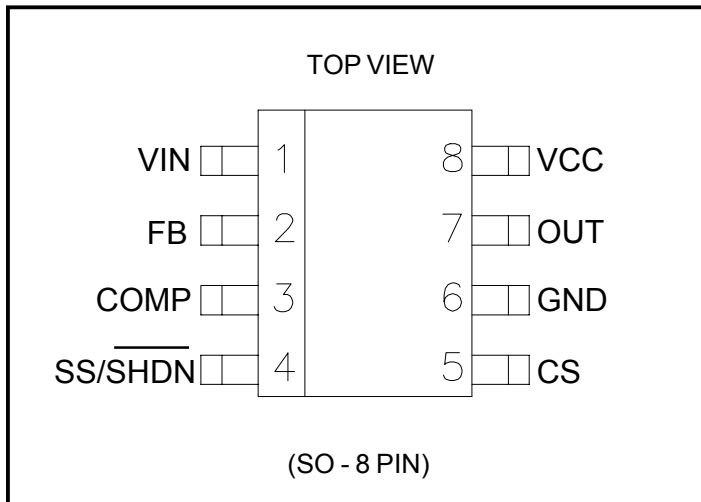


POWER MANAGEMENT
Pin Configuration

Ordering Information

Part Number	Top Mark	Package
SC4812STRT ⁽¹⁾⁽²⁾	SC4812	SO-8
SC4812EVB	Evaluation Board	

Notes:

- (1) Only available in tape and reel packaging. A reel contains 2500 devices.
- (2) Lead free product. This product is fully WEEE and RoHS compliant.

Absolute Maximum Ratings

Exceeding the specifications below may result in permanent damage to the device, or device malfunction. Operation outside of the parameters specified in the Electrical Characteristics section is not implied. Exposure to Absolute Maximum rated conditions for extended periods of time may affect device reliability.

Parameter	Symbol	Maximum	Units
Input Voltage	V_{IN}	-0.5 to 100	V
Supply Voltage	V_{CC}	-0.5 to 18	V
Supply Current	I_{CC}	20	mA
FB, COMP, CS, and SS/SHDN to GND		-0.5 to 7	V
OUT Peak Current		±1	A
Continuous Power Dissipation	P_D	Internally limited	W
Junction Temperature Range	T_J	-40 to +150	°C
Thermal Resistance ⁽¹⁾	θ_{JA}	105	°C/W
Storage Temperature Range	T_{STG}	-65 to +150	°C
Lead Temperature (Soldering) 10 Sec.	T_{LEAD}	+300	°C

Note:

- (1) Mounted to 3" x 4.5", 4 layer FR4 PCB in still air per JESD51 standards.

POWER MANAGEMENT
Electrical Characteristics

Unless specified: $V_{CC} = 12V$, a 10 μF capacitor connects V_{CC} to GND, $V_{CS} = 0$, $V_{IN} = 48V$, a 0.1 μF capacitor connects SS/SHDN to GND, OUT = open circuit, FB = GND, $T_A = T_J = -40$ to $+125^\circ C$. Typical values are at $T_A = 25^\circ C$

Parameter	Test Conditions	Min	Typ	Max	Unit
Startup/Winding Regulator					
V_{IN} Input Voltage Range		12		90	V
V_{IN} Supply Current	$V_{IN} = 90V$, V_{CC} open, driver switching		5	7.5	mA
	$V_{IN} = 90V$, V_{CC} open, $V_{FB} = 3V$, driver not switching		3.5	5	mA
V_{IN} Supply Current after Startup	$V_{IN} = 90V$		50	100	μA
V_{IN} Shutdown Current	$V_{IN} = 90V$, $V_{SS/SHDN} = 0$		250	380	μA
V_{CC} Output Voltage	Power from V_{IN}	6.8	7.4	8	V
V_{CC} Current Limit	10% below no load V_{CC} output voltage	12	20		mA
V_{CC} Supply					
V_{CC} Turn-on Voltage		6	6.5	6.7	V
Hysteresis		0.8	1	1.4	V
Operating Current			3	7.5	mA
V_{CC} Zener Shunt Voltage	$I_{CC} = 10mA$	15.25	16.25	17.25	V
Error Amplifier					
Feedback Input Voltage	close loop	2.44	2.50	2.56	V
Feedback Input Voltage Regulation	$V_{CC} = 8V$ to $14V$	2.425		2.575	V
Input Bias Current			0.5	0.8	μA
Amplifier Transconductance			1000		μmho
Amplifier Source Current			110		μA
Amplifier Sink Current			110		μA
Open Loop Voltage Gain			60		dB
PWM Comparator					
Slope Compensation			28		mV/ μS
Oscillator					
Clock Frequency Range		235	260	285	kHz
Max Duty Cycle		75	80	85	%

POWER MANAGEMENT
Electrical Characteristics (Cont.)

Unless specified: $V_{CC} = 12V$, a 10uF capacitor connects V_{CC} to GND, $V_{CS} = 0$, $V_{IN} = 48V$, a 0.1uF capacitor connects SS/SHDN to GND, OUT = open circuit, FB = GND, $T_A = T_J = -40$ to $+125^\circ C$. Typical values are at $T_A = 25^\circ C$

Parameter	Test Conditions	Min	Typ	Max	Units
Current Limit					
CS Threshold Voltage		419	465	510	mV
CS Input Bias Current	$0 \leq V_{CS} \leq 2V$	-1		1	μA
Propagation Delay to Gate			70		nS
CS Blanking Time			70		nS
Soft Start					
SS Source Current	$V_{SS/SHDN} = 0$	4	6	8	μA
SS Sink Current			1		mA
Shutdown Threshold	$V_{SS/SHDN}$ falling	0.25	0.5	0.6	V
	$V_{SS/SHDN}$ rising	0.61	0.7	0.8	
Output					
Peak Source Current			570		mA
Peak Sink Current			1000		mA
Rise Time	$C_L = 1nF$		45		nS
Fall Time	$C_L = 1nF$		35		nS
Thermal Shutdown					
Thermal Shutdown Temperature			150		$^\circ C$
Thermal Hysteresis			25		$^\circ C$

Note:

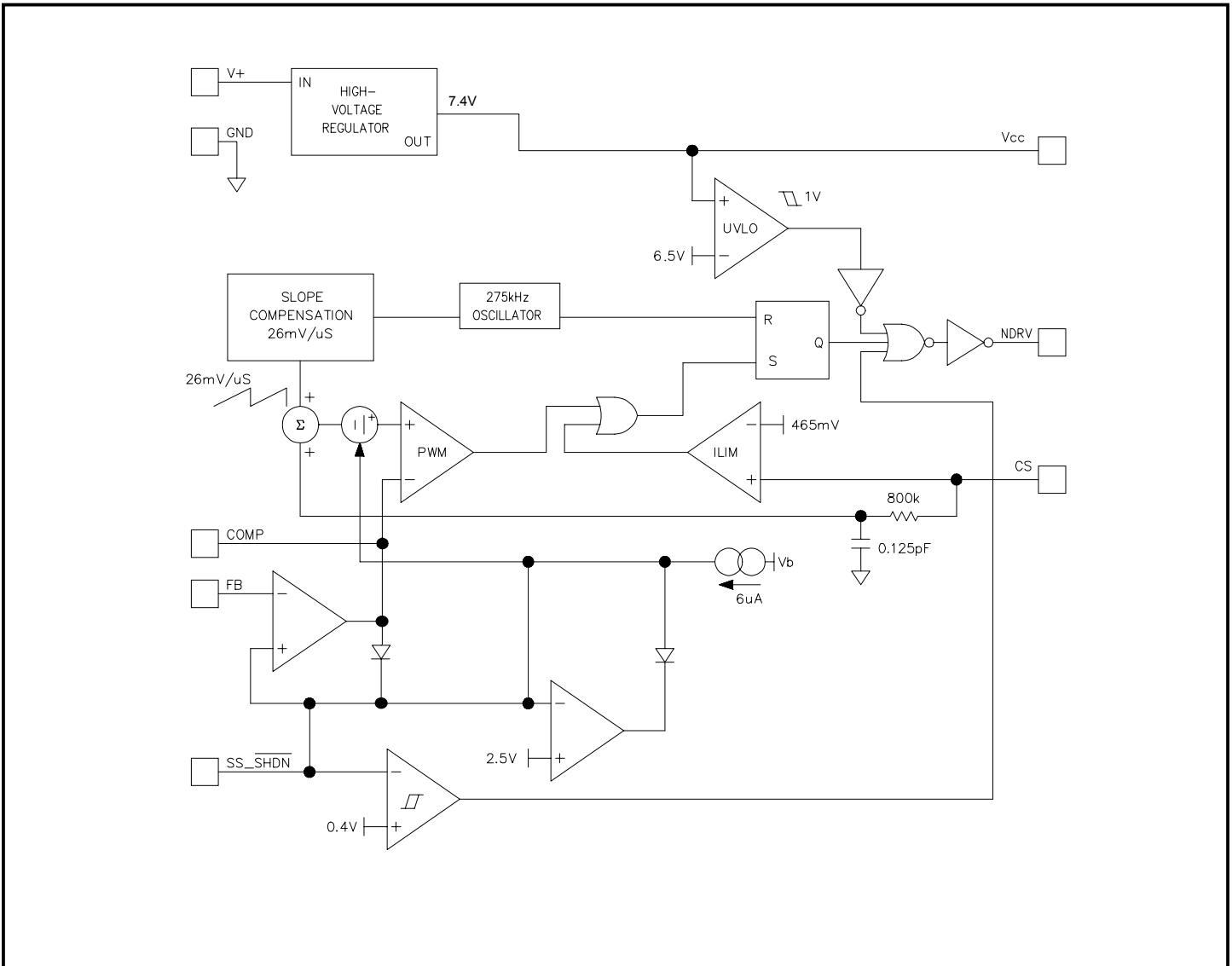
(1) This device is ESD sensitive. Use of standard ESD handling precautions is required.

POWER MANAGEMENT
Pin Descriptions

Pin #	Pin Name	Pin Function
1	VIN	High voltage startup input. Connect directly to an input voltage between 12 to 90V. Connects internally to a high voltage linear regulator that generates V_{CC} during startup.
2	FB	Feedback input to the internal transconductance error amplifier. V_{FB} sensed the regulated output voltage through an external resistor divider.
3	COMP	Internal transconductance error amplifier output. Compensation network of the overall loop is placed between this pin and GND.
4	SS/ $\overline{\text{SHDN}}$	Soft start timing capacitor connection. Ramp time to full current limit is approximately TBD ms/nF. This pin is also the reference voltage output. Bypass with a minimum 10nF capacitor to GND. The device goes into shutdown when $V_{SS,\overline{\text{SHDN}}}$ is pulled below 0.25V.
5	CS	Current sense input. Turns power switch off if V_{CS} rises above 465mV for cycle-by-cycle current limiting. CS is also the feedback for the current mode controller. CS is connected to the PWM comparator through a leading edge blanking circuit.
6	GND	Ground.
7	OUT	Gate drive. Drives a high voltage external N-channel power MOSFET.
8	VCC	Supply voltage. Provides power for entire IC. V_{CC} is regulated from V_{IN} during startup. Bypass V_{CC} with a 10uF tantalum capacitor in parallel with 0.1uF ceramic capacitor to GND.

POWER MANAGEMENT

Block Diagram



POWER MANAGEMENT
Application Information
Introduction

The SC4812 is a 8 pin peak current mode controlled PWM controller for isolated or non-isolated DC-DC switching power supplies. It features an internal startup regulator, programmable external soft start and programmable cycle-by-cycle current limit. It operates in a fixed frequency at 260KHz.

The SC4812 can be applied in a flyback or forward topology with the input voltage ranging from 36V to 75V.

Startup Regulator

The internal startup regulator of the SC4812 makes its initial startup without a lossy startup resistor or external startup circuitry to save cost and board space. As input voltage exceeds 12V, it provides regulated 7.4V to V_{CC} which is with the maximum turn-on voltage 6.7V.

Soft-Start/Shutdown and V_{CC} Lockout

During power startup, the output voltage has to ramp up in a controlled manner to avoid overshoot. The SC4812 internal non-inverting terminal to the error amplifier is connected to the soft-start pin, which forces the internal 2.5V reference to gradually ramp up during power startup. In a non-isolated application, as the internal error amplifier is used, output voltage of a converter ramps up with close loop startup fashion smoothly. In case of an isolated application in which the internal error amplifier may not be used, isolated voltage feedback is through an opto-coupler and connected to the COMP pin. During power startup, the COMP pin will follow the soft-start pin voltage through an internal diode.

Soft-start operation begins when SS/SHDN ramps above 0.7V. When soft-start completed, SS/SHDN is regulated to 2.50V, the internal voltage reference. Pull SS/SHDN below 0.5V to disable the controller.

Undervoltage lockout shuts down the controller when V_{CC} is less than 5.5V. The internal startup regulator and the reference remain on during shutdown.

Current-Sense

The function of the CS pin is to limit the peak current through the MOSFET. Current is sensed at CS as a voltage across a sense resistor between the source of the MOSFET and GND. An RC filter is recommended to connect CS to the sense resistor to reduce effect of the MOSFET turn-on leading edge spike and noise. Select the current-sense resistor with the following equation:

$$R_s = 0.465V / (1.2 \times I_{LIM_PRI})$$

where I_{LIM_PRI} is the maximum peak primary-side current. When $V_{CS} > 465mV$, the power MOSFET turns off after 70nS propagation delay from the switch current reaches the trip point to the driver.

PWM Comparator and Slope Compensation

The SC4812 runs fixed 260 KHz frequency by an internal oscillator. At the beginning of each switching cycle, the OUT pin switches the MOSFET on. the OUT pin switches off after the 80% maximum duty cycle has been reached, regardless of the feedback.

Since an artificial slope is required for current-mode operation when duty cycle is larger than 50%, the SC4812 uses an internal ramp generator for slope compensation. The internal ramp signal is reset at the beginning of each cycle and slews at 26mV/ μ S.

The PWM comparator compares the instantaneous primary peak current to the feedback error signal through the opto-coupler, the internal offset and slope compensation and determine when to turn off the MOSFET. In steady state operation, the MOSFET turns off when:

$$I_{LIM_PRI} \cdot R_s > V_{OPTO} - V_{OFFSET} - V_{SLOPE}$$

where I_{LIM_PRI} is the current on the primary side through the MOSFET. V_{OFFSET} is 1.5V internal offset voltage and V_{SLOPE} is the artificial ramp starting at with slew rate 26mV/ μ S.

When selecting an inductor in a forward-converter or magnetizing inductance in a flyback-converter, the following condition must be met to avoid control-loop sub-harmonic oscillations:

$$\frac{N_s}{N_p} \times \frac{K \times R_s \times V_o}{L} = 26mV / \mu S$$

where $K = 0.5$ TO 1 , AND N_s and N_p are the turns of the main transformer on secondary and primary side respectively. L is the output inductor on secondary side in a forward-converter or magnetizing inductance on secondary side in a flyback-converter.

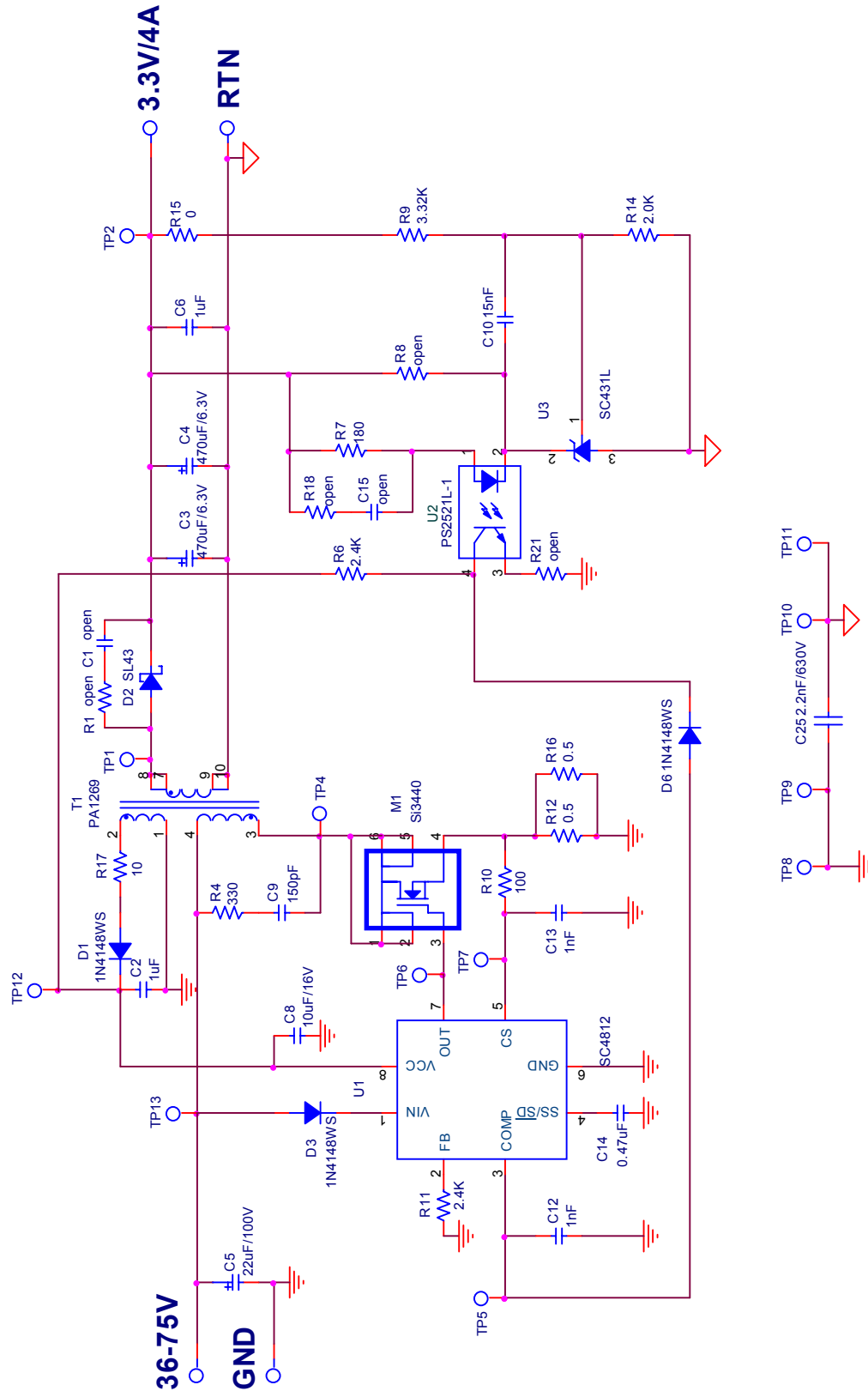
POWER MANAGEMENT**Applications Information (Cont.)****PCB Layout Guideline**

PCB layout is very critical, and the following should be considered to insure proper operation of the SC4812. High switching currents are present in applications and their effect on ground plane must be understood and minimized.

- 1) The high power parts of the circuit should be placed on a board first. A ground plane should be used. Isolated or semi-isolated areas of the ground plane may be deliberately introduced to constrain ground currents to particular areas, for example the input capacitor and the main switch FET ground.
- 2) The loop formed by the Input Capacitor(s) (C_{in}), the main transformer and the main switch FET must be kept as small as possible. This loop contains all the high fast transient switching current. Connections should be as wide and as short as possible to minimize loop inductance. Minimizing this loop area will a) reduce EMI, b) lower ground injection currents, resulting in electrically "cleaner" grounds for the rest of the system and c) minimize source ringing, resulting in more reliable gate switching signals.
- 3) The connection between FETs and the main transformer should be a wide trace or copper region. It should be as short as practical. Since this connection has fast voltage transitions, keeping this connection short will minimize EMI.
- 4) The output capacitor(s) (C_{out}) should be located as close to the load as possible. Fast transient load currents are supplied by C_{out} only. Connections between C_{out} and the load must be short, wide copper areas to minimize inductance and resistance.
- 5) A 0.1 μ F to 1 μ F ceramic capacitor should be directly connected between VCC and GND and a 1 μ F to 4.7 μ F. The SC4812 is best placed over a quiet ground plane area. Avoid pulse currents in the C_{in} and the main switch FET loop flowing in this area. GND should be returned to the ground plane close to the package and close to the ground side of (one of) the VCC supply capacitor(s). Under no circumstances should GND be returned to a ground inside the C_{in} and the main switch FET loop. This can be achieved by making a star connection between the quiet GND planes that the SC4812 will be connected to and the noisy high current GND planes connected to the FETs.
- 6) The feed back connection between the error amplifier and the FB pin should be kept as short as possible, and the GND connections should be to the quiet GND used for the SC4812.
- 7) If an opto-coupler is used for isolation, quiet primary and secondary ground planes should be used. The same precautions should be followed for the primary GND plane as mentioned in item 5. For the secondary GND plane, the GND plane method mentioned in item 4 should be followed.
- 8) All the noise sensitive components such as VCC bypass capacitor, COMP resistor/capacitor network, current sensing circuitry and feedback circuitry should be connected as close as possible to the SC4812. The GND return should be connected to the quiet SC4812 GND plane.
- 9) The connection from the OUT of the SC4812 should be minimized to avoid any stray inductance. If the layout can not be optimized due to constraints, a small Schottky diode may be connected from the OUT pin to the ground directly at the IC. This will clamp excessive negative voltages at the IC.

POWER MANAGEMENT

SC4812 Evaluation Board - Schematics(Isolated Flyback)

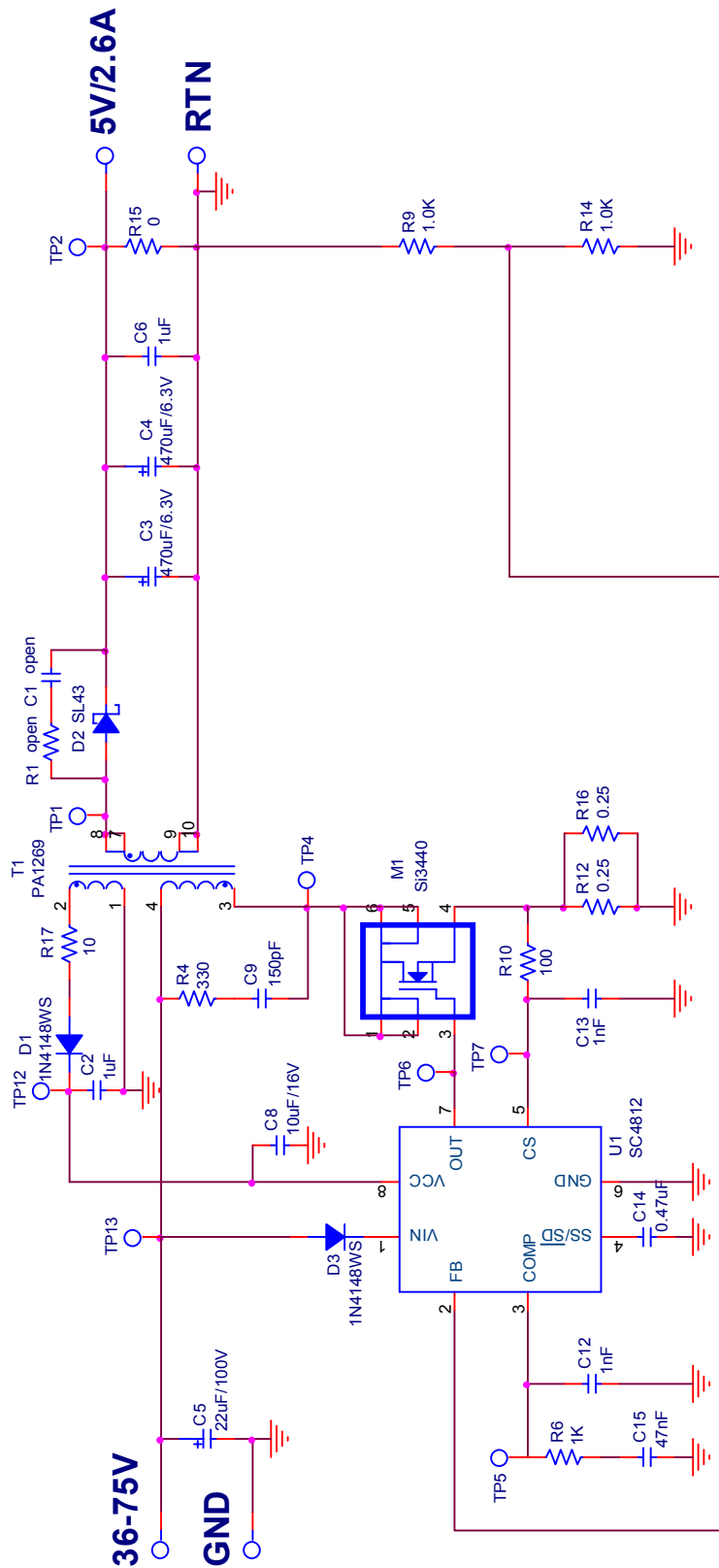


POWER MANAGEMENT
SC4812 Evaluation Board - BOM(Isolated Flyback)

Item	Qty.	Reference	Part/Value	Manufacturer	Manufacturer P.N.
1	2	C2,C6	1uF/6.3V	Kemet	C0805C105M9PAC3810
2	2	C3,C4	470uF/6.3V	Sanyo	6TPB470M
3	1	C5	22uF/100V	Panasonic-ECG	ECA-2AHG220
4	1	C8	10uF/16V	TDK	C3216X7R1C106MF
5	1	C9	150pF	muRata	GRM2165C2A151JA01
6	1	C10	15nF	Panasonic-ECG	ECJ-2VB1H153K
7	1	C12	1nF	Vishay	VJ0805Y102KXXAT
8	1	C13	1000pF	Vishay	VJ0805Y102KXXAT
9	1	C14	0.1uF	Vishay	VJ0805Y104KXXxx
10	1	C25	2.2nF/630V	TDK	C3216X7R2J222K
11	3	D1,D3,D6	1N4148WS	Vishay	1N4148WS-V-GS08
12	1	D2	SL43	Vishay	SL43
13	1	M1	Si3440	Vishay	SI3440DV-T1-E3
14	1	R4	330	Vishay	CRCW0805330RFKEA
15	1	R6	2.4K	Vishay	CRCW08052K40FKEA
16	1	R7	180	Vishay	CRCW0805180RFKEA
17	1	R9	3.32K	Vishay	CRCW08053K32FKEA
18	1	R10	100	Panasonic-ECG	ERJ-6ENF1000V
19	1	R11	10K	Vishay	CRCW080510K0FK
20	2	R12,R16	0.5	Susumu	RL1220S-R50-F
21	1	R14	2.0K	Yageo America	9C08052A2001FKHFT
22	2	R15,R21	0	Vishay	CRCW08050000ZSTA
23	1	R17	10	Yageo America	9C08052A10R0FKHFT
24	1	T1	PA1269	Pulse Eng.	PA1269
25	1	U1	SC4812	Semtech	SC4812STRT
26	1	U2	PS2521L-1	NEC	PS2521L-1
27	1	U3	SC431L	Semtech	SC431LCSK

POWER MANAGEMENT

SC4812 Evaluation Board - Schematics(Non-Isolated Flyback)

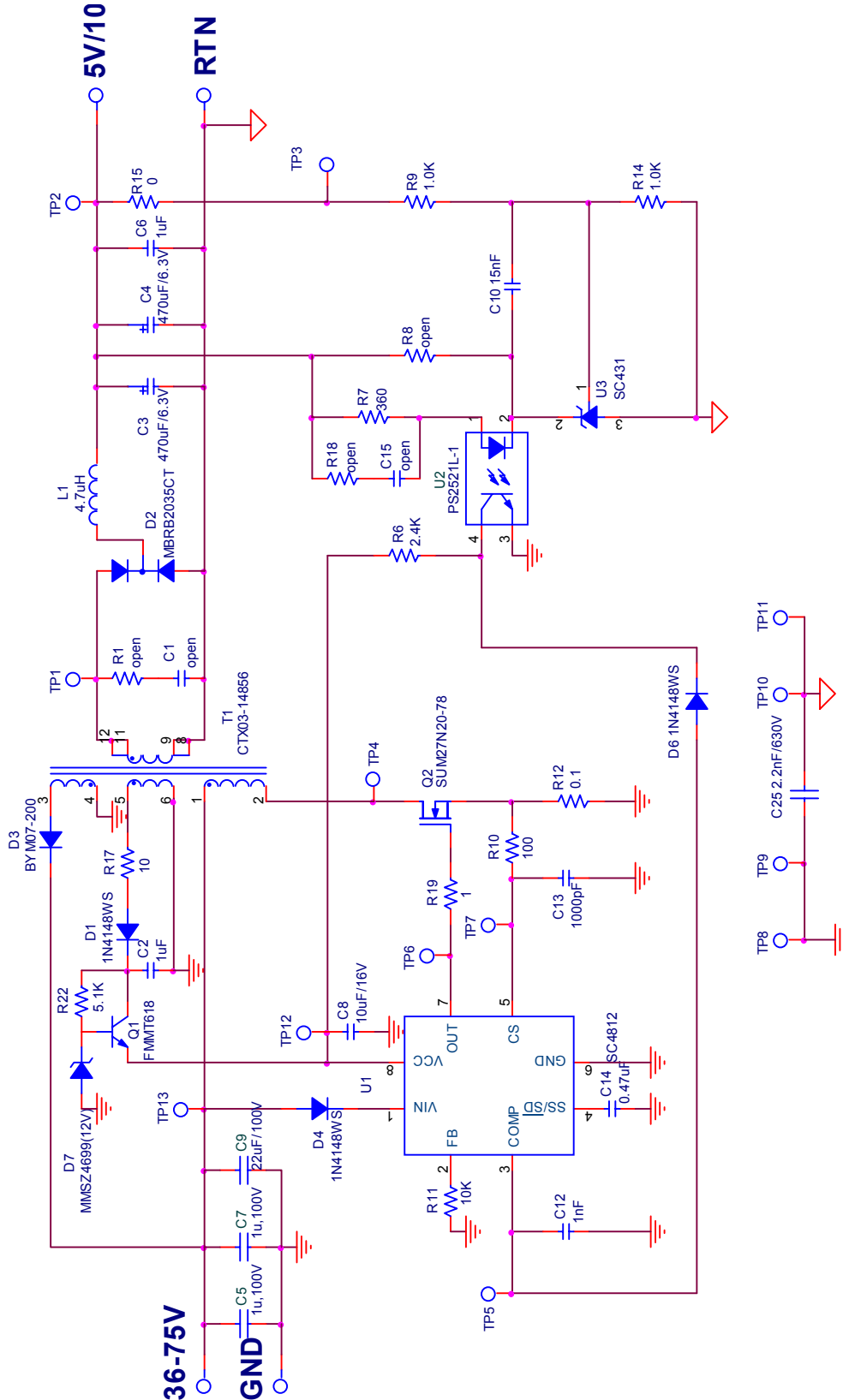


POWER MANAGEMENT
SC4812 Evaluation Board - BOM(Non-Isolated Flyback)

Item	Qty.	Reference	Part/Value	Manufacturer	Manufacturer P.N.
1	2	C2,C6	1uF/16V	Panasonic-ECG	ECJ-2FB1C105K
2	2	C3,C4	470uF/6.3V	Sanyo	6TPB470M
3	1	C5	22uf/100V	Panasonic-ECG	ECA-2AHG220
4	1	C8	10uF/16V	TDK	C3216X7R1C106MT
5	1	C9	150pF/100V	Panasonic-ECG	ECJ-2VC2A151x
6	2	C12, C13	1nF/16V	Vishay	VJ0805Y102KXJPW1BC
7	1	C14	0.1uF/16V	Vishay	VJ0805Y104KXJAC
8	1	C16	47nF/16V	Vishay	VJ0805Y473KXJxx
9	1	D1, D3	1N4148WS	Vishay	1N4148WS-V-GS08
10	2	D2	SL43	Vishay	SL43
11	1	M1	Si3440	Vishay	SI3440DV-T1-E3
12	1	R4	330	Vishay	CRCW0805330RJNEA
13	3	R9, R13, R14	1.0K	Panasonic-ECG	ERJ-6ENF1001V
14	2	R10,R17	100	Vishay	CRCW0805100RFKxx
15	2	R12,R16	0.25	Panasonic-ECG	ERJ-6BQFR24x
16	1	T1	PA1260	Pulse	PA1260
17	1	U1	SC4812	Semtech	SC4812STRT

POWER MANAGEMENT

SC4810B Evaluation Board - Schematics(Forward)

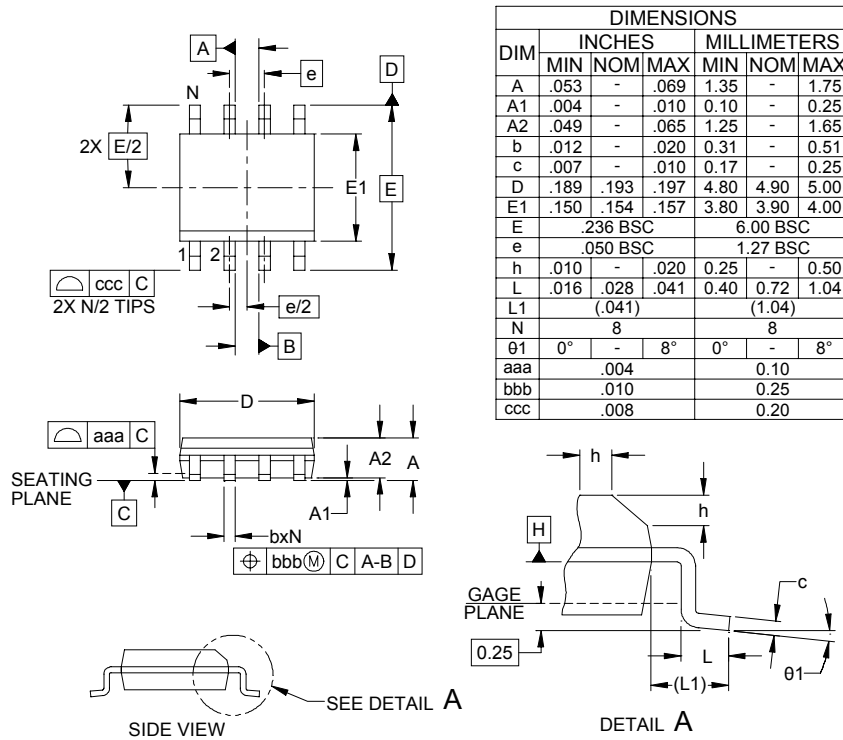


POWER MANAGEMENT
SC4812 Evaluation Board - BOM(Forward)

Item	Qty.	Reference	Part/Value	Manufacturer	Manufacturer P. N.
1	1	C9	22uf/100V	Panasonic-ECG	ECA2AHG220
2	2	C2, C6	1uf/6.3V	Kemet	C0805C105M9PAC3810
3	2	C3, C4	470uf,/6.3V	Sanyo	6TPB470M
4	2	C5, C7	1uf/100V		
5	1	C8	10uf/16V	TDK	C3216X7R1C106MT
6	1	C10	15nf	Panasonic-ECG	ECJ2VB1H153K
7	1	C12	1nf	Vishay	VJ0805Y102KXXAT
8	1	C13	1000pf	Vishay	VJ0805Y102KXXAT
9	1	C14	0.47uf	TDK	C2012X7R1E474K
10	1	C25	2.2nf/630V	TDK	C3216X7R2J222K
11	2	D1, D6	1N4148WS	Vishay	1N4148WS-V-GS08
12	1	D2	MBRB2035CT	Vishay	MBRB2035CT/31
13	1	D3	BYM07-200	Vishay	BYM07-200
14	1	D7	MMSZ4699(12V)	ON Semiconductor	MMSZ4699T1
15	1	L1	4.7uH	Cooper Bussmann	HC2LP-4R7
16	1	Q1	FMMT618	Zetex	FMMT618TA
17	1	Q2	SUM27N20-78	Vishay	SUM27N20-78-E3
18	2	R5, R15	0 ohm	Vishay	CRCW08050000ZSTA
19	1	R6	2.4k ohm	Vishay	CRCW08052K40FKEA
20	1	R7	360 ohm	Panasonic-ECG	ERJ6GEYJ361V
21	2	R9, R14	1.0k ohm	Panasonic-ECG	ERJ6ENF1001V
22	1	R10	100 ohm	Panasonic-ECG	ERJ6ENF1000V
23	1	R11	10k ohm	Vishay	CRCW080510K0FK
24	1	R12	0.1 ohm	Panasonic-ECG	ERJ1TRSFR10x
25	1	R17	10 ohm	Yageo America	9C08052A10R0FKHFT
26	1	R19	1 ohm	Panasonic-ECG	ERJ6GEYJ1R0V
27	1	R22	5.1k ohm	Panasonic-ECG	ERJ6GEYJ512V
28	1	T1	CTX03-14856	Cooper Bussmann	CTX03-14856
29	1	U1	SC4812	Semtech	SC4812STRT
30	1	U2	PS2521L-1	NEC	PS2521L-1-E3-A
31	1	U3	SC431	Semtech	SC431CSK-1.TRT

POWER MANAGEMENT

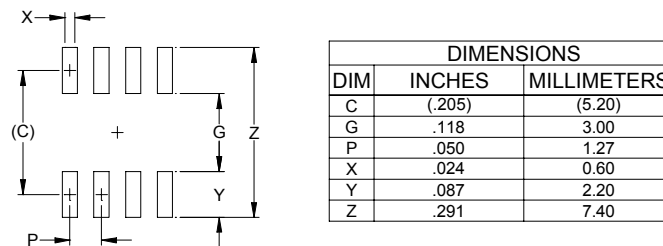
Outline Drawing - SO-8



NOTES:

1. CONTROLLING DIMENSIONS ARE IN MILLIMETERS (ANGLES IN DEGREES).
2. DATUMS **-A-** AND **-B-** TO BE DETERMINED AT DATUM PLANE **-H-**
3. DIMENSIONS "E1" AND "D" DO NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS.
4. REFERENCE JEDEC STD MS-012, VARIATION AA.

Land Pattern - SO-8



NOTES:

1. THIS LAND PATTERN IS FOR REFERENCE PURPOSES ONLY. CONSULT YOUR MANUFACTURING GROUP TO ENSURE YOUR COMPANY'S MANUFACTURING GUIDELINES ARE MET.
2. REFERENCE IPC-SM-782A, RLP NO. 300A.

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