DBB03
Baseband ASIC for Dolphin Chipset
SWRS027B−DECEMBER 2004−REVISED MARCH 2005

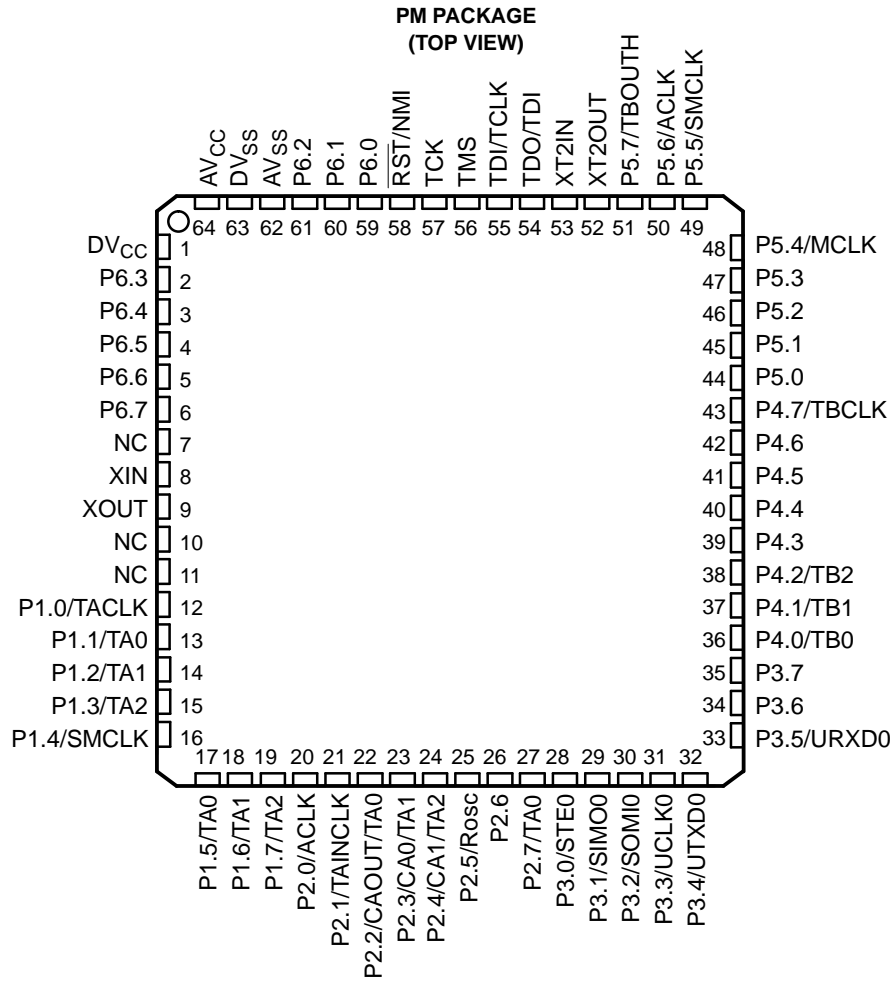TEXAS
INSTRUMENTS
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Figure 1. DBB03 - Baseband ASIC for the Dolphin Chipset

The Wireless UART Dolphin chipset is a true Data-In/RF-out and RF-in/Data-out solution with all aspects of data management and frequency hopping implemented in firmware residing on the DBB03. As illustrated in Figure 1, the DBB03 baseband ASIC contains the complete firmware for Dolphin (PHYsical, MAC and the Data Link layer), while the application layer protocol is handled by the external Host/System Microcontroller.
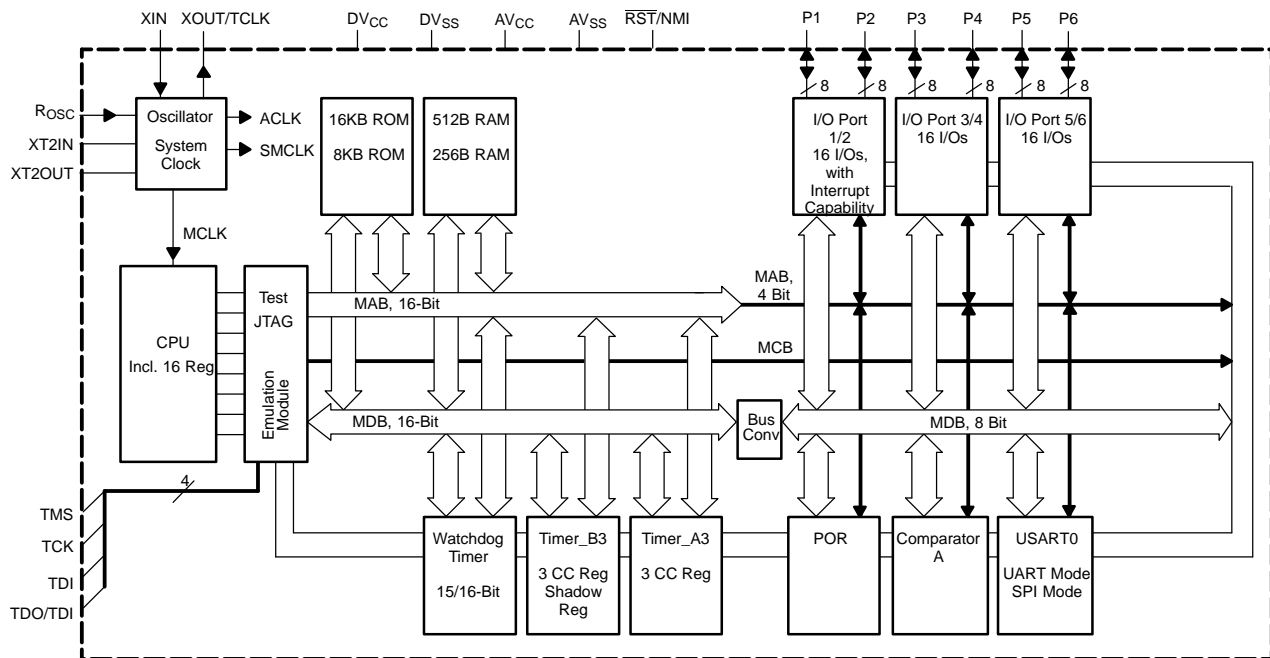
AVAILABLE OPTIONS

T_A	PACKAGE	ORDER NUMBER
-40°C to 85°C	Plastic 64-pin QFP (PM)	DBB03 IPM

PIN DESIGNATION, DBB03 Baseband ASIC

PM PACKAGE
(TOP VIEW)

Top pins (64–49):
AV_{CC}, DV_{SS}, AV_{SS}, P6.2, P6.1, P6.0, $\overline{RST}$/NMI, TCK, TMS, TDI/TCLK, TDO/TDI, XT2IN, XT2OUT, P5.7/TBOUTH, P5.6/ACLK, P5.5/SMCLK

Left side (1–16):
Pin	Name
1	DV_{CC}
2	P6.3
3	P6.4
4	P6.5
5	P6.6
6	P6.7
7	NC
8	XIN
9	XOUT
10	NC
11	NC
12	P1.0/TACLK
13	P1.1/TA0
14	P1.2/TA1
15	P1.3/TA2
16	P1.4/SMCLK

Right side (48–33):
Pin	Name
48	P5.4/MCLK
47	P5.3
46	P5.2
45	P5.1
44	P5.0
43	P4.7/TBCLK
42	P4.6
41	P4.5
40	P4.4
39	P4.3
38	P4.2/TB2
37	P4.1/TB1
36	P4.0/TB0
35	P3.7
34	P3.6
33	P3.5/URXD0

Bottom pins (17–32):
P1.5/TA0, P1.6/TA1, P1.7/TA2, P2.0/ACLK, P2.1/TAINCLK, P2.2/CAOUT/TA0, P2.3/CA0/TA1, P2.4/CA1/TA2, P2.5/Rosc, P2.6, P2.7/TA0, P3.0/STE0, P3.1/SIMO0, P3.2/SOMI0, P3.3/UCLK0, P3.4/UTXD0

NC – No internal connection

FUNCTIONAL BLOCK DIAGRAMS: DBB03

DEVICE INFORMATION

TERMINAL FUNCTIONS

TERMINAL		I/O	DESCRIPTION
NAME	NO.		
AV_{CC}	64		Supply voltage, positive terminal. AV_{CC} and DV_{CC} are internally connected together.
AV_{SS}	64		Supply voltage, negative terminal. AV_{SS} and DV_{SS} are internally connected together.
DV_{CC}	1		Supply voltage, positive terminal. AV_{CC} and DV_{CC} are internally connected together.
DV_{SS}	63		Supply voltage, negative terminal. AV_{SS} and DV_{SS} are internally connected together.
P1.0/TACLK	12	I/O	General-purpose digital I/O pin/Timer_A, clock signal TACLK input
P1.1/TA0	13	I/O	General-purpose digital I/O pin/Timer_A, capture: CCI0A input, compare: Out0 output
P1.2/TA1	14	I/O	General-purpose digital I/O pin/Timer_A, capture: CCI1A input, compare: Out1 output
P1.3/TA2	15	I/O	General-purpose digital I/O pin/Timer_A, capture: CCI2A input, compare: Out2 output
P1.4/SMCLK	16	I/O	General-purpose digital I/O pin/SMCLK signal output
P1.5/TA0	17	I/O	General-purpose digital I/O pin/Timer_A, compare: Out0 output
P1.6/TA1	18	I/O	General-purpose digital I/O pin/Timer_A, compare: Out1 output
P1.7/TA2	19	I/O	General-purpose digital I/O pin/Timer_A, compare: Out2 output
P2.0/ACLK	20	I/O	General-purpose digital I/O pin/ACLK output
P2.1/TAINCLK	21	I/O	General-purpose digital I/O pin/Timer_A, clock signal at INCLK
P2.2/CAOUT/TA0	22	I/O	General-purpose digital I/O pin/Timer_A, capture: CCI0B input/Comparator_A output
P2.3/CA0/TA1	23	I/O	General-purpose digital I/O pin/Timer_A, compare: Out1 output/Comparator_A input
P2.4/CA1/TA2	24	I/O	General-purpose digital I/O pin/Timer_A, compare: Out2 output/Comparator_A input
P2.5/R_{OSC}	25	I/O	General-purpose digital I/O pin/input for external resistor defining the DCO nominal frequency
P2.6	26	I/O	General-purpose digital I/O pin

DEVICE INFORMATION (continued)

TERMINAL FUNCTIONS (continued)

TERMINAL		I/O	DESCRIPTION
NAME	NO.		
P2.7/TA0	27	I/O	General-purpose digital I/O pin/Timer_A, compare: Out0 output
P3.0/STE0	28	I/O	General-purpose digital I/O pin/slave transmit enable - USART0/SPI mode
P3.1/SIMO0	29	I/O	General-purpose digital I/O pin/slave in/master out of USART0/SPI mode
P3.2/SOMI0	30	I/O	General-purpose digital I/O pin/slave out/master in of USART0/SPI mode
P3.3/UCLK0	31	I/O	General-purpose digital I/O pin/external clock input - USART0/UART or SPI mode, clock output - USART0/SPI mode
P3.4/UTXD0	32	I/O	General-purpose digital I/O pin/transmit data out - USART0/UART mode
P3.5/URXD0	33	I/O	General-purpose digital I/O pin/receive data in - USART0/UART mode
P3.6	34	I/O	General-purpose digital I/O pin
P3.7	35	I/O	General-purpose digital I/O pin
P4.0/TB0	36	I/O	General-purpose digital I/O pin/Timer_B, capture: CCI0A/B input, compare: Out0 output
P4.1/TB1	37	I/O	General-purpose digital I/O pin/Timer_B, capture: CCI1A/B input, compare: Out1 output
P4.2/TB2	38	I/O	General-purpose digital I/O pin/Timer_B, capture: CCI2A/B input, compare: Out2 output
P4.3	39	I/O	General-purpose digital I/O pin
P4.4	40	I/O	General-purpose digital I/O pin
P4.5	41	I/O	General-purpose digital I/O pin
P4.6	42	I/O	General-purpose digital I/O pin
P4.7/TBCLK	43	I/O	General-purpose digital I/O pin/Timer_B, clock signal TBCLK input
P5.0	44	I/O	General-purpose digital I/O pin
P5.1	45	I/O	General-purpose digital I/O pin
P5.2	46	I/O	General-purpose digital I/O pin
P5.3	47	I/O	General-purpose digital I/O pin
P5.4/MCLK	48	I/O	General-purpose digital I/O pin/main system clock MCLK output
P5.5/SMCLK	49	I/O	General-purpose digital I/O pin/submain system clock SMCLK output
P5.6/ACLK	50	I/O	General-purpose digital I/O pin/auxiliary clock ACLK output
P5.7/TBOUTH	51	I/O	General-purpose digital I/O pin/switch all PWM digital output ports to high impedance - Timer_B7 TB0 to TB2
P6.0	59	I/O	General-purpose digital I/O pin
P6.1	60	I/O	General-purpose digital I/O pin
P6.2	61	I/O	General-purpose digital I/O pin
P6.3	2	I/O	General-purpose digital I/O pin
P6.4	3	I/O	General-purpose digital I/O pin
P6.5	4	I/O	General-purpose digital I/O pin
P6.6	5	I/O	General-purpose digital I/O pin
P6.7	6	I/O	General-purpose digital I/O pin
$\overline{RST}$/NMI	58	I	Reset input, nonmaskable interrupt input port
TCK	57	I	Test clock. TCK is the clock input port for device programming test.
TDI/TCLK	55	I	Test data input or test clock input. TDI is used as a data input port. The device protection fuse is connected to TDI.
TDO/TDI	54	I/O	Test data output port. TDO/TDI data output
TMS	56	I	Test mode select. TMS is used as an input port for device test.
NC	7, 10, 11		No internal connection
XIN	8	I	Input port for crystal oscillator XT1. Standard or watch crystals can be connected.
XOUT	9	O	Output terminal of crystal oscillator XT1
XT2IN	53	I	Input port for crystal oscillator XT2. Only standard crystals can be connected.
XT2OUT	52	O	Output terminal of crystal oscillator XT2

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)	Op Temp (°C)	Top-Side Markings (4)	Samples
DBB03IPM	NRND	LQFP	PM	64		TBD	Call TI	Call TI	-40 to 85	DBB03	
DBB03IPMR	NRND	LQFP	PM	64		TBD	Call TI	Call TI	-40 to 85		

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
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(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.
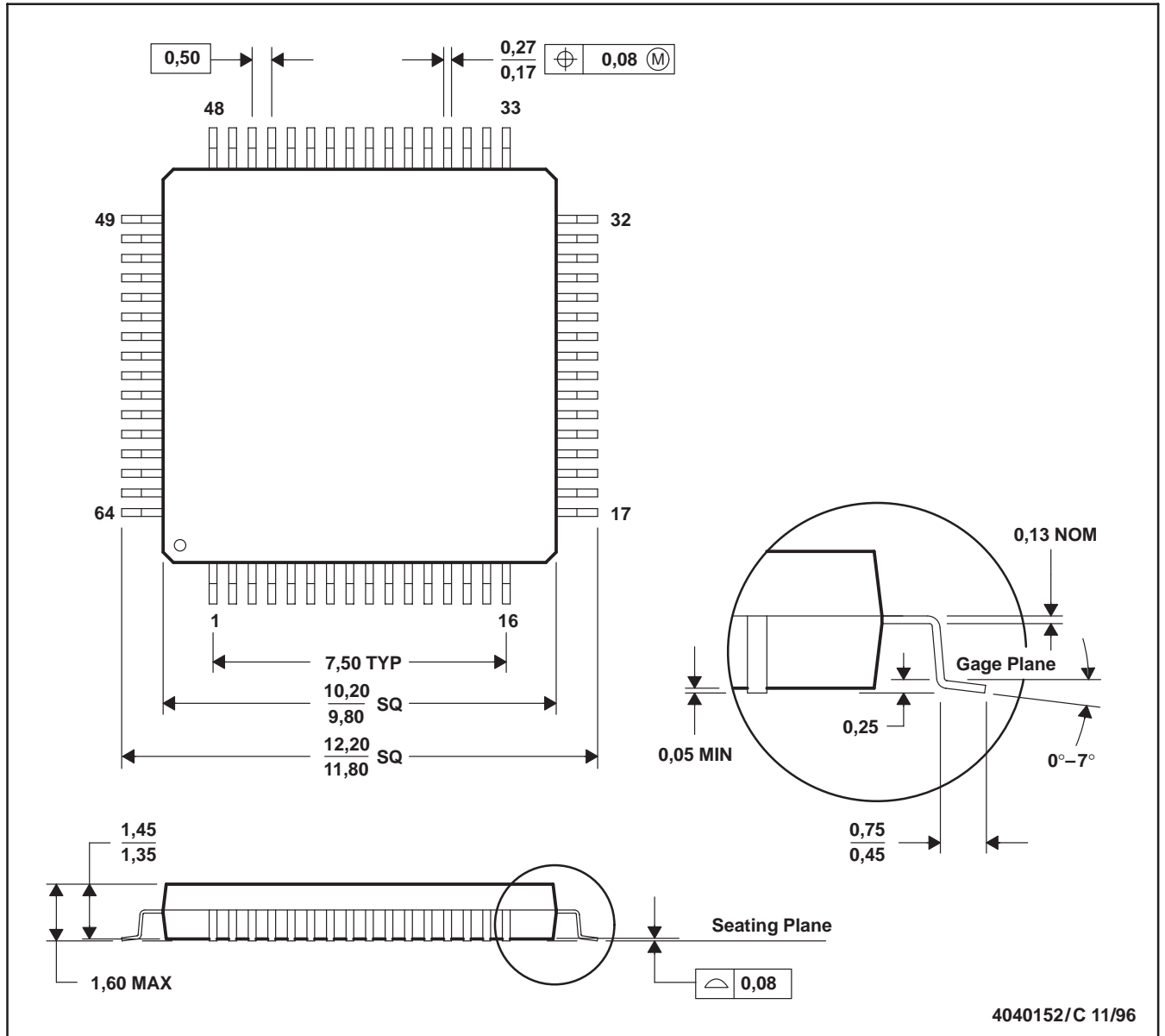
(4) Multiple Top-Side Markings will be inside parentheses. Only one Top-Side Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Top-Side Marking for that device.

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PM (S-PQFP-G64) PLASTIC QUAD FLATPACK

0,50

$\frac{0,27}{0,17}$ ⊕ 0,08 Ⓜ

48   33

49   32

0,13 NOM

64   17

Gage Plane

1   16

0,05 MIN   0,25   0°–7°

7,50 TYP

$\frac{10,20}{9,80}$ SQ

$\frac{12,20}{11,80}$ SQ

$\frac{0,75}{0,45}$

$\frac{1,45}{1,35}$

Seating Plane

1,60 MAX   ◁ 0,08

4040152/C 11/96

NOTES: A. All linear dimensions are in millimeters.
   B. This drawing is subject to change without notice.
   C. Falls within JEDEC MS-026
   D. May also be thermally enhanced plastic with leads connected to the die pads.

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