## RATINGS AND CHARACTERISTICS CURVES

($T_A$=25°C unless otherwise noted)

Fig. 1 Admissible Power Dissipation Curve

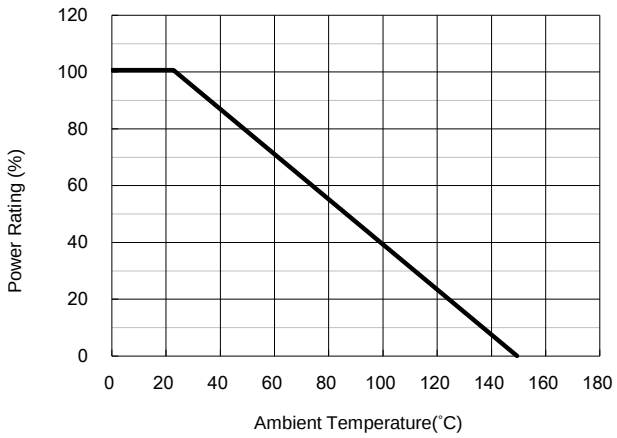



Fig. 2 Typical Junction Capacitance

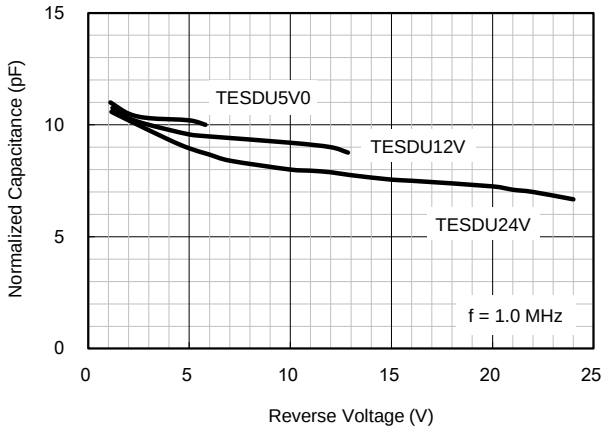
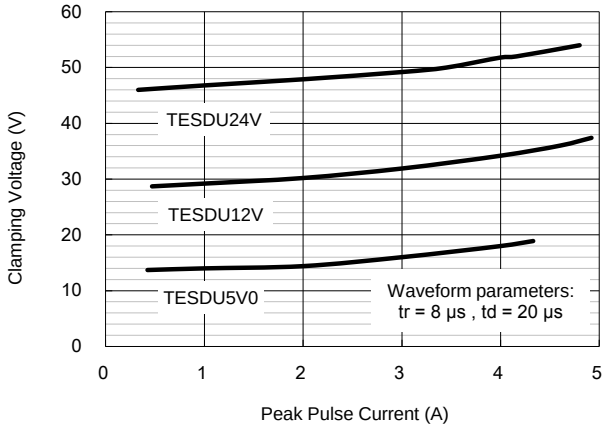



Fig. 3 Clamping Voltage VS. Peak Pulse Current



| ORDERING INFORMATION | | | | |
|---|---|---|---|---|
| **PART NO.** | **PACKING CODE** | **PACKING CODE SUFFIX** | **PACKAGE** | **PACKING** |
| TESDUxxx (Note1, 2) | RG | G | 0603 | 4,000 / 7" Reel |

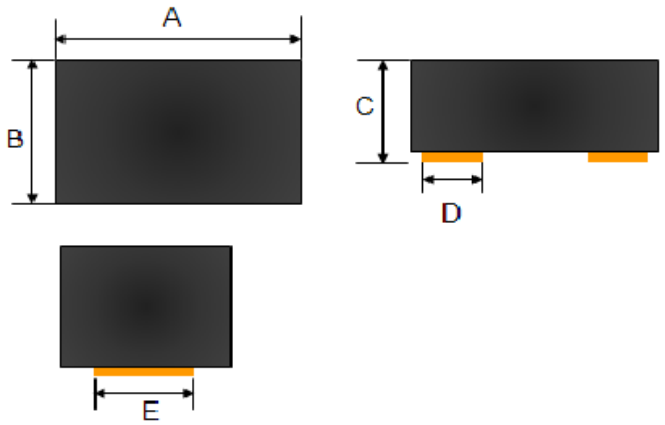
Note 1: "xxx" defines voltage from 5V (TESDU5V0) to 24V (TESDU24V)

Note 2: Whole series with green compound

| EXAMPLE | | | | |
|---|---|---|---|---|
| **EXAMPLE P/N** | **PART NO.** | **PACKING CODE** | **PACKING CODE SUFFIX** | **DESCRIPTION** |
| TESDU5V0 RGG | TESDU5V0 | RG | G | Green compound |

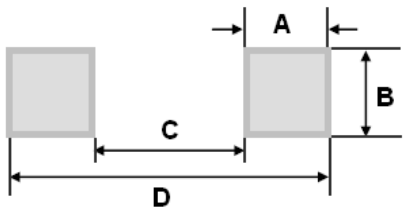
## PACKAGE OUTLINE DIMENSIONS

**0603**




| DIM. | Unit (mm) | | Unit (inch) | |
|---|---|---|---|---|
| | **Min** | **Max** | **Min** | **Max** |
| A | 1.60 | 1.80 | 0.063 | 0.071 |
| B | 0.80 | 1.00 | 0.031 | 0.039 |
| C | 0.70 | 0.85 | 0.028 | 0.033 |
| D | 0.45 (Typ.) | | 0.018 (Typ.) | |
| E | 0.70 (Typ.) | | 0.028 (Typ.) | |

## SUGGEST PAD LAYOUT




| DIM. | Unit (mm) | Unit (inch) |
|---|---|---|
| | **Typ.** | **Typ.** |
| A | 0.60 | 0.024 |
| B | 1.00 | 0.039 |
| C | 0.65 | 0.026 |
| D | 1.85 | 0.073 |

Note: The suggested land pattern dimensions have been provided for reference only, as actual pad layouts may vary depending on application.

## MARKING

| Part NO. | Marking |
|---|---|
| TESDU5V0 | E05 |
| TESDU12V | E12 |
| TESDU24V | E24 |

## APPLICATIONS INFORMATION

◇ Designed to protect one data, I/O, or power supply line
◇ Designed to protect sensitive electronics from damage or latch-up due to ESD
◇ Designed to replace multilayer varistors (MLVs) in portable applications
◇ Features large cross-sectional area junctions for conducting high transient currents
◇ Offers superior electrical characteristics such as lower clamping voltage and no device degradation when compared to MLVs
◇ The combination of small size and high ESD surge capability makes them ideal for use in portable applications

## CIRCUIT BOARD LAYOUT RECOMMENDATIONS

Good circuit board layout is critical for the suppression of ESD induced transients
◇ Place the ESD Protection Diode near the input terminals or connectors to restrict transient coupling
◇ Minimize the path length between the ESD Protection Diode and the protected line
◇ Minimize all conductive loops including power and ground loops
◇ The ESD transient return path to ground should be kept as short as possible
◇ Never run critical signals near board edges
◇ Use ground planes whenever possible

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