Dual, Audio, Log Taper Digital Potentiometers

ABSOLUTE MAXIMUM RATINGS

V_{DD}, V_{LOGIC}, $\overline{CS}$, SCLK, DIN to GND .....-0.3V to +6V
H_, L_, and W_ to GND .....-0.3V to (V_{DD} + 0.3V)
DOUT to GND.....-0.3V to (V_{DD} + 0.3V)
AGND to GND .....-0.3V to +0.3V
Input and Output Latchup Immunity.....±200mA
Maximum Continuous Current into H_, L_, and W_.....±500µA

Continuous Power Dissipation (T_A = +70°C)
16-Pin QSOP (derate 8.3mW/°C above +70°C).....666.7mW
16-Pin QFN (derate 18.5mW/°C above +70°C) 1481mW
Operating Temperature Range .....-40°C to +85°C
Storage Temperature Range .....-60°C to +150°C
Maximum Junction Temperature .....+150°C
Lead Temperature (soldering, 10s) .....+300°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

(V_{DD} = +2.7V to +3.6V (MAX5408/MAX5409), V_{DD} = +4.5V to +5.5V (MAX5410/MAX5411), $V_{H\_}$ = V_{DD}, $V_{L\_}$ = 0, T_A = T_{MIN} to T_{MAX}. Typical values are at T_A = +25°C, unless otherwise specified.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
End-to-End Resistance			7	10	13	kΩ
Maximum Bandwidth		(Note 1) $C_{W\_}$ = 50pF	100			kHz
Absolute Tolerance				±0.25		dB
Tap-to-Tap Tolerance				±0.1		dB
Total Harmonic Distortion + Noise	THD+N	V_{IN} = $1V_{RMS}$, f = 1kHz, tap = -6dB		0.002		%
Channel Isolation				-100		dB
Interchannel Matching		f = 20Hz to 20kHz, tap = -6dB		±0.5		dB
Mute Attenuation				-90		dB
Power-Supply Rejection Ratio	PSRR			-80		dB
Wiper Resistance	R_W			1000	1700	Ω
Wiper Capacitance	C_W			10		pF
Digital Clock Feedthrough		f_{SCLK} = 20Hz to 20kHz, tap = -6dB		-90		dB
End-to-End Resistance Temperature Coefficient				35		ppm/°C
Ratiometric Resistance Temperature Coefficient				5		ppm/°C
DIGITAL INPUTS (V_{LOGIC} > 4.5V)						
Input High Voltage	V_{IH}		2.4			V
Input Low Voltage	V_{IL}				0.8	V
Input Leakage Current					±1	µA
Input Capacitance				5		pF
DIGITAL INPUTS (V_{LOGIC} < 4.5V)						
Input High Voltage	V_{IH}		0.7 x V_{LOGIC}			V
Input Low Voltage	V_{IL}				0.3 x V_{LOGIC}	V
Input Leakage Current					±1	µA
Input Capacitance				5		pF

ELECTRICAL CHARACTERISTICS (continued)

(V_{DD} = +2.7V to +3.6V (MAX5408/MAX5409), V_{DD} = +4.5V to +5.5V (MAX5410/MAX5411), $V_{H\_}$ = V_{DD}, $V_{L\_}$ = 0, T_A = T_{MIN} to T_{MAX}. Typical values are at T_A = +25°C, unless otherwise specified.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
DIGITAL OUTPUT						
Output High Voltage	V_{OH}	I_{SOURCE} = 0.5mA	V_{LOGIC} - 0.5			V
Output Low Voltage	V_{OL}	I_{SINK} = 2mA			0.4	V
TIMING CHARACTERISTICS (Figure 1)						
SCLK Clock Period	t_{CP}		100			ns
SCLK Pulse Width High	t_{CH}		40			ns
SCLK Pulse Width Low	t_{CL}		40			ns
$\overline{CS}$ Fall to SCLK Rise Setup Time	t_{CSS}		40			ns
SCLK Rise to $\overline{CS}$ Rise Hold Time	t_{CSH}		0			ns
DIN Setup Time	t_{DS}		40			ns
DIN Hold Time	t_{DH}		0			ns
SCLK Fall to DOUT Valid Propagation Delay	t_{DO}	C_{LOAD} = 200pF			80	ns
$\overline{CS}$ Rise to SCLK Rise Hold Time	t_{CS1}		40			ns
$\overline{CS}$ Pulse Width High	t_{CSW}		100			ns
Wiper Settling Time	t_{IW}	Zero-crossing detect disabled		1		µs
POWER SUPPLIES						
Supply Voltage	V_{DD}	MAX5408/MAX5409	2.7		3.6	V
		MAX5410/MAX5411	4.5		5.5	
Active Supply Current	I_{DD}	f_{SCLK} = 2MHz (Note 2)			100	µA
Standby Supply Current		(Note 3)		0.2	10	
Logic Supply Voltage	V_{LOGIC}		2.7		5.5	V
Logic Active Supply Current	I_{LOGIC}	f_{SCLK} = 2MHz, DOUT = floating (Note 2)			120	µA
Logic Standby Supply Current		DOUT = floating (Note 3)		0.5	10	

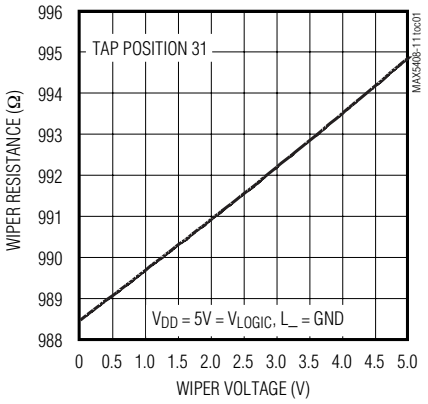
Note 1: Guaranteed by design, not production tested.
Note 2: Supply current measured while changing wiper position with zero crossing enabled.
Note 3: Supply current measured while wiper position is fixed.

Dual, Audio, Log Taper Digital Potentiometers

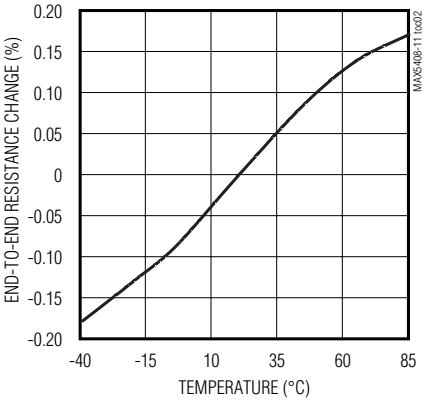
Typical Operating Characteristics

(V_{DD} = +3V (MAX5408/MAX5409), V_{DD} = +5V (MAX5410/MAX5411), DOUT = floating)

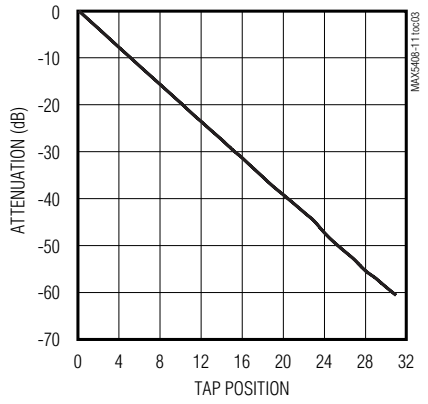
WIPER RESISTANCE vs. WIPER VOLTAGE



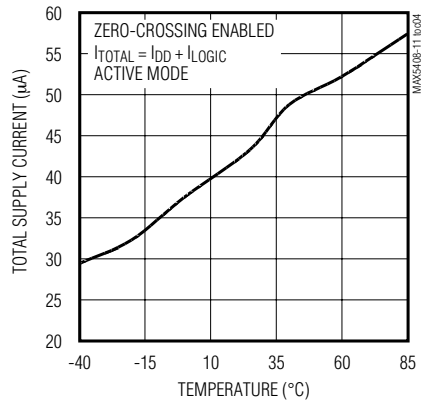
END-TO-END RESISTANCE % CHANGE vs. TEMPERATURE



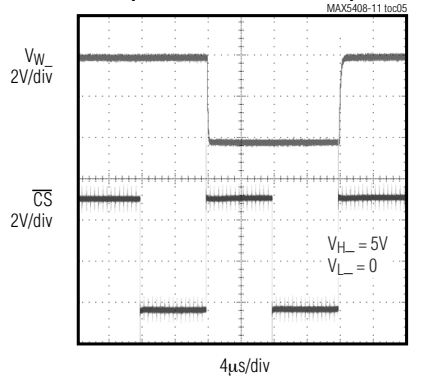
ATTENUATION vs. TAP POSITION



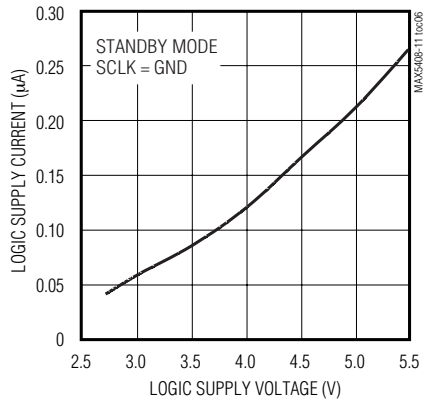
TOTAL SUPPLY CURRENT vs. TEMPERATURE



TAP-TO-TAP SWITCHING TRANSIENT (ZERO-CROSSING DISABLE)



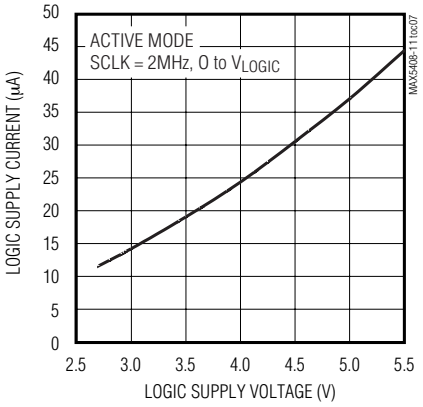
LOGIC CURRENT vs. LOGIC VOLTAGE



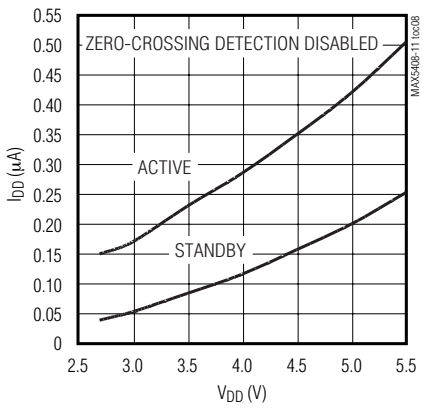
Typical Operating Characteristics (continued)

(V_{DD} = +3V (MAX5408/MAX5409), V_{DD} = +5V (MAX5410/MAX5411), DOUT = floating)

LOGIC CURRENT vs. LOGIC VOLTAGE



SUPPLY CURRENT vs. SUPPLY VOLTAGE



Pin Description

PIN				NAME	FUNCTION
MAX5408/ MAX5410 (QFN)	MAX5408/ MAX5410 (QSOP)	MAX5409/ MAX5411 (QFN)	MAX5409/ MAX5411 (QSOP)		
1	3	1	3	SCLK	Serial Clock Input
2	4	2	4	$\overline{CS}$	Chip-Select Input
3	5	3	5	H0	High Terminal of Resistor 0
4	6	4	6	L0	Low Terminal of Resistor 0
5	7	5	7	W0A	Wiper Terminal A of Resistor 0
—	—	6	8	W0B	Wiper Terminal B of Resistor 0
—	—	7	9	W1B	Wiper Terminal B of Resistor 1
8	10	8	10	W1A	Wiper Terminal A of Resistor 1
9	11	9	11	L1	Low Terminal of Resistor 1
10	12	10	12	H1	High Terminal of Resistor 1
11	13	11	13	AGND	Analog Ground
12	14	12	14	GND	Ground
13	15	13	15	V_{LOGIC}	Digital Logic Power Supply
14	16	14	16	V_{DD}	Analog Power Supply
15	1	15	1	DOUT	Serial Data Output
16	2	16	2	DIN	Serial Data Input
6, 7	8, 9	—	—	N.C.	No Connection. Not internally connected.

Table 1. Serial Interface Programming Commands for MAX5408/MAX5410

8-BIT SERIAL WORD				FUNCTION
A0	A1	A2	D4–D0	
0	0	0	5-bit DAC data	Set position of wiper W0A
0	0	1	5-bit DAC data	No change
0	1	0	5-bit DAC data	Set position of wiper W1A
0	1	1	5-bit DAC data	No change
1	0	0	4-bit mute data, D0 = “don’t care”	Data for mute register (see Table 3)
1	0	1	4-bit zero-crossing detection data, D0 = “don’t care”	Data for zero-crossing detection register (see Table 5)
1	1	0	00000	Readback contents of wiper register for W0A at DOUT
1	1	0	00001	No change
1	1	0	00010	Readback contents of wiper register for W1A at DOUT
1	1	0	00011	No change
1	1	0	00100	Readback contents of mute register at DOUT
1	1	0	00101	Readback contents of zero-crossing detection register at DOUT
1	1	1	D4 = 0, D3–D0 = “don’t care”	Immediate update then analog power-down when zero crossing is enabled. No effect when zero crossing is disabled.

Detailed Description

Digital Serial Interface

An SPI-compatible serial interface controls the MAX5408–MAX5411. The input word to the device is eight bits long, composed of three address bits (A0, A1, and A2), followed by five data bits, with MSB first (see Tables 1 and 2). The first three address bits set the value of internal registers. The five data bits control the wiper position. For certain commands, some of the five data bits are “don’t cares”, but must be sent to the device.

The serial data is listed in Tables 1 and 2.

The control code determines:

- Potentiometer to update or register to set.
- Data for mute register (Tables 3 and 4).
- Data for zero-crossing detection register (Tables 5 and 6).

The data bits control the position of the wiper (Table 7). A logic low on the chip-select input ($\overline{CS}$) enables the device’s serial interface. A logic high on $\overline{CS}$ disables the interface control circuitry. See Figure 1 for serial-interface timing description.

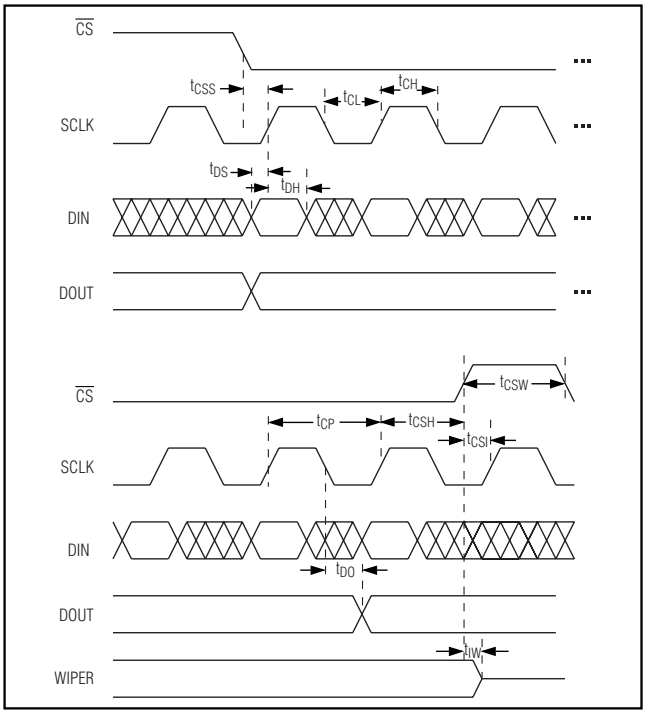


Figure 1. Serial Timing Diagram

Table 2. Serial Interface Programming Commands for MAX5409/MAX5411

8-BIT SERIAL WORD				FUNCTION
A0	A1	A2	D4–D0	
0	0	0	5-bit DAC data	Set position of wiper W0A
0	0	1	5-bit DAC data	Set position of wiper W0B
0	1	0	5-bit DAC data	Set position of wiper W1A
0	1	1	5-bit DAC data	Set position of wiper W1B
1	0	0	4-bit mute data, D0 = “don’t care”	Data for mute register (see Table 4)
1	0	1	4-bit zero-crossing detection data, D0 = “don’t care”	Data for zero-crossing detection register (see Table 6)
1	1	0	00000	Readback contents of wiper register for W0A at DOUT
1	1	0	00001	Readback contents of wiper register for W0B at DOUT
1	1	0	00010	Readback contents of wiper register for W1A at DOUT
1	1	0	00011	Readback contents of wiper register for W1B at DOUT
1	1	0	00100	Readback contents of mute register at DOUT
1	1	0	00101	Readback contents of zero-crossing detection register at DOUT
1	1	1	D4 = 0, D3–D0 = “don’t care”	Analog power-down
1	1	1	D4 = 1, D3–D0 = “don’t care”	Analog power-up

Table 3. Mute Register Bit Definitions for MAX5408/MAX5410

DATA BIT	VALUE	FUNCTION
D4	0	Set wiper W0A to preprogrammed value (-62dB on power-up)
	1	Set wiper W0A to mute (-90dB)
D3	“don’t care”	No change
D2	0	Set wiper W1A to preprogrammed value (-62dB on power-up)
	1	Set wiper W1A to mute (-90dB)
D1	“don’t care”	No change
D0	“don’t care”	No change

Table 4. Mute Register Bit Definitions for MAX5409/MAX5411

DATA BIT	VALUE	FUNCTION
D4	0	Set wiper W0A to preprogrammed value (-62dB on power-up)
	1	Set wiper W0A to mute (-90dB)
D3	0	Set wiper W0B to preprogrammed value (-62dB on power-up)
	1	Set wiper W0B to mute (-90dB)
D2	0	Set wiper W1A to preprogrammed value (-62dB on power-up)
	1	Set wiper W1A to mute (-90dB)
D1	0	Set wiper W1B to preprogrammed value (-62dB on power-up)
	1	Set wiper W1B to mute (-90dB)
D0	“don’t care”	No change

Table 5. Zero-Crossing Detection Register Bit Definitions for MAX5408/MAX5410

DATA BIT	VALUE	FUNCTION
D4	0	Disable wiper W0A zero-crossing detection circuit
	1	Enable wiper W0A zero-crossing detection circuit
D3	"don't care"	No change
D2	0	Disable wiper W1A zero-crossing detection circuit
	1	Enable wiper W1A zero-crossing detection circuit
D1	"don't care"	No change
D0	"don't care"	No change

Table 6. Zero-Crossing Detection Register Bit Definitions for MAX5409/MAX5411

DATA BIT	VALUE	FUNCTION
D4	0	Disable wiper W0A zero-crossing detection circuit
	1	Enable wiper W0A zero-crossing detection circuit
D3	0	Disable wiper W0B zero-crossing detection circuit
	1	Enable wiper W0B zero-crossing detection circuit
D2	0	Disable wiper W1A zero-crossing detection circuit
	1	Enable wiper W1A zero-crossing detection circuit
D1	0	Disable wiper W1B zero-crossing detection circuit
	1	Enable wiper W1B zero-crossing detection circuit
D0	"don't care"	No change

Table 7. Attenuation and Wiper Position

POSITION	OUTPUT LEVEL (dB)
0	0
1	-2
2	-4
3	-6
4	-8
⋮	⋮
30	-60
31	-62
MUTE	<-90

The digital output, DOUT, lags the digital input signal, DIN by 8.5 clock cycles. Force $\overline{CS}$ high to disable DOUT, placing DOUT in three-state mode. Force $\overline{CS}$ low to enable DOUT and disable three-state mode.

Force $\overline{CS}$ high, after a word has been written to the MAX5408–MAX5411 to make a readback request. The next $\overline{CS}$ low period writes the requested data to DOUT.

A readback request overwrites any previous data in the shift register. Note that the data appears at DOUT in the order: A0, A1, A2, D4, D3, D2, D1, D0. A0 will be available after the first high-to-low transition of SCLK when $\overline{CS}$ is low. The input continues to load the shift register while data is being read out of the MAX5408–MAX5411. The input data appears at DOUT 8.5 clock cycles later. A $\overline{CS}$ transition from low-to-high latches the input data. For any control byte, the state of SCLK must be the same for both $\overline{CS}$ low-to-high transitions and $\overline{CS}$ high-to-low transitions in order to preserve the data at DOUT while $\overline{CS}$ transitions. For proper operation, ensure that the input data remains valid on both the SCLK rising and falling edges when daisy chaining multiple devices.

Zero-Crossing Detection

The zero-crossing detection register enables the zero-crossing detect feature. The zero-crossing detect feature reduces the audible noise ("clicks and pops") that result from wiper transitions. The wiper changes position only when the voltage at L_ is the same as the voltage at H_. Each wiper has a zero-crossing and timeout

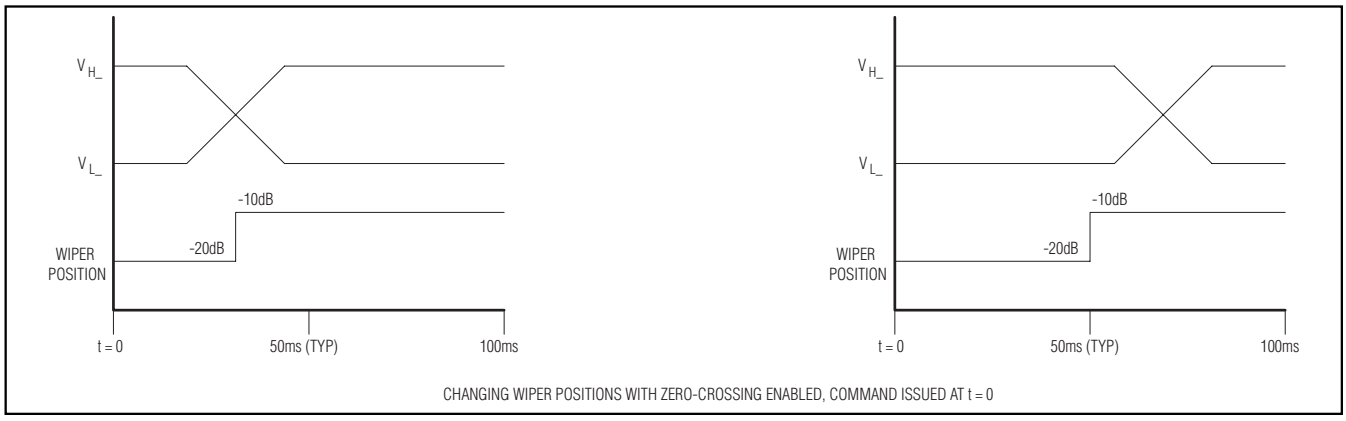


Figure 2. Zero-Crossing Timing Diagram

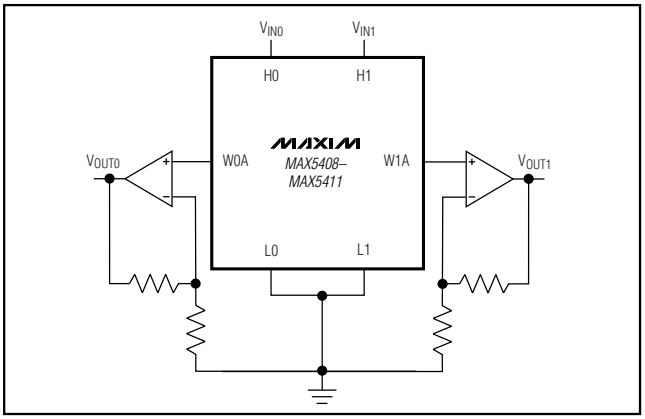


Figure 3. Attenuation Control

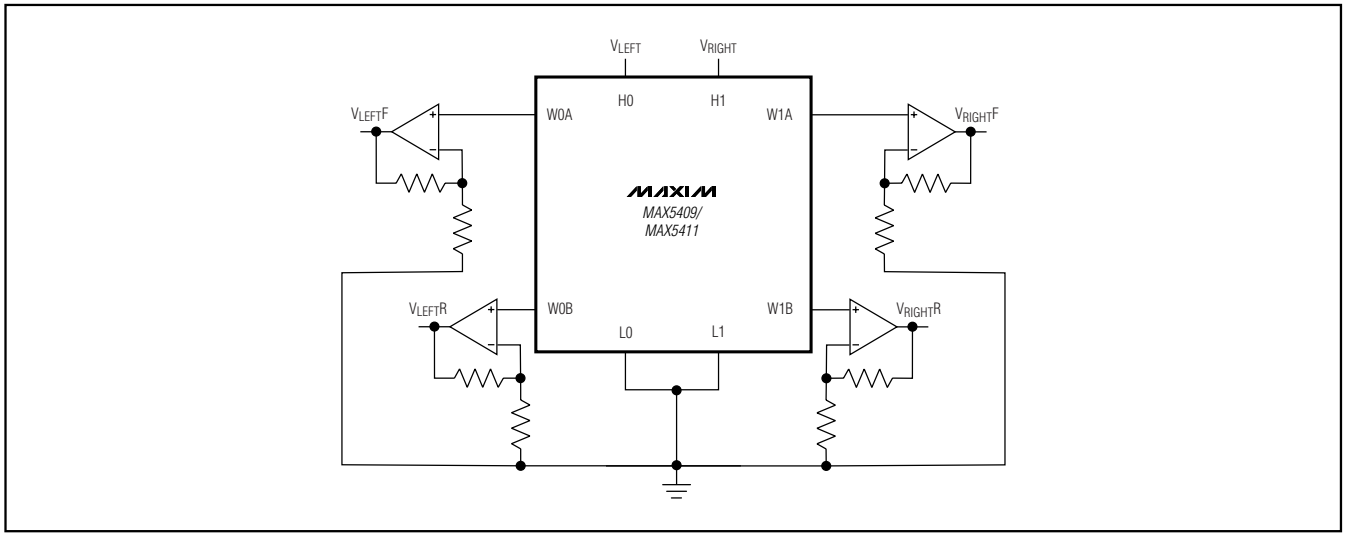


Figure 4. Stereo Volume Control with Front and Rear Fade

Dual, Audio, Log Taper Digital Potentiometers

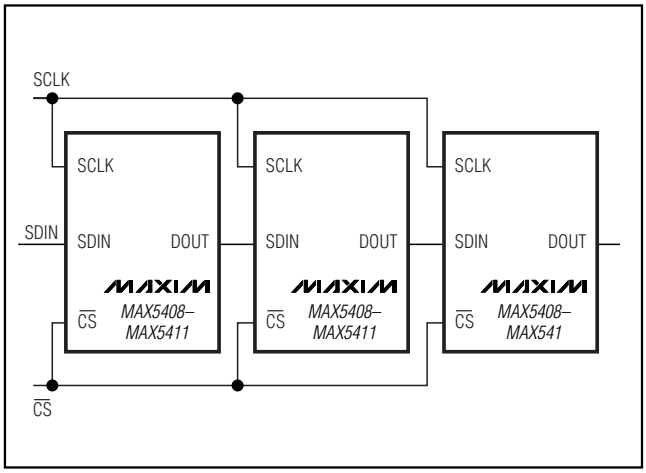


Figure 5. Daisy-Chaining of Serial Interfaces

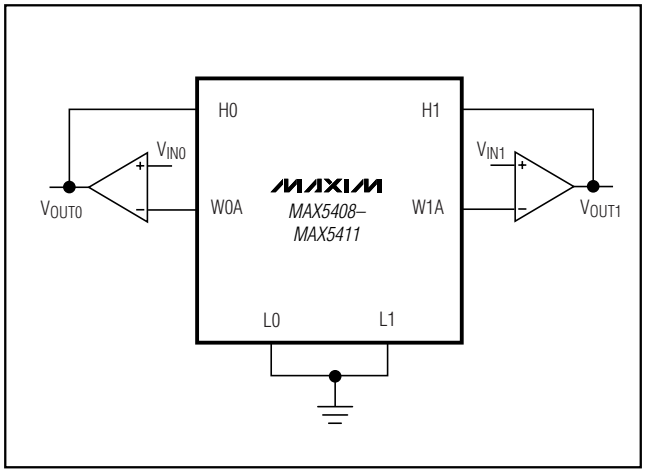


Figure 6. Gain Control

circuit (see Figure 2). With zero-crossing enabled, the MAX5408–MAX5411 change wiper position after 50ms or when zero crossing is detected.

Power-On Reset

The power-on reset (POR) feature sets all the wipers to the maximum attenuation (tap position 31, -62dB) at power-up. If either V_{DD} or V_{LOGIC} is zero volts, a power-on reset intiates when one of the supplies is brought back to the operating voltage.

Mute Function

When mute is enabled, the wipers go to -90dB attenuation. When mute is disabled, the wiper returns to its position before mute was enabled. All wipers can be muted simultaneously or independently.

Applications Information

Attenuation Control

Figure 3 shows the application of an attenuation control. The op amps are connected in a follower configuration with a fixed gain. The digitally controlled potentiometer attenuates the input signal.

Stereo Volume Control

Figure 4 shows the application of stereo volume control using MAX5409/MAX5411. The op amps are connected in a follower configuration with fixed gain. The digitally controlled potentiometer attenuates the input signals. The second wiper of each potentiometer controls the signal amplitude at the rear set of speakers.

Daisy-Chaining

Figure 5 shows an application daisy-chaining the serial-interfaces of the MAX5408–MAX5411. A single-write command updates multiple devices from a single digital port in this configuration (see *Digital Serial Interface* section).

Gain Control

Figure 6 shows the application of a gain control. **Note:** Muting the potentiometer creates unpredictable behavior at the output of the op amp, and may seriously degrade the performance of the op amp.

Ordering Information (continued)

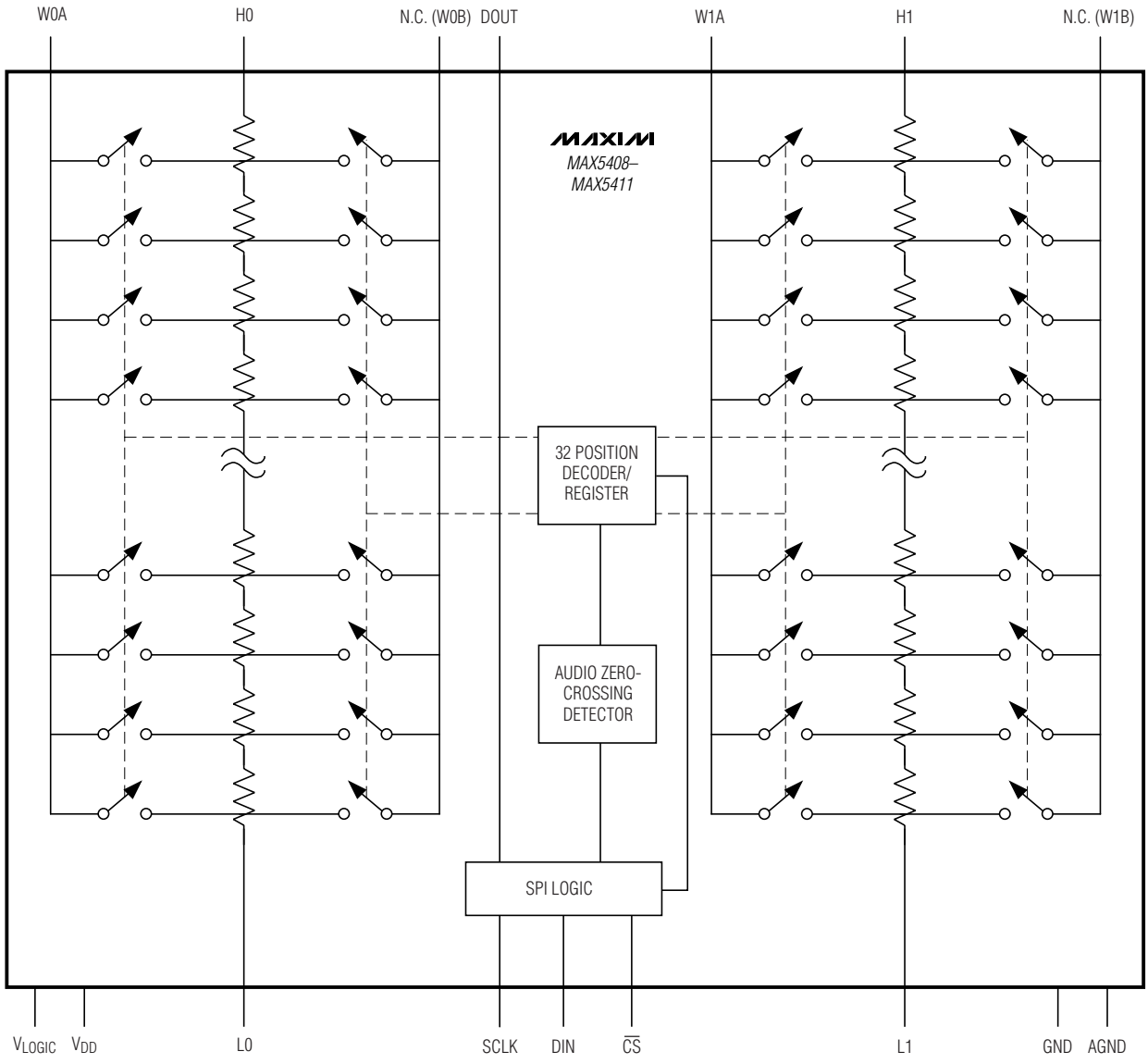
PART	TEMP RANGE	PIN-PACKAGE	WIPERS PER RESISTOR
MAX5409ETE	-40°C to +85°C	16 Thin QFN	2
MAX5410EEE	-40°C to +85°C	16 QSOP	1
MAX5410ETE	-40°C to +85°C	16 Thin QFN	1
MAX5411EEE	-40°C to +85°C	16 QSOP	2
MAX5411ETE	-40°C to +85°C	16 Thin QFN	2

Chip Information

TRANSISTOR COUNT: 12,875

PROCESS: BiCMOS

Functional Diagram

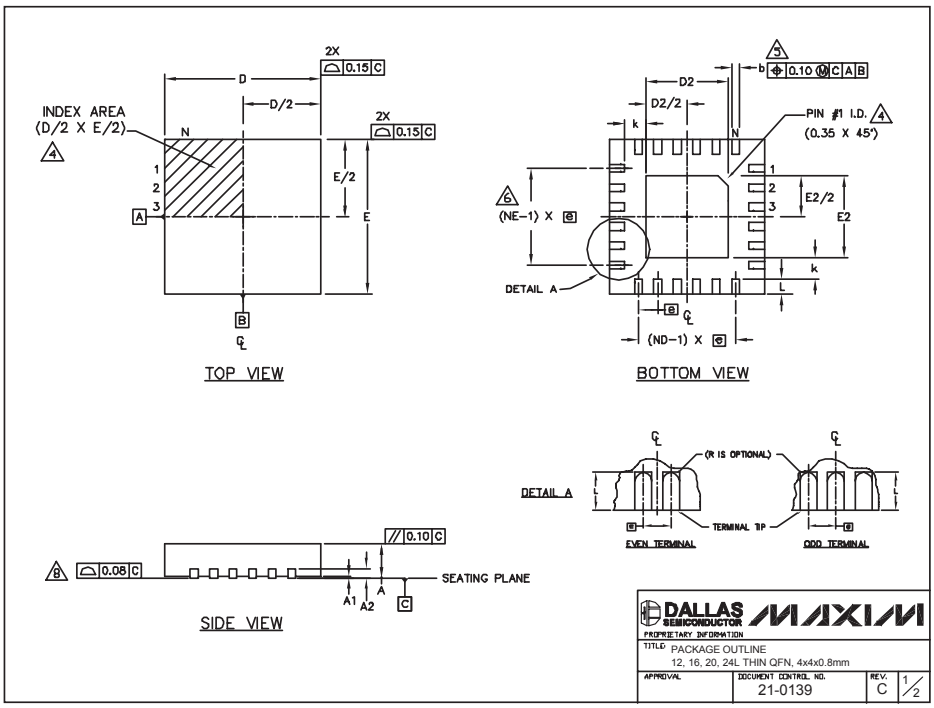


Dual, Audio, Log Taper Digital Potentiometers

Package Information

(The package drawing(s) in this data sheet may not reflect the most current specifications. For the latest package outline information, go to **www.maxim-ic.com/packages**.)

24L QFN THIN.EPS



COMMON DIMENSIONS												
PKG	12L 4x4			16L 4x4			20L 4x4			24L 4x4		
REF.	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A	0.70	0.75	0.80	0.70	0.75	0.80	0.70	0.75	0.80	0.70	0.75	0.80
A1	0.0	0.02	0.05	0.0	0.02	0.05	0.0	0.02	0.05	0.0	0.02	0.05
A2	0.20 REF			0.20 REF			0.20 REF			0.20 REF		
b	0.25	0.30	0.35	0.25	0.30	0.35	0.20	0.25	0.30	0.18	0.23	0.30
D	3.90	4.00	4.10	3.90	4.00	4.10	3.90	4.00	4.10	3.90	4.00	4.10
E	3.90	4.00	4.10	3.90	4.00	4.10	3.90	4.00	4.10	3.90	4.00	4.10
e	0.80 BSC.			0.65 BSC.			0.50 BSC.			0.50 BSC.		
k	0.25	-	-	0.25	-	-	0.25	-	-	0.25	-	-
L	0.45	0.55	0.65	0.45	0.55	0.65	0.45	0.55	0.65	0.30	0.40	0.50
N	12			16			20			24		
ND	3			4			5			6		
NE	3			4			5			6		
Jedec Var.	WGGB			WGGC			WGGD-1			WGGD-2		

EXPOSED PAD VARIATIONS							
PKG. CODES	D2			E2			DOWN BONDS ALLOWED
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.	
T1244-2	1.95	2.10	2.25	1.95	2.10	2.25	NO
T1244-3	1.95	2.10	2.25	1.95	2.10	2.25	YES
T1244-4	1.95	2.10	2.25	1.95	2.10	2.25	NO
T1644-2	1.95	2.10	2.25	1.95	2.10	2.25	NO
T1644-3	1.95	2.10	2.25	1.95	2.10	2.25	YES
T1644-4	1.95	2.10	2.25	1.95	2.10	2.25	NO
T2044-1	1.95	2.10	2.25	1.95	2.10	2.25	NO
T2044-2	1.95	2.10	2.25	1.95	2.10	2.25	YES
T2044-3	1.95	2.10	2.25	1.95	2.10	2.25	NO
T2444-1	2.45	2.60	2.63	2.45	2.60	2.63	NO
T2444-2	1.95	2.10	2.25	1.95	2.10	2.25	YES
T2444-3	2.45	2.60	2.63	2.45	2.60	2.63	YES
T2444-4	2.45	2.60	2.63	2.45	2.60	2.63	NO

NOTES:

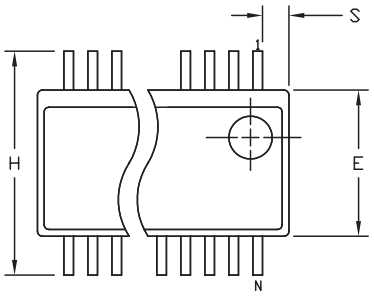
1. DIMENSIONING & TOLERANCING CONFORM TO ASME Y14.5M-1994.
2. ALL DIMENSIONS ARE IN MILLIMETERS. ANGLES ARE IN DEGREES.
3. N IS THE TOTAL NUMBER OF TERMINALS.
4. THE TERMINAL #1 IDENTIFIER AND TERMINAL NUMBERING CONVENTION SHALL CONFORM TO JESD 95-1 SPP-012. DETAILS OF TERMINAL #1 IDENTIFIER ARE OPTIONAL, BUT MUST BE LOCATED WITHIN THE ZONE INDICATED. THE TERMINAL #1 IDENTIFIER MAY BE EITHER A MOLD OR MARKED FEATURE.
5. DIMENSION b APPLIES TO METALLIZED TERMINAL AND IS MEASURED BETWEEN 0.25 mm AND 0.30 mm FROM TERMINAL TIP.
6. ND AND NE REFER TO THE NUMBER OF TERMINALS ON EACH D AND E SIDE RESPECTIVELY.
7. DEPOPULATION IS POSSIBLE IN A SYMMETRICAL FASHION.
8. COPLANARITY APPLIES TO THE EXPOSED HEAT SINK SLUG AS WELL AS THE TERMINALS.
9. DRAWING CONFORMS TO JEDEC MO220, EXCEPT FOR T2444-1, T2444-3 AND T2444-4.

DALLAS SEMICONDUCTOR MAXIM
PROPRIETARY INFORMATION
TITLE: PACKAGE OUTLINE
12, 16, 20, 24L THIN QFN, 4x4x0.8mm
APPROVAL
DOCUMENT CONTROL NO. 21-0139
REV. C
2/2

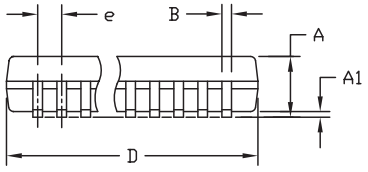
Package Information (continued)

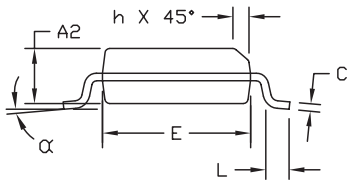
(The package drawing(s) in this data sheet may not reflect the most current specifications. For the latest package outline information, go to **www.maxim-ic.com/packages**.)

QSOP.EPS



	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	.061	.068	1.55	1.73
A1	.004	.0098	0.102	0.249
A2	.055	.061	1.40	1.55
B	.008	.012	0.20	0.30
C	.0075	.0098	0.191	0.249
D	SEE VARIATIONS			
E	.150	.157	3.81	3.99
e	.025 BSC		0.635 BSC	
H	.230	.244	5.84	6.20
h	.010	.016	0.25	0.41
L	.016	.035	0.41	0.89
N	SEE VARIATIONS			
α	0°	8°	0°	8°





VARIATIONS:

	INCHES		MILLIMETERS			
	MIN.	MAX.	MIN.	MAX.	N	
D	.189	.196	4.80	4.98	16	AB
S	.0020	.0070	0.05	0.18		
D	.337	.344	8.56	8.74	20	AD
S	.0500	.0550	1.270	1.397		
D	.337	.344	8.56	8.74	24	AE
S	.0250	.0300	0.635	0.762		
D	.386	.393	9.80	9.98	28	AF
S	.0250	.0300	0.635	0.762		

NOTES:
1). D & E DO NOT INCLUDE MOLD FLASH OR PROTRUSIONS.
2). MOLD FLASH OR PROTRUSIONS NOT TO EXCEED .006" PER SIDE.
3). CONTROLLING DIMENSIONS: INCHES.
4). MEETS JEDEC MO137.

DALLAS SEMICONDUCTOR MAXIM
PROPRIETARY INFORMATION

TITLE:
PACKAGE OUTLINE, QSOP .150", .025" LEAD PITCH

APPROVAL	DOCUMENT CONTROL NO.	REV.	
	21-0055	E	1/1

Mouser Electronics

Authorized Distributor

Click to View Pricing, Inventory, Delivery & Lifecycle Information:

Maxim Integrated:

MAX5410EEE+ MAX5408EEE+ MAX5408EEE+T MAX5408ETE+ MAX5408ETE+T MAX5409EEE+ MAX5409EEE+T MAX5409ETE+ MAX5409ETE+T MAX5410EEE+T MAX5410ETE+ MAX5410ETE+T MAX5411EEE+ MAX5411EEE+T MAX5411ETE+ MAX5411ETE+T