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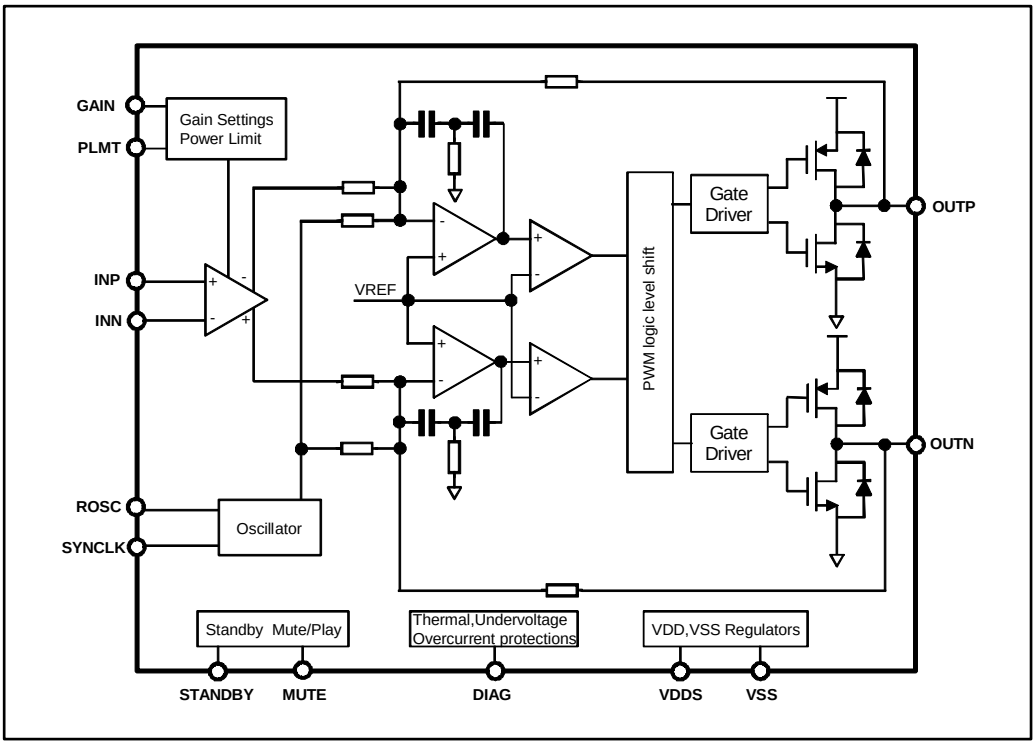
1 Device block diagram

Figure 1: "Internal block diagram (showing one channel only)" shows the block diagram of one of the two identical channels of the TDA7492E.

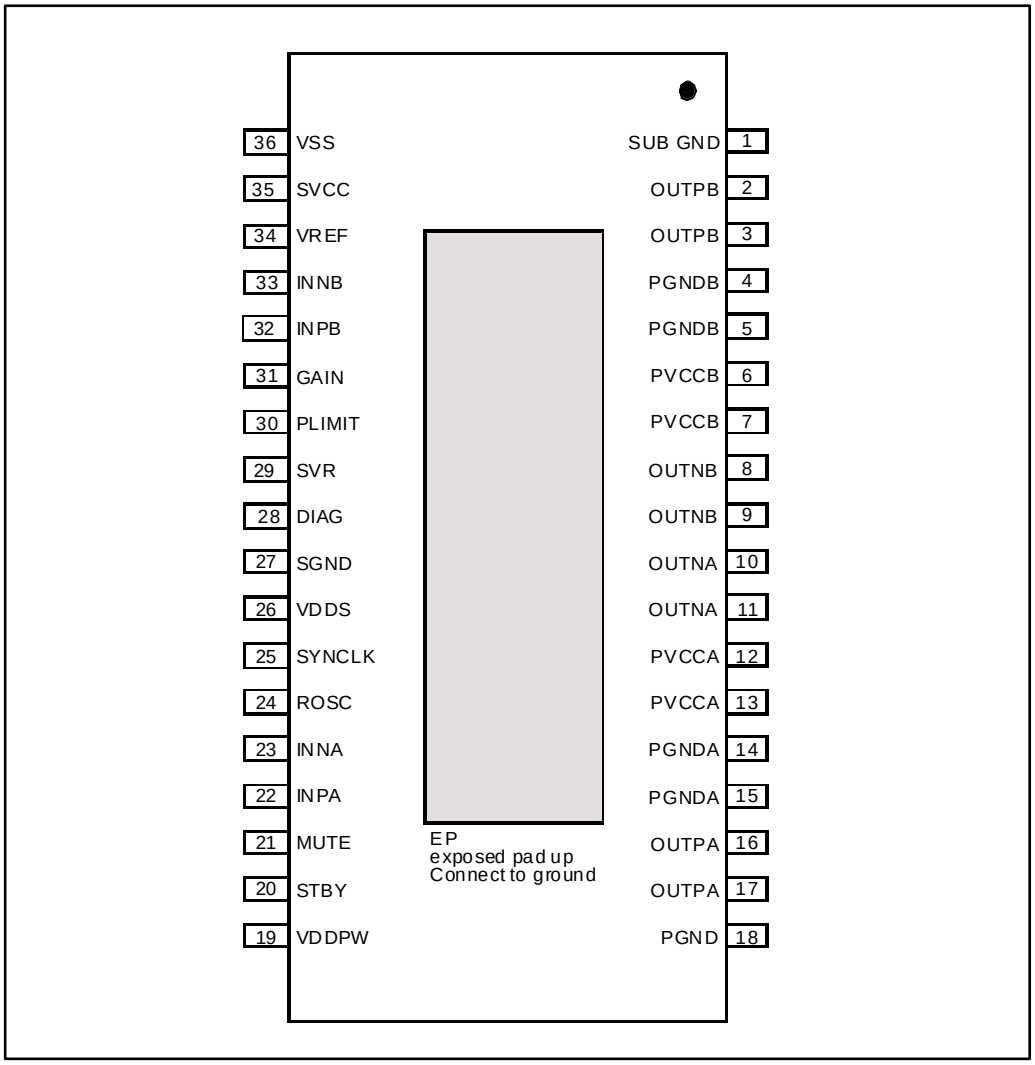
Figure 1: Internal block diagram (showing one channel only)



2 Pin description

2.1 Pinout

Figure 2: Pin connections (top view, PCB view)



2.2 Pin list

Table 2: Pin description list

Number	Name	Type	Description
1	SUB_GND	PWR	Connect to the frame
2, 3	OUTPB	O	Positive PWM for right channel
4, 5	PGNDB	PWR	Power stage ground for right channel
6, 7	PVCCB	PWR	Power supply for right channel
8, 9	OUTNB	O	Negative PWM output for right channel
10, 11	OUTNA	O	Negative PWM output for left channel
12, 13	PVCCA	PWR	Power supply for left channel
14, 15	PGNDA	PWR	Power stage ground for left channel
16, 17	OUTPA	O	Positive PWM output for left channel
18	PGND	PWR	Power stage ground
19	VDDPW	O	3.3 V (nominal) regulator output referred to ground for power stage
20	STBY	I	Standby mode control
21	MUTE	I	Mute mode control
22	INPA	I	Positive differential input of left channel
23	INNA	I	Negative differential input of left channel
24	ROSC	O	Master oscillator frequency-setting pin
25	SYNCLK	I/O	Clock in/out for external oscillator
26	VDDS	O	3.3 V (nominal) regulator output referred to ground for signal blocks
27	SGND	PWR	Signal ground
28	DIAG	O	Open-drain diagnostic output
29	SVR	O	Supply voltage rejection
30	PLIMIT	I	Output voltage level setting
31	GAIN	I	Gain setting input
32	INPB	I	Positive differential input of right channel
33	INNB	I	Negative differential input of right channel
34	VREF	O	Half VDDS (nominal) referred to ground
35	SVCC	PWR	Signal power supply
36	VSS	O	3.3 V (nominal) regulator output referred to power supply
-	EP	-	Exposed pad for heatsink, to be connected to GND

3 Electrical specifications

3.1 Absolute maximum ratings

Table 3: Absolute maximum ratings

Symbol	Parameter	Value	Unit
V_{CC}	DC supply voltage for pins PVCCA, PVCCB, SVCC	30	V
VI	Voltage limits for input pins STBY, MUTE, INNA, INPA, INNB, INPB, GAIN, MODE	-0.3 to +4.6	V
T_{op}	Operating temperature	-40 to +85	°C
T_j	Junction temperature	-40 to +150	°C
T_{stg}	Storage temperature	-40 to +150	°C

3.2 Thermal data

Table 4: Thermal data

Symbol	Parameter	Min.	Typ.	Max.	Unit
$R_{th\ j\text{-}case}$	Thermal resistance, junction-to-case	-	2.98		°C/W

3.3 Electrical specifications

Unless otherwise stated, the results in *Table 5: "Electrical specifications"* below are given for the conditions: V_{CC} = 26 V, R_L= 6 Ω, R_{OSC} = 33 kΩ, f = 1 kHz, G_V = 20.8 dB and Tamb = 25 °C.

Table 5: Electrical specifications

Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
V_{CC}	Supply voltage for pins PVCCA, PVCCB, SVCC	-	7	-	26	V
I_q	Total quiescent current	Without LC, no load	-	40		mA
I_{qSTBY}	Quiescent current in standby	-	-	1	-	µA
V_{OS}	Output offset voltage	Vi = 0, Av = 20 dB, no load		20		mV
I_{OCP}	Overcurrent protection threshold	R_L = 0 Ω	9	10	13	A
T_j	Junction temperature at thermal shutdown	-	140	150	160	°C
R_i	Input resistance	Differential input		60	-	kΩ
R_{dsON}	Power transistor on-resistance	High side	-	0.2	-	Ω
		Low side	-	0.2	-	
G_V	Closed-loop gain	GAIN < 0.25*Vdd		20.8	-	dB
		0.25*Vdd < GAIN < 0.5*Vdd	-	26.8	-	
		0.5*Vdd < GAIN < 0.75*Vdd	-	30	-	
		GAIN1>0.75*Vdd	-	32.8	-	
ΔG_V	Gain matching	-	-	-	±1	dB
CT	Crosstalk	f = 1 kHz	-	70	-	dB
SVRR	Supply voltage rejection ratio	fr = 100 Hz, Vr = 0.5 V, C_{SVR} = 10 µF	-	60	-	dB
T_r, T_f	Rise and fall times	PWM signal 50% duty cycle	-	24	40	ns
f_{SW}	Switching frequency	Internal oscillator with external Rosc = 33 kΩ	-	500	-	kHz
f_{SWR}	Output switching frequency range	With internal oscillator by changing Rosc (1)	450	-	550	kHz
V_{inH}	Digital input high (H)	-	2.0	-	-	V
V_{inL}	Digital input low (L)		-	-	0.8	
Function mode	Standby, Mute, Play	STBY < 0.5 V Mute = 'X'	Standby			
		STBY > 2.5 V Mute < 0.8 V	Mute			
		STBY > 2.5 V Mute > 2.5 V	Play			
A_{MUTE}	Mute attenuation	V_{MUTE} = 1 V	60	80	-	dB

Notes:

(1)$f_{SW} = 10^6 / [(12 * R_{OSC} + 110) * 4]$ kHz, $f_{SYNCLK} = 2 * f_{SW}$ (where R_{OSC} is in kΩ and f_{SW} in kHz) with Rosc = 33 kΩ.

3.4 Stereo BTL application

All specifications are for V_{CC} = 22 V, Rosc = 33 kΩ, f = 1 kHz, Tamb = 25 °C, unless otherwise specified.

Table 6: Stereo BTL application

Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
P_o	Output power	R_L = 6 Ω, THD = 10%	-	41	-	W
		R_L = 6 Ω, THD = 1%	-	32	-	
		R_L = 6 Ω, THD = 10%, V_{CC} = 26 V	-	57	-	
		R_L = 6 Ω, THD = 1%, V_{CC} = 26 V	-	44	-	
THD	Total harmonic distortion	P_o = 1 W, fin = 1 kHz	-	0.04	-	%
VN	Total output noise	Inputs shorted and connected to GND, A curve, G_V = 20.8 dB	-	150	-	µV

3.5 Parallel BTL (mono) application

All specifications are for V_{CC} = 22 V, Rosc = 33 kΩ, f = 1 kHz, Tamb = 25 °C, INPB, INNB connected to VDDS, unless otherwise specified.

Table 7: Stereo BTL (mono) application

Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
P_o	Output power	R_L = 3 Ω, THD = 10%	-	90	-	W
		R_L = 3 Ω, THD = 1%	-	70	-	
		R_L = 3 Ω, THD = 10%, Vcc = 26 V	-	110	-	
		R_L = 3 Ω, THD = 1%, V_{CC} = 26V	-	86	-	
THD	Total harmonic distortion	P_o = 1 W, fin = 1 kHz	-	0.04	-	%
VN	Total output noise	Inputs shorted and connected to GND, A curve, G_V = 20.8 dB	-	150	-	µV

4 Application information

4.1 Gain setting

The four gain settings of the TDA7492E are set by GAIN (pin 31). Internally, gain is set by changing the feedback resistors of the amplifier.

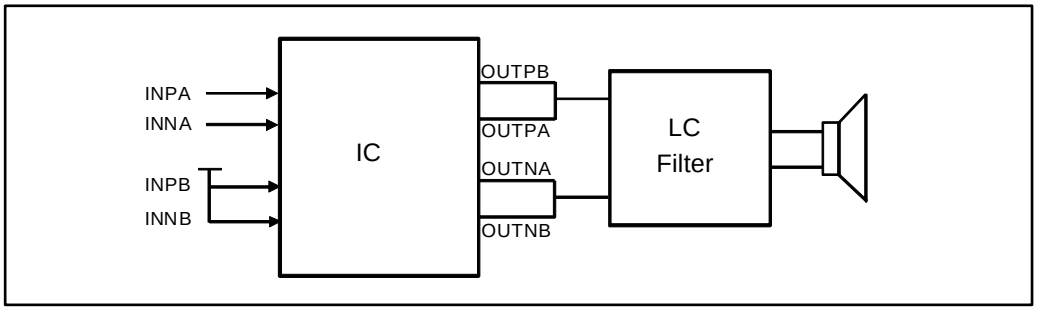
Table 8: Gain settings

Voltage on GAIN pin	Total gain	Application recommendations
V_{GAIN} < 0.25*VDDS	20.8 dB	GAIN pin connected to SGND
0.25*VDDS < V_{GAIN} < 0.5*VDDS	26.8 dB	External resistor divider <100 k
0.5*VDDS < V_{GAIN} < 0.75*VDDS	30 dB	External resistor divider <100 k
V_{GAIN} > 0.75*VDDS	32.8 dB	GAIN pin connected to VDDS

4.2 Stereo and mono applications

The TDA7492E can be used in stereo BTL or in mono BTL configuration. When the input pins, INPB and INNB of the right channel are directly shorted to VDDS (without input capacitors) the device is in mono configuration as shown in *Figure 3: "Mono BTL settings"*.

Figure 3: Mono BTL settings



4.3 Smart protections

4.3.1 Overcurrent protection (OCP)

If the overcurrent protection threshold is reached, the power stage will be shut down immediately. The device will recover automatically when the fault is removed.

The overcurrent protection scheme is shown in *Table 9: "Overcurrent protection"*. Two typical thresholds are as follows.

Table 9: Overcurrent protection

	I (Shutdown)
High side (A)	11.2
Low side (A)	10.0

The thresholds in MUTE mode are reduced to about 1/2 and two typical thresholds are as follows.

Table 10: Overcurrent protection (mute mode)

	I (Shutdown)
High side (A)	6.2
Low side (A)	5.9

4.3.2 Thermal protection

When internal die temperature exceeds 140 °C, the device enters into Mute by pulling the MUTE pin low first.

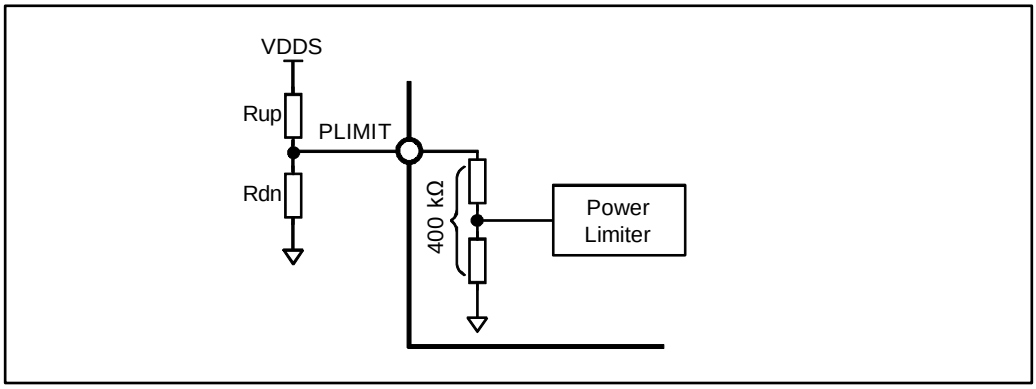
When internal die temperature exceeds 150 °C, the device directly shuts down the power stage. The TDA7492E automatically recovers when the temperature become lower than the threshold.

4.3.3 Power limit

A built-in power limit is used to limit the output voltage level below the supply rail by limiting the duty cycle. The limit level is set through the voltage at PLIMIT (pin 30). The pin voltage is set by the following equation:

$$VPLIMIT = V_{DD}\left[\frac{(Rdn//400k)}{(Rdn//400k + Rup)}\right]$$

Figure 4: Recommended power limit pin connections



It is recommended that external resistors are less than 40 kΩ if a voltage divider is used as shown in *Figure 4: "Recommended power limit pin connections"*. The relationship of the maximum duty cycle (Dmax) and the voltage at P_{LIMIT} is:

$$Dmax = \frac{\left\{8.8 \times \frac{VPLIMIT}{V_{cc} - \frac{2 \times V_{cc} \times Rs}{Rload \times 2 \times Rs}} + 1\right\}}{2}$$

Where V_{CC} is the power supply voltage, VPLIMIT is the voltage applied at the P_{LIMIT} pin, Rs is the series resistance including Rdson of power transistor, output filter resistance and bonding wire resistance. Rload is the load resistance.

An example of maximum effective control voltage at P_{LIMIT} vs. power supply and load resistance is shown in *Table 11: "Max effective voltage of PLIMIT pin vs. power supply and load"*.

Table 11: Max effective voltage of PLIMIT pin vs. power supply and load

Rload	Power supply		
	7 V	13 V	24 V
4 Ω	0.71 V	1.32 V	2.44 V
6 Ω	0.74 V	1.37 V	2.53 V
8 Ω	0.75 V	1.39 V	2.57 V

4.4 Mode selection

The three operating modes of the TDA7492E are set by two inputs: STBY (pin 20) and MUTE (pin 21).

- Standby mode: all circuits are turned off, very low current consumption.
- Mute mode: inputs are connected to ground and the positive and negative PWM outputs are at 50% duty cycle
- Play mode: the amplifiers are active.

The protection functions of the TDA7492E are implemented by pulling down the voltages of the STBY and MUTE inputs shown in *Figure 5: "Standby and mute circuits"*. The input current of the corresponding pins must be limited to 200 µA.

Table 12: Mode settings

Mode	STBY	MUTE
Standby	L(1)	X (don't care)
Mute	H	L
Play	H	H

Notes:

(1)Drive levels defined in *Table 5: "Electrical specifications"*.

Figure 5: Standby and mute circuits

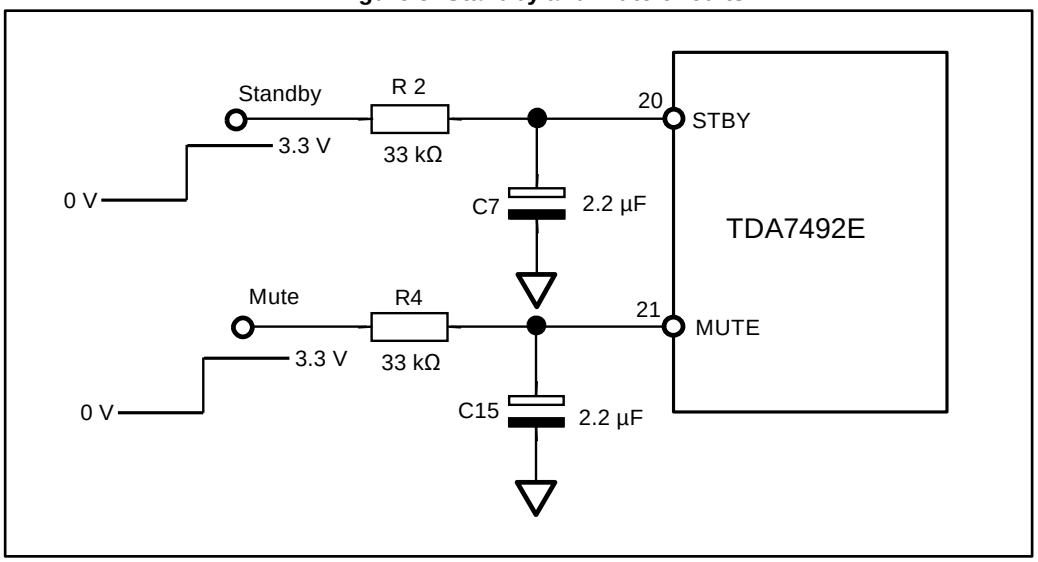
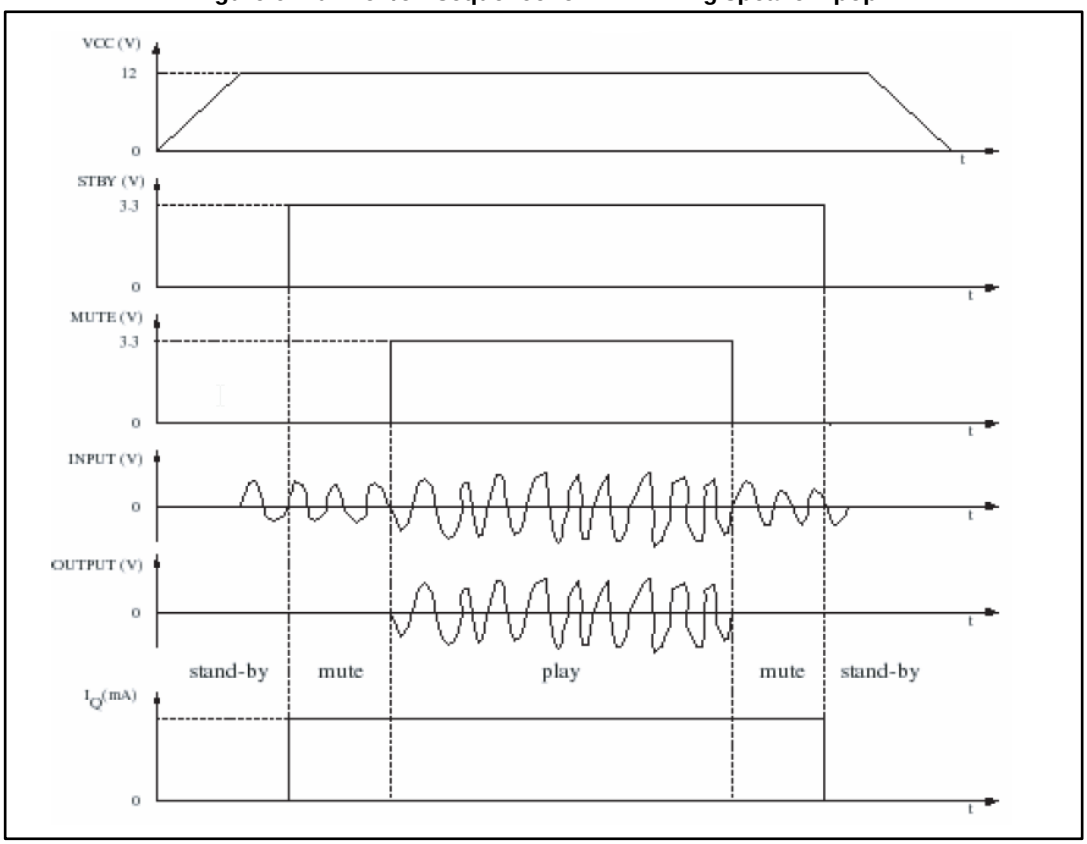
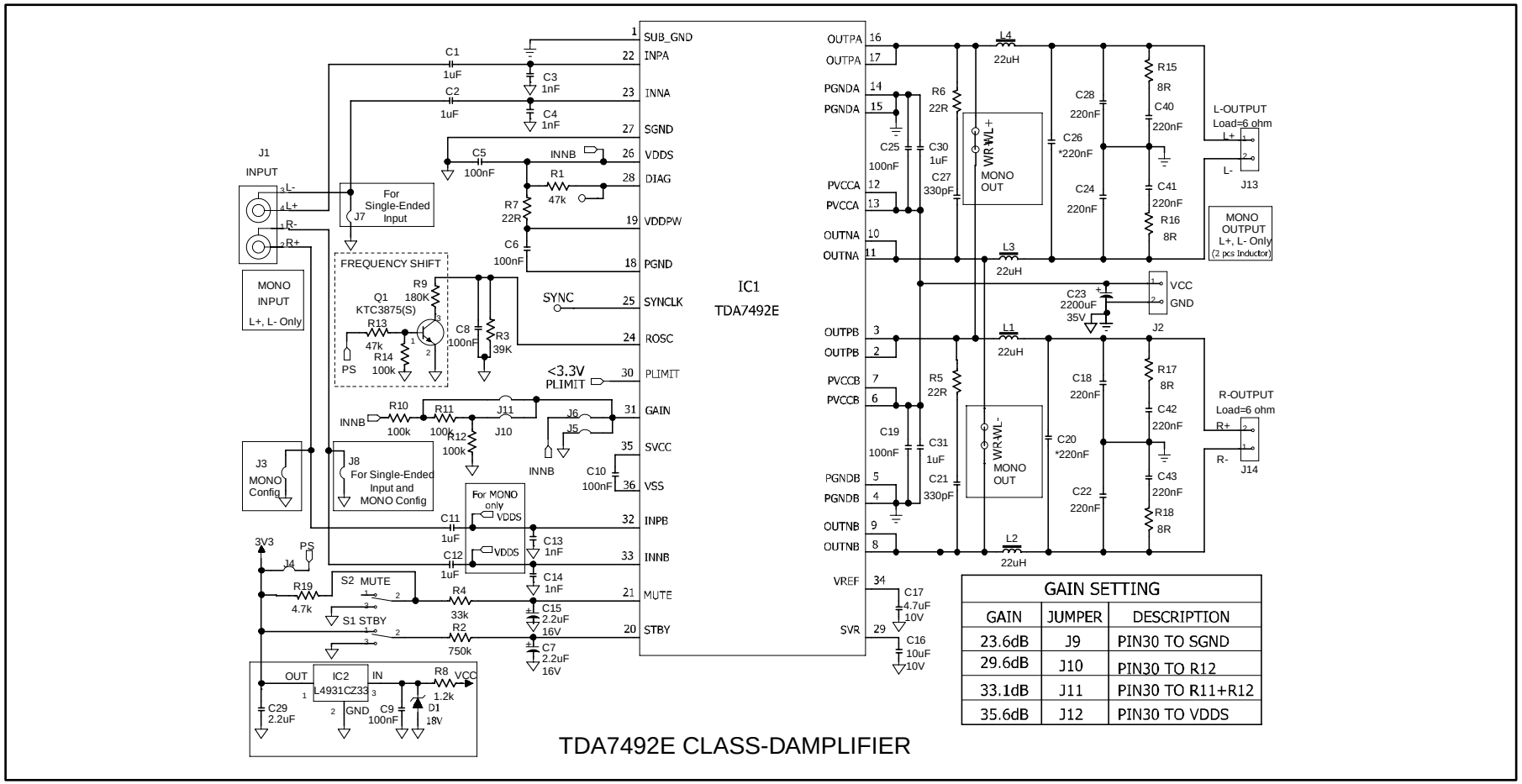


Figure 6: Turn-on/off sequence for minimizing speaker “pop”



5 Schematic diagram

Figure 7: Application circuit



TDA7492E CLASS-DAMPLIFIER

6 Characterization curves

Unless otherwise stated, measurements were made under the following conditions: V_{CC} = 22 V, Rl = 6 Ω, f = 1 kHz, Gv = 20.8 dB, R_{OSC} = 33 kΩ, T_{amb} = 25 °C.

Note: Maximum output power must be derated according to case temperature.

6.1 Stereo configuration

The following characterization curves were made using the TDA7492E demonstration board (*Figure 7: "Application circuit"*). The characterization curves were made under the following test conditions:

Vs = 7 and 26 V, R_l = 6 Ω, Rosc = 33 kΩ, Cosc = 100 nF, Gain = 20.8 dB and Tamb = 25°C unless otherwise specified.

Figure 8: Output power vs. supply voltage

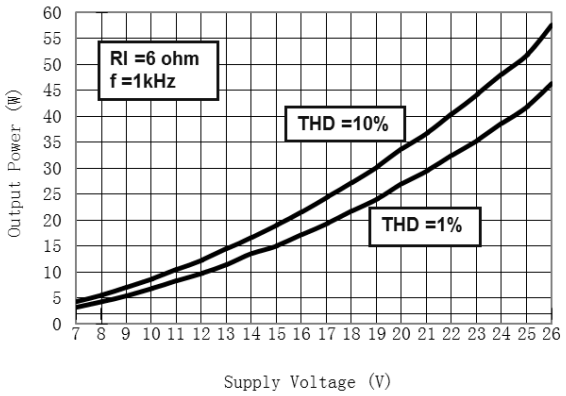


Figure 9: THD vs. Pout (Vs = 26 V, f = 1 kHz)

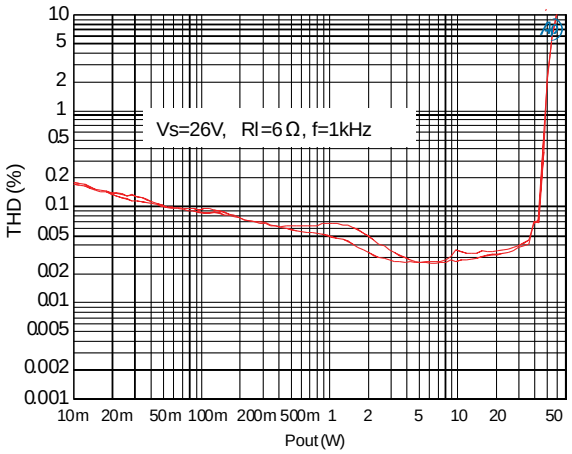


Figure 10: THD vs. Pout (Vs = 26 V, f = 100 Hz)

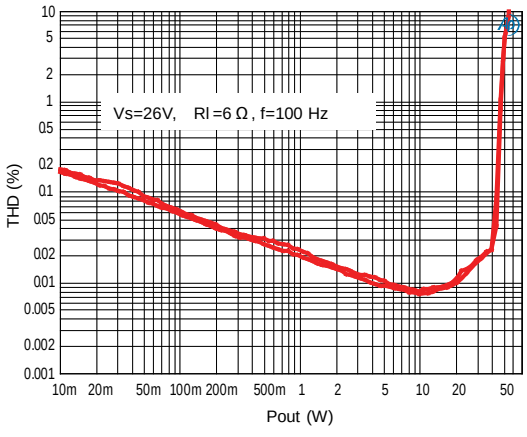


Figure 11: THD vs. Pout (Vs = 26 V, f = 6 kHz)

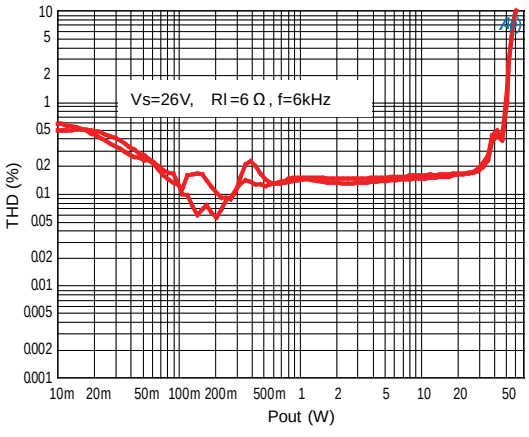


Figure 12: THD vs. frequency (Vs = 26 V, Po = 1 W)

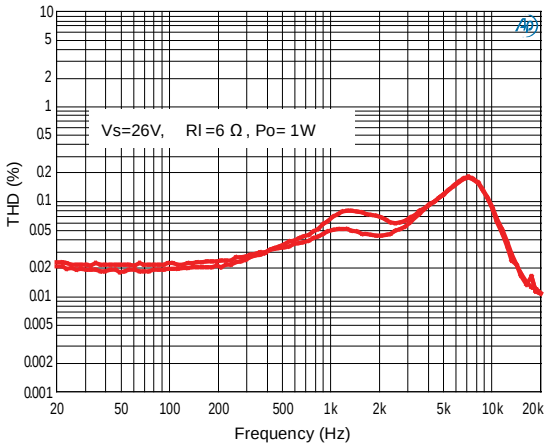


Figure 13: Frequency response Vs = 26 V

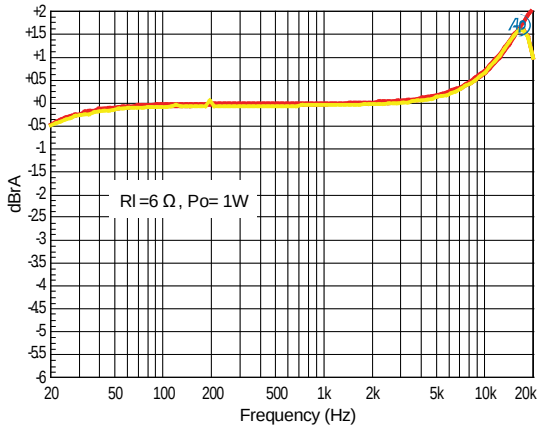


Figure 14: Signal-to-noise ratio (Vs = 26 V, gain = 32.6 dB, not weighted)

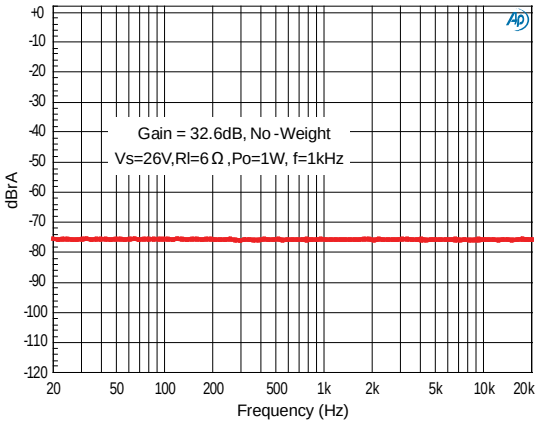


Figure 15: Signal-to-noise ratio (Vs = 26 V, gain = 20.6 dB, not weighted)

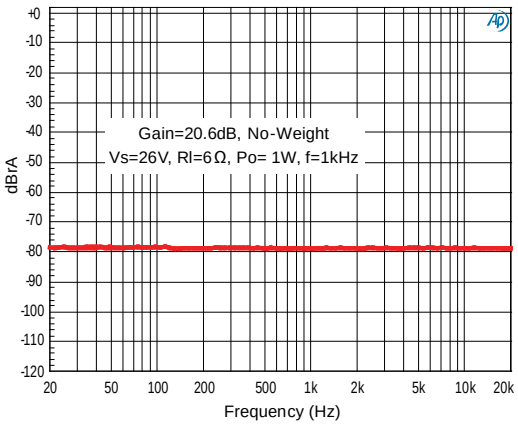


Figure 16: Signal-to-noise ratio (Vs = 26 V, gain = 32.6 dB, A-weighted)

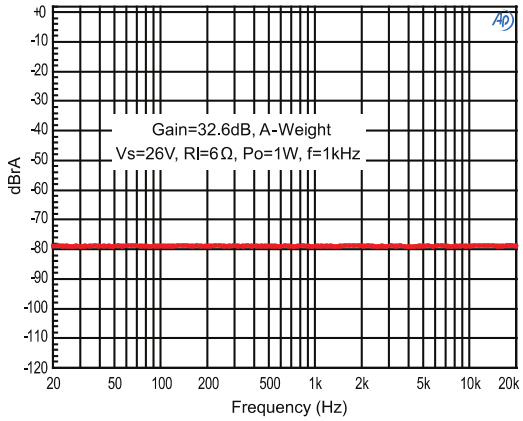


Figure 17: Signal-to-noise ratio (Vs = 26 V, gain = 20.6 dB, A-weighted)

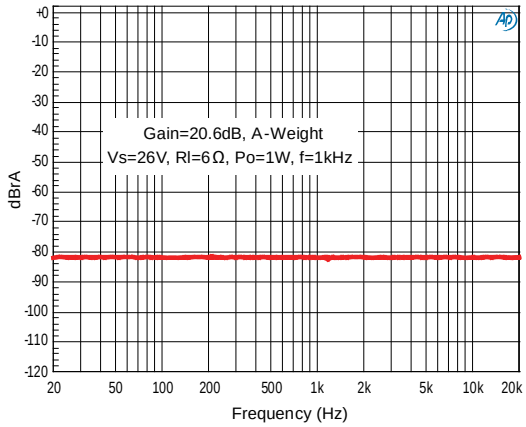


Figure 18: Crosstalk Vs = 26 V

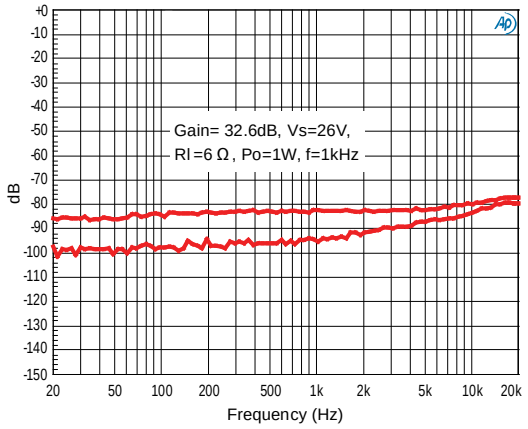


Figure 19: FFT (0 dB) Vs = 26 V

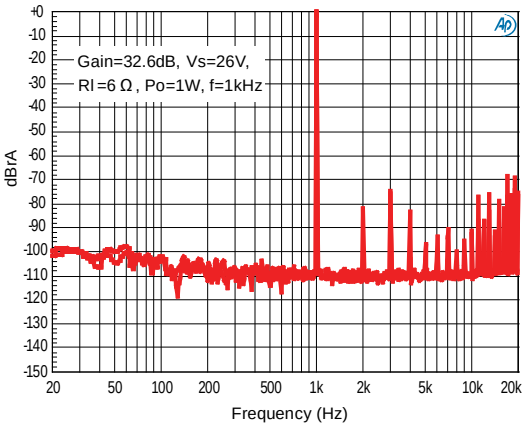
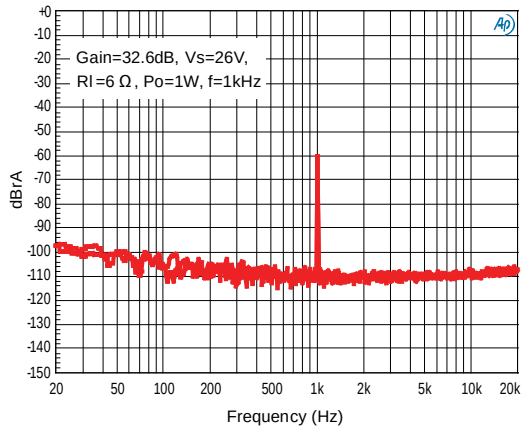


Figure 20: FFT (-60 dB) Vs = 26 V



7 Package information

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: ***www.st.com***. ECOPACK® is an ST trademark.

7.1 PowerSSO36 EPU package information

The device comes in a 36-pin PowerSSO package with exposed pad up (EPU).

Figure 21: "PowerSSO-36 EPU package outline" shows the package outline and *Table 13: "PowerSSO-36 EPU package mechanical data"* gives the dimensions.

Figure 21: PowerSSO-36 EPU package outline

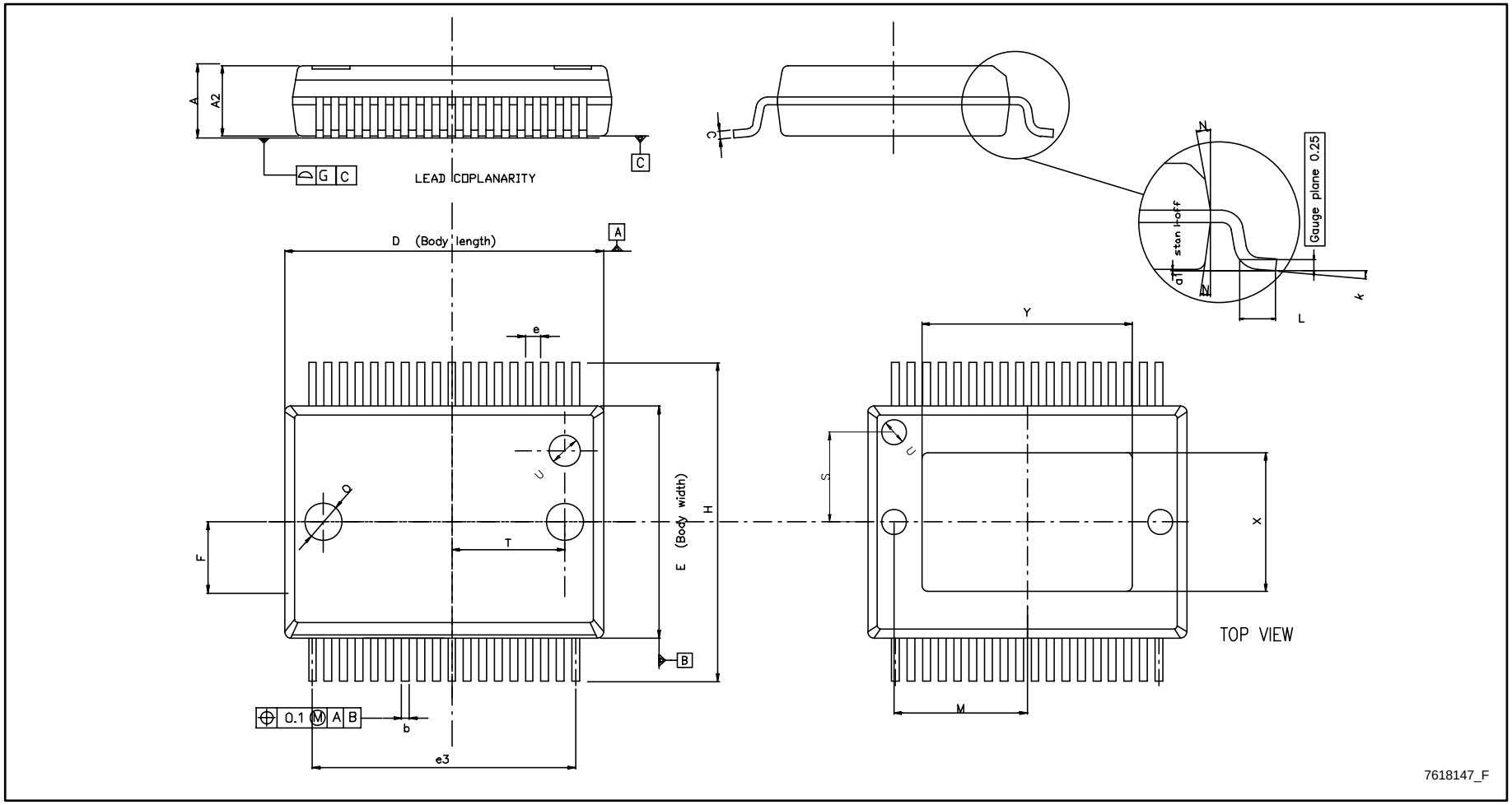


Table 13: PowerSSO-36 EPU package mechanical data

Symbol	Dimensions in mm			Dimensions in inches		
	Min.	Typ.	Max.	Min.	Typ.	Max.
A	2.15	-	2.45	0.085	-	0.096
A2	2.15	-	2.35	0.085	-	0.093
a1	0	-	0.10	0	-	0.004
b	0.18	-	0.36	0.007	-	0.014
c	0.23	-	0.32	0.009	-	0.013
D	10.10	-	10.50	0.398	-	0.413
E	7.40	-	7.60	0.291	-	0.299
e	-	0.5	-	-	0.020	-
e3	-	8.5	-	-	0.335	-
F	-	2.3	-	-	0.091	-
G	-	-	0.10	-	-	0.004
H	10.10	-	10.50	0.398	-	0.413
h	-	-	0.40	-	-	0.016
k	0	-	8 degrees	0	-	8 degrees
L	0.55	-	0.85	0.022	-	0.033
M	-	4.30	-	-	0.169	-
N	-	-	10 degrees	-	-	10 degrees
O	-	1.20	-	-	0.047	-
Q	-	0.80	-	-	0.031	-
S	-	2.90	-	-	0.114	-
T	-	3.65	-	-	0.144	-
U	-	1.00	-	-	0.039	-
X	4.10	-	4.70	0.161	-	0.185
Y	4.90	-	7.10	0.193	-	0.280

8 Revision history

Table 14: Document revision history

Date	Revision	Changes
24-Feb-2017	1	Initial release

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