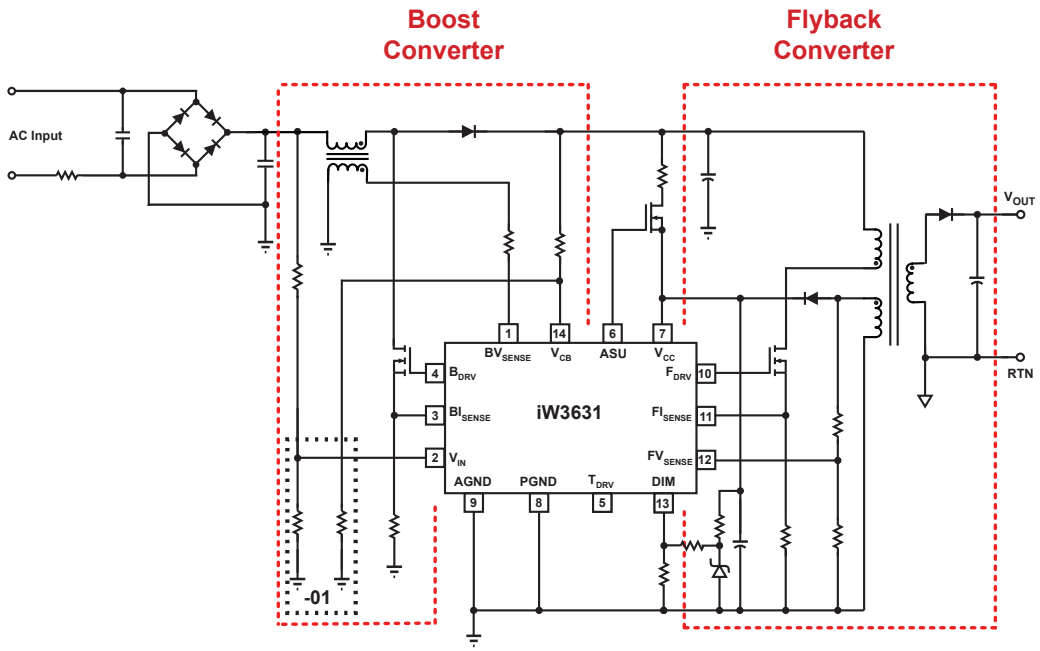


Figure 3.1 : iW3631 Analog Dimming Simplified Schematic with Internal (-00) or External (-01) Sensing

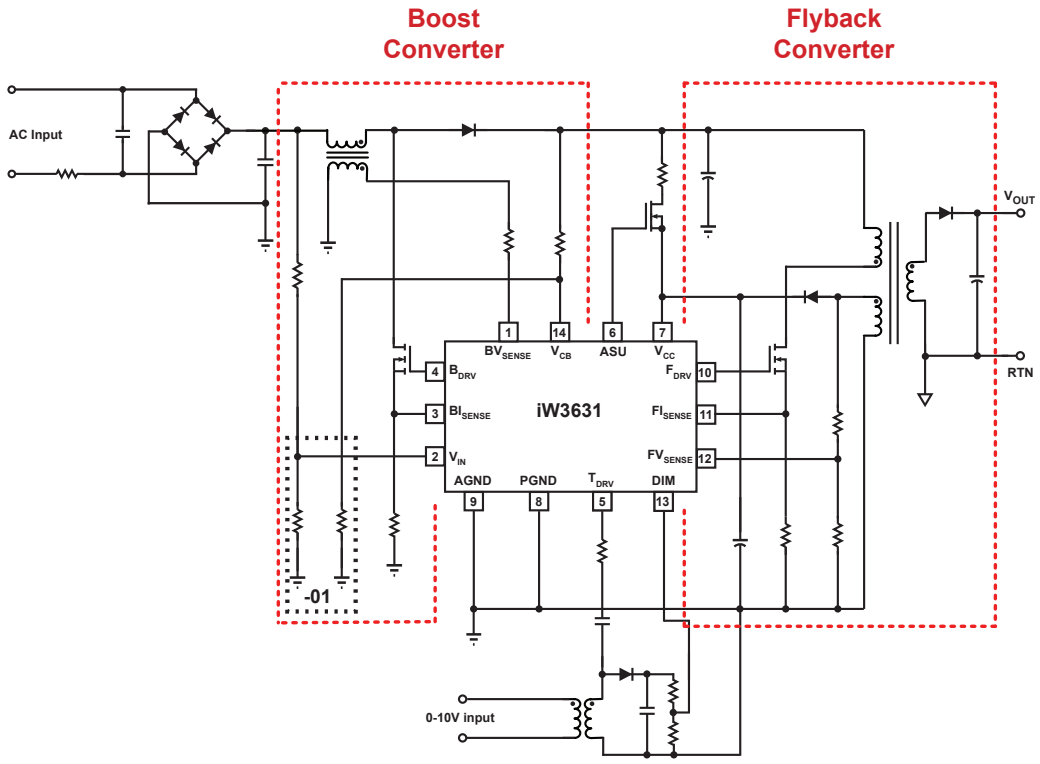


Figure 3.2 : iW3631 0-10V Dimming Simplified Schematic with Internal (-00) or External (-01) Sensing

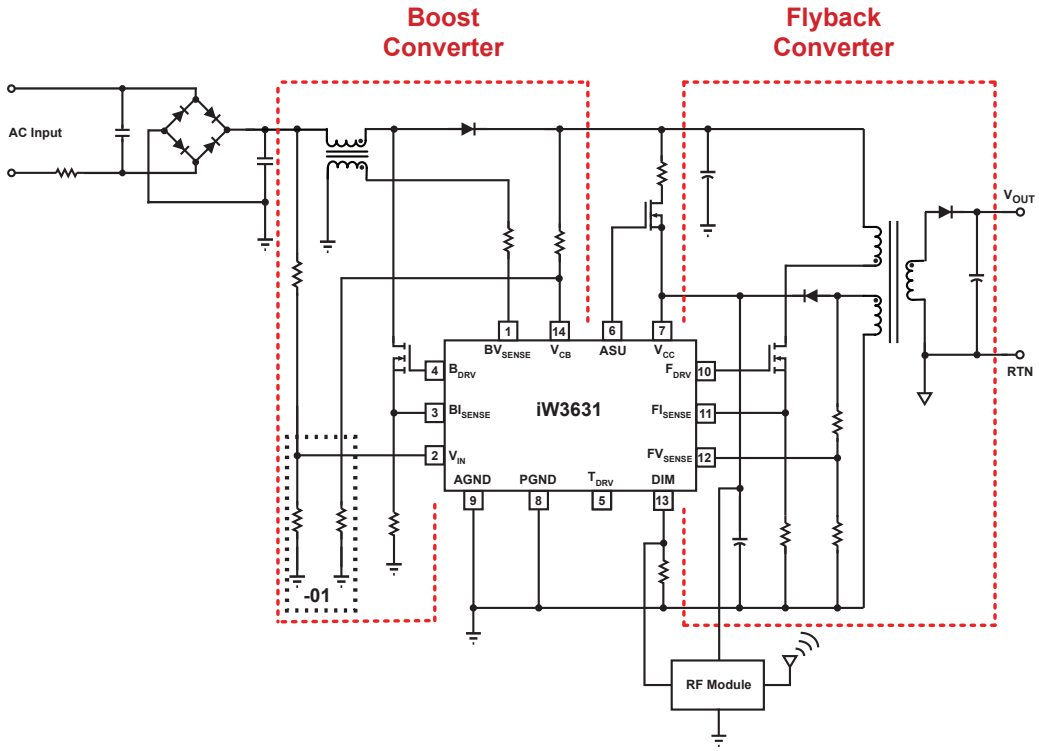


Figure 3.3 : iW3631 Wireless Dimming Simplified Schematic with Internal (-00) or External (-01) Sensing

4 Pinout Description

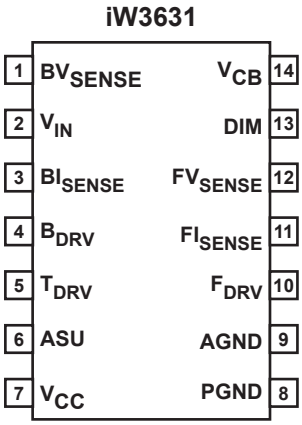


Figure 4.1 : 14-Lead SOIC-14 Package

Pin Number	Pin Name	Type	Pin Description
1	BV_{SENSE}	Analog Input	Boost inductor voltage feedback used for valley mode switching.
2	V_{IN}	Analog Input	Rectified AC line voltage feedback. -00 uses internal resistor (15kΩ typically) to sense line voltage; -01 needs an external resistor connected from this pin to GND.
3	BI_{SENSE}	Analog Input	Boost current sense (only used for cycle-by-cycle peak current limit). Connect an approximately 1kΩ resistor to the source of the boost MOSFET switch to improve noise immunity.
4	B_{DRV}	Output	Gate drive for boost MOSFET.
5	T_{DRV}	Output	0-10V isolation transformer drive output.
6	ASU	Output	Control signal for active start-up device. This signal is pulled low after start-up is finished to cut off the active device. If not using active start-up device, leave this pin floating.
7	V_{CC}	Power	Power supply for control logic and voltage sense for power-on reset circuitry. A decoupling capacitor of 0.1µF or so should be connected between the V_{CC} pin and GND.
8	PGND	Ground	Power ground.
9	AGND	Ground	Signal ground.
10	F_{DRV}	Output	Gate drive for flyback MOSFET.
11	FI_{SENSE}	Analog Input	Primary current sense (used for cycle-by-cycle peak current control and limit). Connect an approximately 1kΩ resistor to the source of the flyback MOSFET switch to improve noise immunity.
12	FV_{SENSE}	Analog Input	Auxiliary voltage sense (used for primary-side regulation and valley mode switching).
13	DIM	Analog Input	Dimming level control input.
14	V_{CB}	Analog Input	Boost output voltage feedback. -00 uses internal resistor (15kΩ typically) to sense line voltage; -01 needs an external resistor connected from this pin to GND.

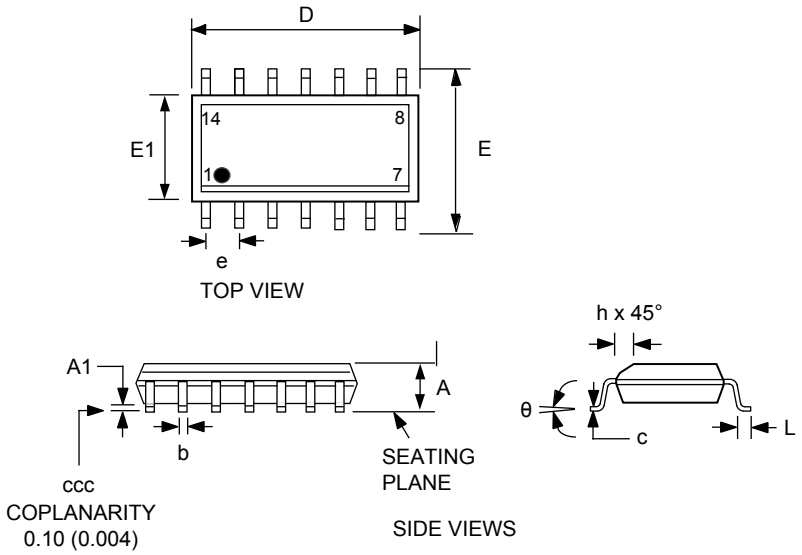
5 Absolute Maximum Ratings

Absolute maximum ratings are the parameter values or ranges which can cause permanent damage if exceeded.

Parameter	Symbol	Value	Units
DC supply voltage range (pin 7)	V_{CC}	-0.3 to 18	V
F_{DRV} output (pin 10)		-0.3 to 18	V
B_{DRV} output (pin 4)		-0.3 to 18	V
T_{DRV} output (pin 5)		-0.3 to 18	V
FV_{SENSE} input (pin 12, I ≤ 10mA)		-0.7 to 4.0	V
BV_{SENSE} input (pin 1, I ≤ 3mA)		-0.7 to 4.0	V
V_{IN} input (pin 2)		-0.3 to 18	V
V_{CB} input (pin 14)		-0.3 to 18	V
FI_{SENSE} input (pin 11)		-0.3 to 4.0	V
BI_{SENSE} input (pin 3)		-0.3 to 4.0	V
ASU output (pin 6)		-0.3 to 18	V
DIM input (pin 13)		-0.3 to 4.0	V
Maximum junction temperature	T_{JMAX}	150	°C
Operating junction temperature	T_{JOPT}	-40 to 150	°C
Storage temperature	T_{STG}	-65 to 150	°C
Thermal Resistance Junction-to-PCB Board Surface Temperature	ψ_{JB}	45	°C/W
ESD rating per JEDEC JESD22-A114		±2,000	V

6 Physical Dimensions

14-Lead SOIC Package



Symbol	Inches		Millimeters	
	MIN	MAX	MIN	MAX
A	0.053	0.069	1.35	1.75
A1	0.004	0.010	0.10	0.25
b	0.013	0.020	0.33	0.51
c	0.007	0.010	0.19	0.25
D	0.337	0.344	8.55	8.75
E1	0.150	0.157	3.80	4.00
E	0.228	0.244	5.80	6.20
e	0.050 BSC		1.27 BSC	
L	0.016	0.050	0.40	1.27
h	0.010	0.020	0.25	0.50
θ	0°	8°	0°	8°
ccc	0.004		0.10	

Compliant to JEDEC Standard MS12F

Controlling dimensions are in inches; millimeter dimensions are for reference only

This product is RoHS compliant and Halide free.

Soldering Temperature Resistance:
[a] Package is IPC/JEDEC Std 020D Moisture Sensitivity Level 1
[b] Package exceeds JEDEC Std No. 22-A111 for Solder Immersion Resistance; package can withstand 10 s immersion < 260˚C

Dimension D does not include mold flash, protrusions or gate burrs. Mold flash, protrusions or gate burrs shall not exceed 0.15 mm per end. Dimension E does not include interlead flash or protrusion. Interlead flash or protrusion shall not exceed 0.25 mm per side.

The package top may be smaller than the package bottom. Dimensions D and E are determined at the outermost extremes of the plastic body exclusive of mold flash, tie bar burrs, gate burrs and interlead flash, but including any mismatch between the top and bottom of the plastic body.

Figure 6.1 : Physical Dimensions of 14-Pin SOIC Package

7 Ordering Information

Part Number	Options	Package	Description
iW3631-00	Internal sensing for V_{IN} and V_{CB}; Z_{IN} = 15kΩ and Z_{CB} = 15kΩ	SOIC-14	Tape & Reel[1]
iW3631-01	External sensing for V_{IN} and V_{CB}	SOIC-14	Tape & Reel[1]

Note 1: Tape & Reel packing quantity is 2,500/reel. Minimum ordering quantity is 2,500.

Two-Stage, Flickerless™ 0-10V Dimmable Digital Off-Line LED Driver with High PF and Low THD

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