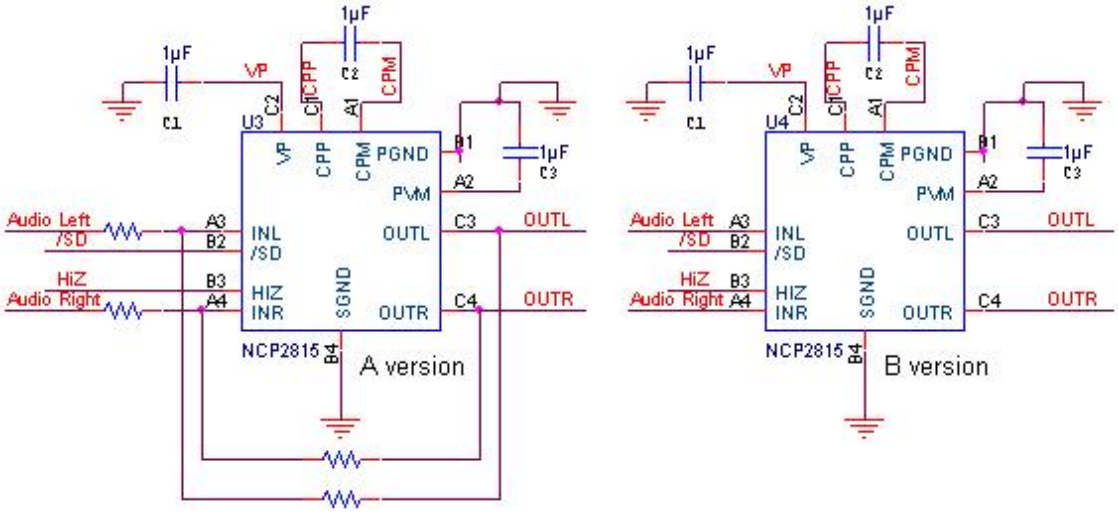


Figure 1. Typical Application Circuit

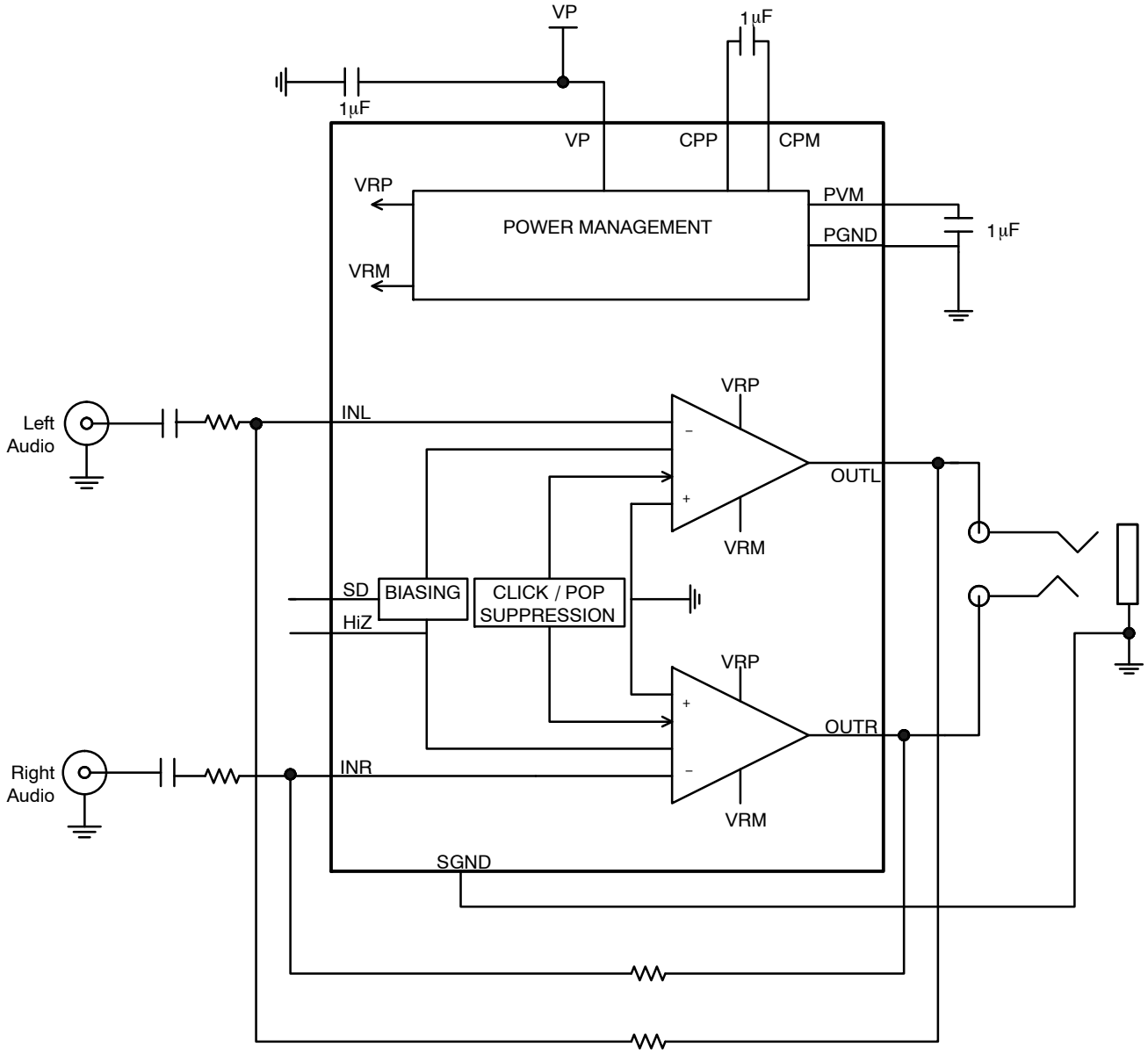


Figure 2. Typical Application Schematic Version A

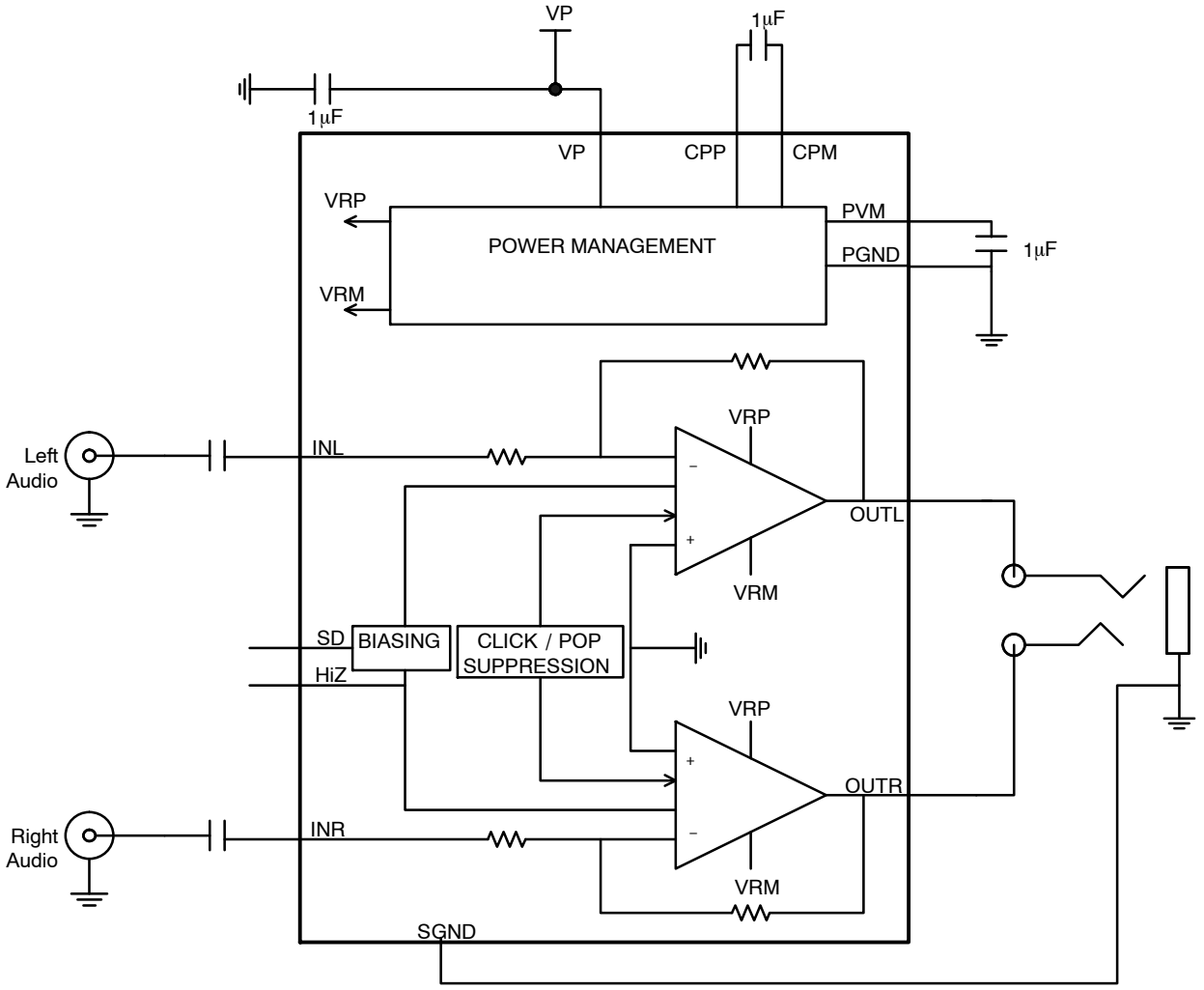


Figure 3. Typical Application Schematic Version B

PIN FUNCTION DESCRIPTION

Pin	Pin Name	Type	Description
A1	CPM	Input / Output	Charge pump flying capacitor negative terminal. A 1 μF ceramic filtering capacitor to CPP is required
A2	PVM	Output	Charge pump output. A 1 μF ceramic filtering capacitor to ground is required
A3	INL	Input	Left input of the audio source
A4	INR	Input	Right input of the audio source
B1	PGND	Ground	Power ground
B2	/SD	Input	Enable activation.
B4	SGND	Ground	Sense Ground. Connect to shield terminal of headphone jack or ground plane.
C1	CPP	Input / Output	Charge pump flying capacitor positive terminal. A 1 μF ceramic filtering capacitor to CPM is required.
C2	VP	Power	Positive supply voltage, connected to a Lithium/Ion battery or other power supply.
C3	OUTL	Output	Left audio channel output signal
C4	OUTR	Output	Right audio channel output signal
B3	HiZ	Input	Output high impedance mode activation.

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
V_P Pin: Power Supply Voltage (Note 1)	V_{IN}	−0.3 to + 4.5	V
INL, INR, /SD pins	V_{mr1}	−0.3 to V_P + 0.3	V
HiZ, OUTL, OUTR pins	V_{mr2}	−0.3 − V_P to V_P + 0.3	V
Human Body Model (HBM) ESD Rating are (Note 2)	ESD HBM	2000	V
Machine Model (MM) ESD Rating are (Note 2)	ESD MM	200	V
CSP 1.2 x 1.6 mm package (Notes 6 and 7) Thermal Resistance Junction to Case	$R_{\theta JC}$	(Note 7)	°C/W
Operating Ambient Temperature Range	T_A	−40 to + 85	°C
Operating Junction Temperature Range	T_J	−40 to + 125	°C
Maximum Junction Temperature (Note 6)	T_{JMAX}	+ 150	°C
Storage Temperature Range	T_{STG}	−65 to + 150	°C
Moisture Sensitivity (Note 5)	MSL	Level 1	

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

1. Maximum electrical ratings are defined as those values beyond which damage to the device may occur at T_A = 25 °C.
2. According to JEDEC standard JESD22−A108B.
3. This device series contains ESD protection and passes the following tests:
   Human Body Model (HBM) ±2.0 kV per JEDEC standard: JESD22−A114 for all pins.
   Machine Model (MM) ±200 V per JEDEC standard: JESD22−A115 for all pins.
4. Latch up Current Maximum Rating: ±100 mA per JEDEC standard: JESD78 class II.
5. Moisture Sensitivity Level (MSL): 1 per IPC/JEDEC standard: J−STD−020A.
6. The thermal shutdown set to 160°C (typical) avoids irreversible damage on the device due to power dissipation.
7. The $R_{\theta CA}$ is dependent on the PCB heat dissipation. The maximum power dissipation (PD) is dependent on the min input voltage, the max output current and the selected external components.

$$R_{\theta CA} = \frac{125 - T_A}{P_D} - R_{\theta JC}$$

ELECTRICAL CHARACTERISTICS Min & Max Limits apply for T_A between −40°C to +85°C and T_J up to + 125°C for V_{IN} between 1.6 V to 3.6 V (Unless otherwise noted). Typical values are referenced to T_A = + 25°C and V_P = 1.8 V.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{BAT}	Supply voltage range		1.6		3.6	V
I_{SD}	Shutdown current				1	μA
I_Q	Quiescent current	V_P = 1.8 V		1.6	2.2	mA
R_{IN}	Input resistance		15	20	25	kΩ
R_{SD}	/SD pull−down resistor			300		kΩ
R_{HiZ}	HiZ pull−down resistor			150		kΩ
	Maximum input signal swing			2.8		V_{P-P}
V_{IH}	High−level input voltage SD and HiZ pin		1.2			V
V_{IL}	Low−level input voltage SD and HiZ pin				0.4	V
UVLO	UVLO threshold	Falling edge		1.4		V
$UVLO_{HYS}$	UVLO hysteresis			100		mV
T_{SD}	Thermal shutdown temperature			160		°C
V_{OS}	Output offset voltage	Input AC grounded		±0.5		mV
T_{WU}	Turning On time			1		ms
V_{LP}	Max Output Swing (peak value) (Note 8)	HSV_{BAT} = 1.8 V, Headset = 32 Ω	1.13			V_{peak}
P_O	Max Output Power (Note 8)	HSV_{BAT} = 1.8 V, THD+N = 1% Headset = 16 Ω Headset = 32 Ω	 20	 35 32		mW
P_O	Max Output Power	HSV_{BAT} = 3.6 V, THD+N = 1% Headset = 16 Ω Headset = 32 Ω		 62 35		mW
	Crosstalk (Note 8)	Headset ≥ 16 Ω		−80	−60	dB
PSRR	Power Supply Rejection Ratio	Inputs Shorted to Ground F = 217 Hz to 1 kHz		−100		dB
THD+N	Total Harmonic Distortion + Noise	Headset = 16 Ω P_{OUT} = 10 mW, F = 1 kHz		0.03		%
THD+N	Total Harmonic Distortion + Noise	Headset = 32 Ω P_{OUT} = 10 mW, F = 1 kHz		0.01		%
THD+N	Total Harmonic Distortion + Noise	Headset = 32 Ω V_{OUT} = 400 mV, F = 1 kHz		−78		dB
SNR	Signal to noise ratio			100		dB
Z_{SD}	Output Impedance in Shutdown Mode			20		kΩ
Z_{HiZ}	Output Impedance in High Impedance Mode		15	20	25	kΩ
	Max channel to channel gain tolerance	B Version only, T_A = +25 °C	−2	±0.3	+2	%
F_{SW1}	Headset charge pump switching frequency	P_{OUT} > 500 μW		1		MHz
F_{SW2}	Headset charge pump switching frequency	P_{OUT} < 500 μW		125		kHz
A_V	Voltage Gain	B version only	−1.54	−1.5	−1.46	V/V

8. Guaranteed by design and characterized.
9. Typical application circuit as depicted

TYPICAL OPERATING CHARACTERISTICS

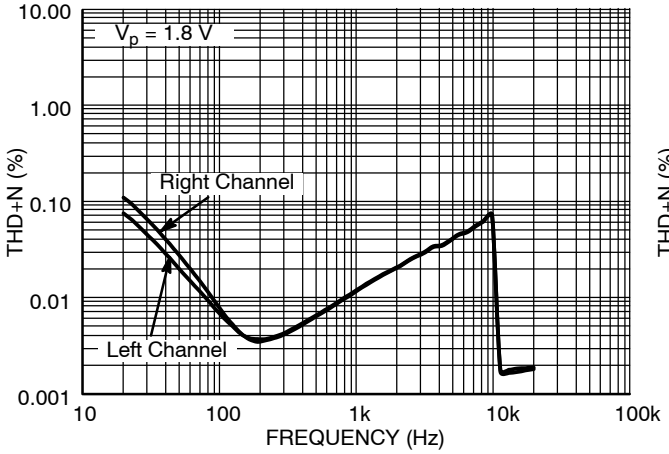


Figure 4. THD+N vs Frequency in Phase, 32 Ω Load, P_{out} = 10 mW

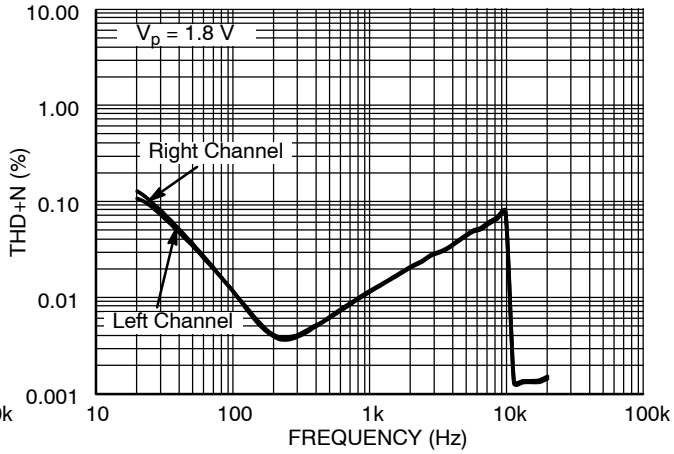


Figure 5. THD+N vs Frequency in Phase, 32 Ω Load, P_{out} = 10 mW

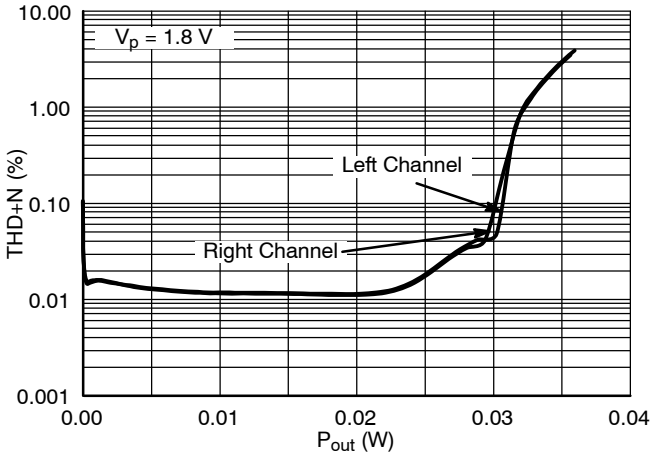


Figure 6. THD+N vs P_{out}, 32 Ω Load

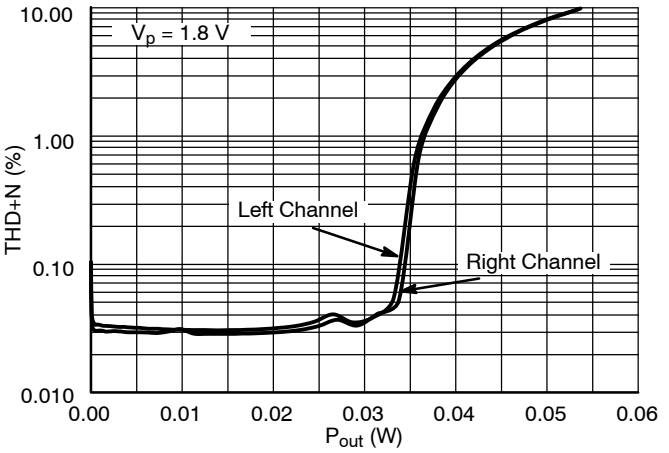


Figure 7. THD+N vs P_{out}, 16 Ω Load

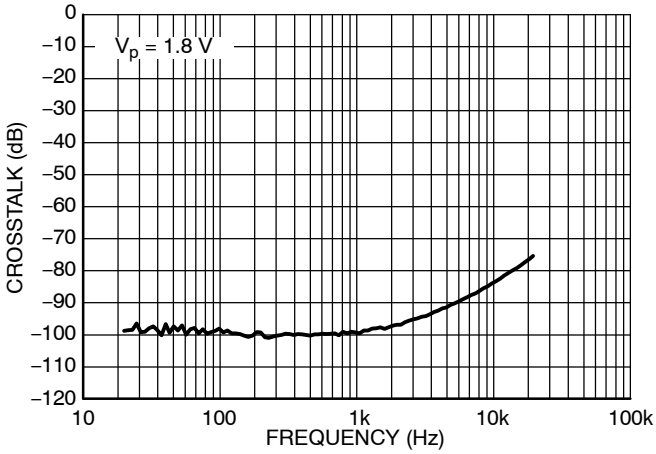


Figure 8. Power Supply Rejection Ratio vs. Frequency

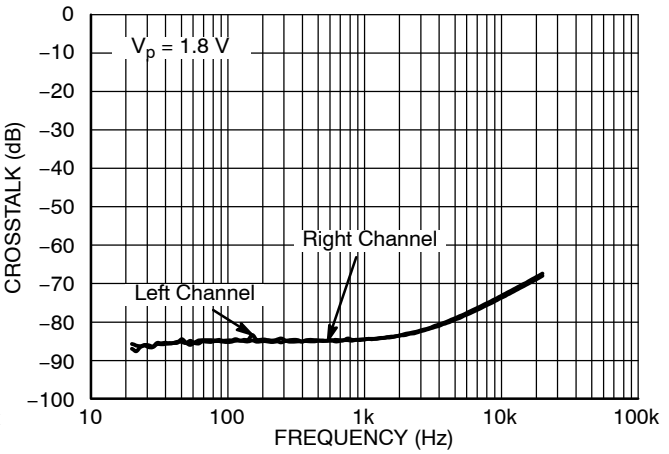


Figure 9. Crosstalk vs. Frequency, R_{load} = 32 Ω, P_{out} = 10 mW

TYPICAL OPERATING CHARACTERISTICS

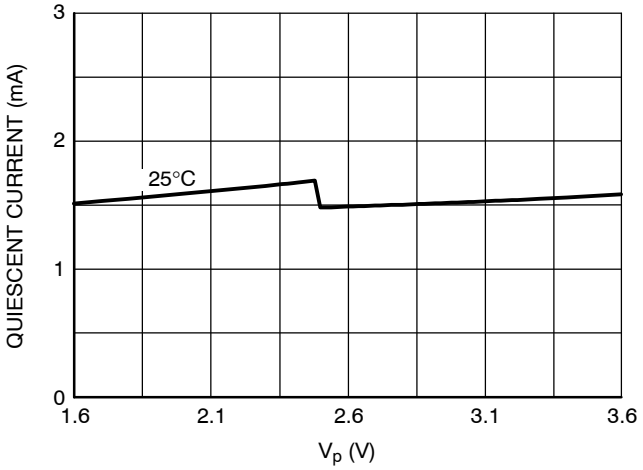


Figure 10. Quiescent Current vs Power Supply

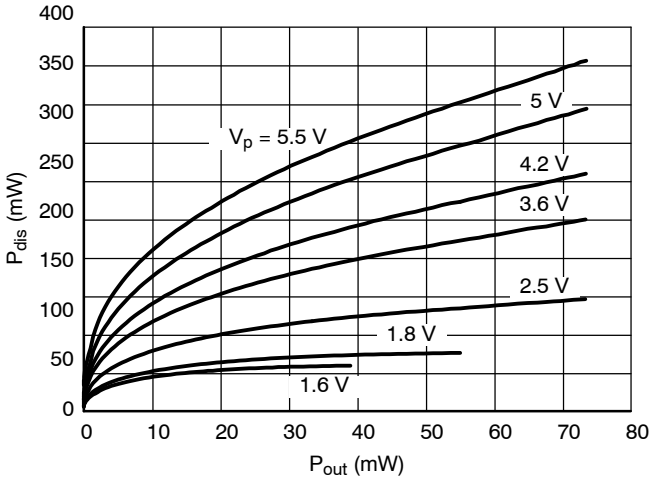


Figure 11. Power Dissipation vs P_{out} Left and Right in Phase

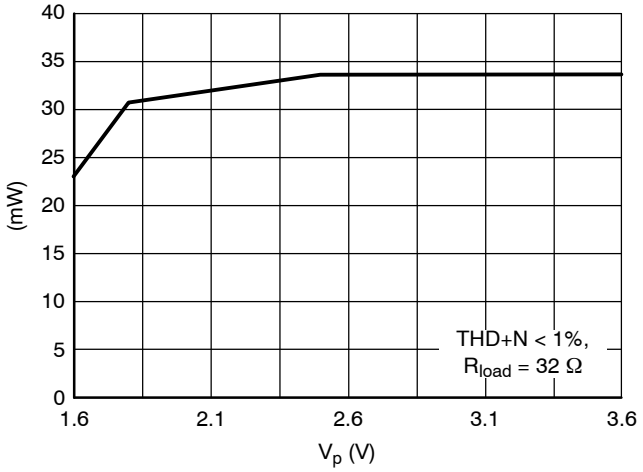


Figure 12. Max Output Power vs V_p, 32 Ω Load

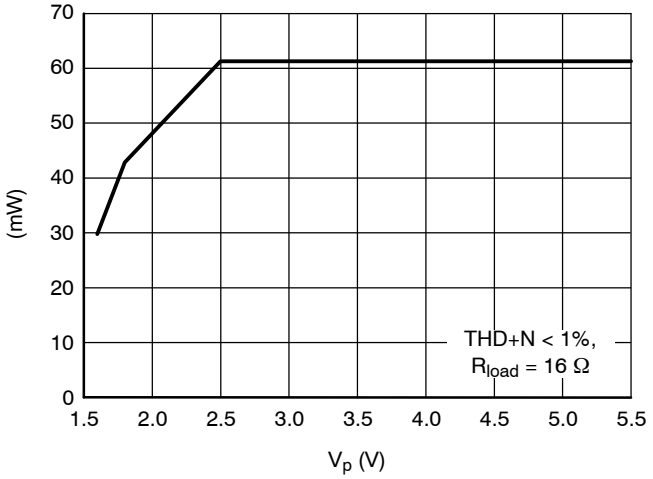


Figure 13. Max Output Power vs V_p, 16 Ω Load

DETAIL OPERATING DESCRIPTION

Detailed Description

The NCP2815 is a stereo headphone amplifier with NOCAP architecture. This architecture eliminates the need to use two big external capacitors required by conventional headphone amplifier.

The structure of the NCP2815 is composed of two true ground amplifiers, a UVLO, a short circuit protection and a thermal shutdown circuit. Additionally, a special circuit is embedded to eliminate any pop and click noise that occurs during turn on and turn off time. Version A has an external gain selectable by two resistors, Version B has a gain of 1.5 V/V.

NOCAP

NOCAP is a patented architecture which requires only 2 small ceramic capacitors. It generates a symmetrical positive and negative voltage which it allows the output of the amplifiers to be biased to ground.

LongPlay Architecture

NCP2815 includes a LongPlay architecture which helps to save battery life by reducing the quiescent current. The charge pump frequency is reduced to 125 kHz for an output load < 500 μW.

Current Limit Protection Circuit

The NCP2815 contains protection circuitry against shorts to ground. The currrent is limited to 300 mA when an output is shorted to GND and a signal appears at the input.

Thermal Overload Protection

Internal amplifiers are switched off when the temperature exceeds 160°C, and are switched back on when the temperature decreases below 140°C.

Under Voltage Lockout

When the battery voltage decreases below 1.4 V, the amplifiers are turned off. The hysteresis required to turn back on the device is 100 mV.

Pop and Click Suppression Circuitry

The NCP2815 includes a special circuit to eliminate any pop and click noise during turn on and turn off time. The amplifier creates an offset during these transitions at the output which give a parasitic noise called “pop and click noise”. The NCP2815 eliminates this problem.

Gain Setting Resistor Selection (Rin and Rf, A Version Only)

R_{in} and R_f set the closed loop gain of the amplifier. A low gain configuration (close to 1) minimizes the THD + noise values and maximizes the signal to noise ratio.

A closed loop gain in the range of 1 to 10 is recommended to optimize overall system performance.

The formula to calculate the gain is:

$$Av = -\frac{Rf}{Rin}$$

Input Capacitor Selection

The input coupling capacitor blocks the DC voltage at the amplifier input terminal. This capacitor creates a high−pass filter with R_{in} (externally selectable for Version A, 20 kΩ for Version B).

The size of the capacitor must be large enough to couple in the low frequencies without severe attenuation in the audio bandwith (20 Hz – 20 kHz).

The cut off frequency for the input high−pass filter is :

$$F_c = \frac{1}{2\pi R_{in} C_{in}}$$

A F_c < 20 Hz is recommended.

Charge Pump Capacitor Selection

Use a ceramic capacitor with low ESR for better performances. An X5R / X7R capacitor is recommended.

The flying capacitor (C2) serves to transfer charge during the generation of the negative voltage.

The PVM capacitor (C3) must be equal at least to the flying capacitor to allow maximum transfer charge.

Table 1 suggests typical values and manufacturers:

Table 1.

Value	Reference	Package	Manufac-turer
1 μF	C1005X5R0J105K	0402	TDK
1 μF	GRM155R60J105K19	0402	Murata

Lower value capacitors can be used but the maximum output power is reduced and the device may not operate to specifications.

Power Supply Decoupling Capacitor (C1)

The NCP2815 is a True Ground amplifier which requires an adequate decoupling capacitor to reduce noise and THD + N. It is recommended to use an X5R / X7R ceramic capacitor with a value of 1 μF and place it as close as possible to the Vp pin.

Shutdown Function

The device enters in shutdown mode when the shutdown signal is low. During the shutdown mode, the DC quiescent current of the circuit does not exceed 1 μA. In this configuration, the output impedance is 20 kΩ on each output.

Layout Recommendation

Connect C1 as close as possible to the Vp pin.

Connect C2 and C3 as close as possible to the NCP2815.

Route the audio signal and SGND far away from Vp, CPP, CPM, PVM and PGND to avoid any perturbation due to the switching.

ORDERING INFORMATION

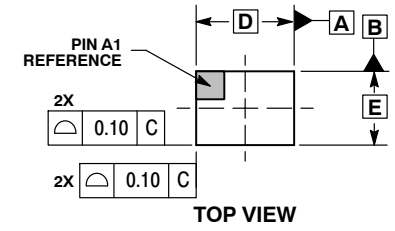
Device	Package	Shipping†
NCP2815AFCT2G	CSP – 12 – 1.6 x 1.2 mm (Pb–Free)	3000 / Tape & Reel
NCP2815BFCT2G	CSP – 12 – 1.6 x 1.2 mm (Pb–Free)	3000 / Tape & Reel
NCP2815BFCCT2G	CSP – 12 – 1.6 x 1.2 mm (Backside laminate coating) (Pb–Free)	3000 / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

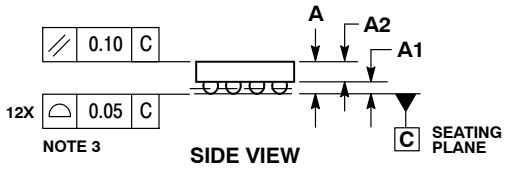
12 PIN FLIP−CHIP, 1.62x1.22, 0.4P
CASE 499BJ
ISSUE C

DATE 18 NOV 2015

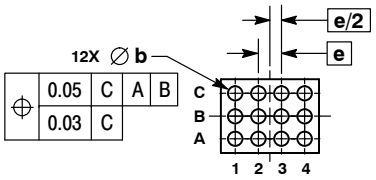
SCALE 4:1



TOP VIEW

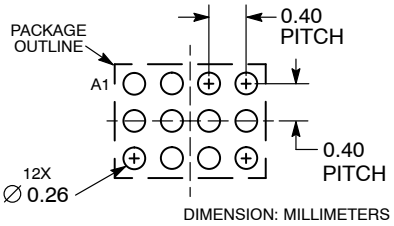


SIDE VIEW



BOTTOM VIEW

RECOMMENDED
SOLDERING FOOTPRINT

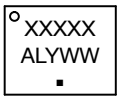


DIMENSION: MILLIMETERS

NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. COPLANARITY APPLIES TO SPHERICAL CROWNS OF SOLDER BALLS.

	MILLIMETERS	
DIM	MIN	MAX
A	0.50	0.56
A1	0.17	0.23
A2	0.33	0.39
b	0.24	0.29
D	1.62 BSC	
E	1.22 BSC	
e	0.40 BSC	

GENERIC
MARKING DIAGRAM*



XXXXX = Specific Device Code
A = Assembly Location
L = Wafer Lot
Y = Year
WW = Work Week
▪ = Pb−Free Package

*This information is generic. Please refer to device data sheet for actual part marking.
Pb−Free indicator, “G” or microdot “ ▪”, may or may not be present.

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DESCRIPTION:	**12 PIN FLIP−CHIP, 1.62 X 1.22, 0.4P**	**PAGE 1 OF 1**

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