CY7C1021CV33 Automotive

1-Mbit (64 K × 16) Static RAM

Features

- Temperature ranges
  - Automotive-A: –40 °C to 85 °C
  - Automotive-E: –40 °C to 125 °C
- Pin and function compatible with CY7C1021CV33
- High speed
  - t_{AA} = 10 ns (Automotive-A)
  - t_{AA} = 12 ns (Automotive-E)
- CMOS for optimum speed and power
- Low active power: 325 mW (max)
- Automatic power down when deselected
- Independent control of upper and lower bits
- Available in Pb-free and non Pb-free 44-pin 400 Mil SOJ, 44-pin TSOP II, and 48-ball FBGA packages

Functional Description

The CY7C1021CV33 is a high performance CMOS static RAM organized as 65,536 words by 16 bits. This device has an automatic power down feature that significantly reduces power consumption when deselected.

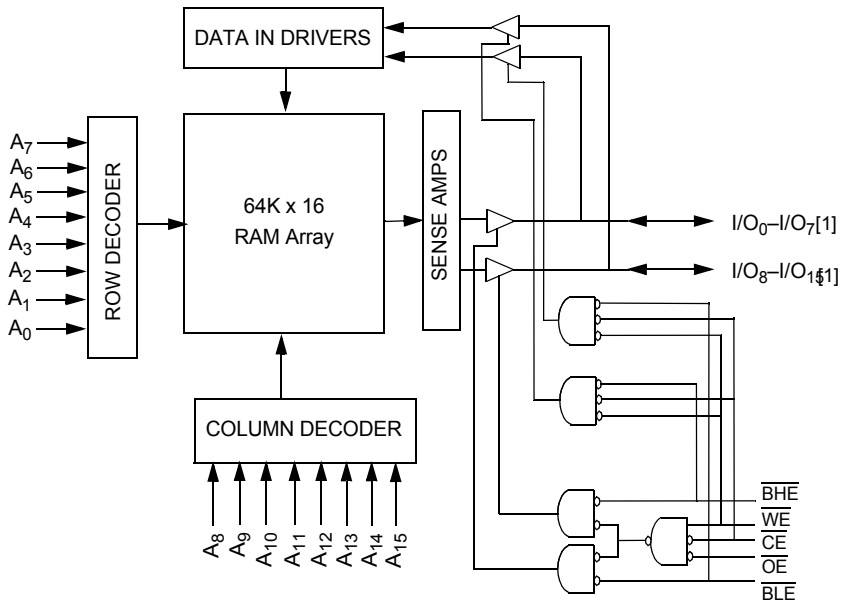
Writing to the device is accomplished by taking Chip Enable ($\overline{CE}$) and Write Enable ($\overline{WE}$) inputs LOW. If Byte Low Enable ($\overline{BLE}$) is LOW, then data from I/O pins (I/O_1 through I/O_8) [1], is written into the location specified on the address pins (A_0 through A_{15}). If Byte High Enable ($\overline{BHE}$) is LOW, then data from I/O pins (I/O_9 through I/O_{16}) [1] is written into the location specified on the address pins (A_0 through A_{15}).

Reading from the device is accomplished by taking Chip Enable ($\overline{CE}$) and Output Enable ($\overline{OE}$) LOW while forcing the Write Enable ($\overline{WE}$) HIGH. If Byte Low Enable ($\overline{BLE}$) is LOW, then data from the memory location specified by the address pins appear on I/O_1 to I/O_8 [1]. If Byte High Enable ($\overline{BHE}$) is LOW, then data from memory appears on I/O_9 to I/O_{16} [1]. For more information, see the Truth Table on page 11 for a complete description of Read and Write modes.

The input and output pins (I/O_1 through I/O_{16}) are placed in a high impedance state when the device is deselected ($\overline{CE}$ HIGH), the outputs are disabled ($\overline{OE}$ HIGH), the $\overline{BHE}$ and $\overline{BLE}$ are disabled ($\overline{BHE}$, $\overline{BLE}$ HIGH), or during a write operation ($\overline{CE}$ LOW and $\overline{WE}$ LOW).

For a complete list of related documentation, click here.

Logic Block Diagram



Note
1. I/O_1–I/O_{16} for SOJ/TSOP and I/O_0–I/O_{15} for BGA packages.

Contents

Selection Guide

Description		-10	-12	Unit
Maximum Access Time		10	12	ns
Maximum Operating Current	Automotive-A	90	–	mA
	Automotive-E	–	90	mA
Maximum CMOS Standby Current	Automotive-A	5	–	mA
	Automotive-E	–	10	mA

Pin Configuration

Figure 1. 44-pin SOJ/TSOP II pinout [2]

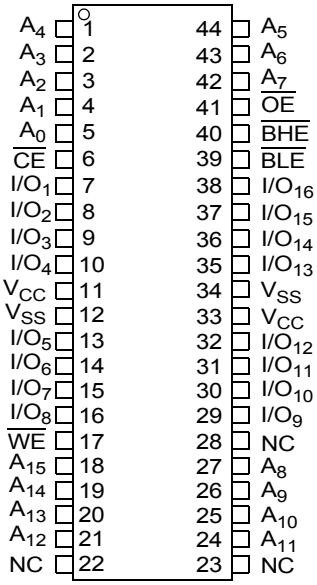
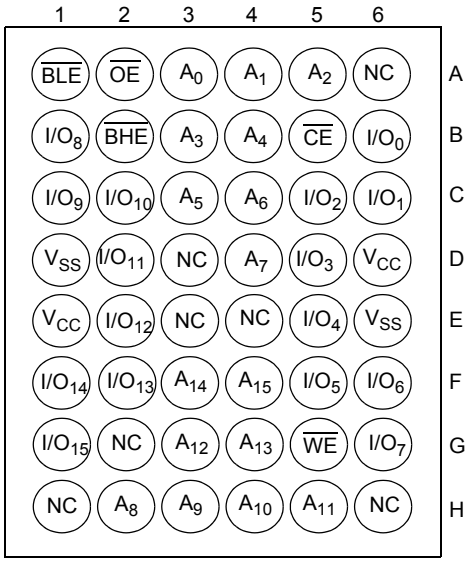


Figure 2. 48-ball FBGA pinout [2]



Note
2. NC pins are not connected on the die.

Pin Definitions

Pin Name	SOJ, TSOP Pin Number	BGA Pin Number	I/O Type	Description
A_0–A_{15}	1–5, 18–21, 24–27, 42–44	A3, A4, A5, B3, B4, C3, C4, D4, H2, H3, H4, H5, G3, G4, F3, F4	Input	**Address Inputs.** Used to select one of the address locations.
I/O_1–I/O_{16} [3]	7–10, 13–16, 29–32, 35–38	B6, C6, C5, D5, E5, F5, F6, G6, B1, C1, C2, D2, E2, F2, F1, G1	Input or Output	**Bidirectional Data I/O lines**. Used as input or output lines depending on operation.
NC	22, 23, 28	A6, D3, E3, E4, G2, H1, H6	No Connect	**No Connects**. Not connected to the die.
$\overline{WE}$	17	G5	Input or Control	**Write Enable Input, Active LOW**. When selected LOW, a write is conducted. When deselected HIGH, a read is conducted.
$\overline{CE}$	6	B5	Input or Control	**Chip Enable Input, Active LOW**. When LOW, selects the chip. When HIGH, deselects the chip.
$\overline{BHE}$, $\overline{BLE}$	40, 39	B2, A1	Input or Control	**Byte Write Select Inputs, Active LOW**. $\overline{BHE}$ controls I/O_{16}–I/O_9 [3], $\overline{BLE}$ controls I/O_8–I/O_1 [3].
$\overline{OE}$	41	A2	Input or Control	**Output Enable, Active LOW**. Controls the direction of the I/O pins. When LOW, the I/O pins are allowed to behave as outputs. When deasserted HIGH, the I/O pins are tristated and act as input data pins.
V_{SS}	12, 34	D1, E6	Ground	**Ground for the Device**. Connected to ground of the system.
V_{CC}	11, 33	D6, E1	Power Supply	**Power Supply Inputs to the Device.**

Note
3. I/O_1–I/O_{16} for SOJ/TSOP and I/O_0–I/O_{15} for BGA packages.

Maximum Ratings

Exceeding maximum ratings may impair the useful life of the device. These user guidelines are not tested.

Storage Temperature ..... –65 °C to +150 °C

Ambient Temperature with Power Applied ..... –55 °C to +125 °C

Supply Voltage on V_{CC} Relative to GND [4] .....–0.5 V to +4.6 V

DC Voltage Applied to Outputs in High Z State [4] ..... –0.5 V to V_{CC} + 0.5 V

DC Input Voltage [4] ..... –0.5 V to V_{CC} + 0.5 V

Current into Outputs (LOW) ..... 20 mA

Static Discharge Voltage (MIL-STD-883, Method 3015) ..... > 2001 V

Latch Up Current ..... > 200 mA

Operating Range

Range	Ambient Temperature (T_A)	V_{CC}
Automotive-A	–40 °C to +85 °C	3.3 V ± 10%
Automotive-E	–40 °C to +125 °C	

Electrical Characteristics

Over the Operating Range

Parameter	Description	Test Conditions		-10		-12		Unit
				Min	Max	Min	Max	
V_{OH}	Output HIGH Voltage	V_{CC} = Min, I_{OH} = –4.0 mA		2.4	–	2.4	–	V
V_{OL}	Output LOW Voltage	V_{CC} = Min, I_{OL} = 8.0 mA		–	0.4	–	0.4	V
V_{IH}	Input HIGH Voltage			2.0	V_{CC} + 0.3	2.0	V_{CC} + 0.3	V
V_{IL}	Input LOW Voltage[4]			–0.3	0.8	–0.3	0.8	V
I_{IX}	Input Leakage Current	GND ≤ V_I ≤ V_{CC}	Automotive-A	–1	+1	–	–	µA
			Automotive-E	–	–	–12	+12	
I/O_Z	Output Leakage Current	GND ≤ V_I ≤ V_{CC}, Output disabled	Automotive-A	–1	+1	–	–	µA
			Automotive-E	–	–	–12	+12	
I_{CC}	V_{CC} Operating Supply Current	V_{CC} = Max, I_{OUT} = 0 mA, f = f_{MAX} = $1/t_{RC}$	Automotive-A	–	90	–	–	mA
			Automotive-E	–	–	–	90	
I_{SB1}	Automatic CE Power Down Current —TTL Inputs	Max V_{CC}, CE ≥ V_{IH} V_{IN} ≥ V_{IH} or V_{IN} ≤ V_{IL}, f = f_{MAX}	Automotive-A	–	15	–	–	mA
			Automotive-E	–	–	–	20	
I_{SB2}	Automatic CE Power Down Current — CMOS Inputs	Max V_{CC}, CE ≥ V_{CC} – 0.3 V, V_{IN} ≥ V_{CC} – 0.3 V, or V_{IN} ≤ 0.3 V, f = 0	Automotive-A	–	5	–	–	mA
			Automotive-E	–	–	–	10	

Note

4. V_{IL} (min) = –2.0 V and V_{IH}(max) = V_{CC} + 0.5 V for pulse durations of less than 20 ns.

Capacitance

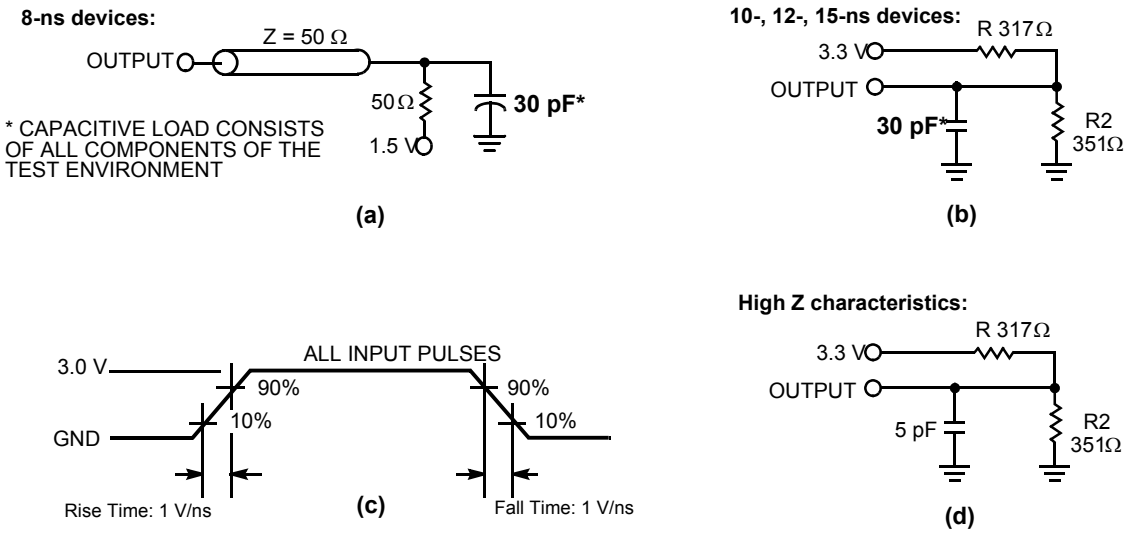
Parameter [5]	Description	Test Conditions	Max	Unit
C_{IN}	Input capacitance	T_A = 25 °C, f = 1 MHz, V_{CC} = 3.3 V	8	pF
C_{OUT}	Output capacitance		8	pF

Thermal Resistance

Parameter [5]	Description	Test Conditions	44-pin SOJ	44-pin TSOP II	48-ball FBGA	Unit
Θ_{JA}	Thermal resistance (junction to ambient)	Test conditions follow standard test methods and procedures for measuring thermal impedance, per EIA/JESD51	65.06	76.92	95.32	°C/W
Θ_{JC}	Thermal resistance (junction to case)		34.21	15.86	10.68	°C/W

AC Test Loads and Waveforms

Figure 3. AC Test Loads and Waveforms [6]



Notes
5. Tested initially and after any design or process changes that may affect these parameters.
6. AC characteristics (except High Z) for all 8-ns parts are tested using the load conditions shown in Figure 3 (a). All other speeds are tested using the Thevenin load shown in Figure 3 (b). High Z characteristics are tested for all speeds using the test load shown in Figure 3 (d).

Switching Characteristics

Over the Operating Range

Parameter [7]	Description	-10		-12		Unit
		Min	Max	Min	Max	
Read Cycle						
t_{power} [8]	V_{CC}(Typical) to the First Access	100	–	100	–	µs
t_{RC}	Read Cycle Time	10	–	12	–	ns
t_{AA}	Address to Data Valid	–	10	–	12	ns
t_{OHA}	Data Hold from Address Change	3	–	3	–	ns
t_{ACE}	$\overline{CE}$ LOW to Data Valid	–	10	–	12	ns
t_{DOE}	$\overline{OE}$ LOW to Data Valid	–	5	–	6	ns
t_{LZOE}	$\overline{OE}$ LOW to Low Z [9]	0	–	0	–	ns
t_{HZOE}	$\overline{OE}$ HIGH to High Z [9, 10]	–	5	–	6	ns
t_{LZCE}	$\overline{CE}$ LOW to Low Z [9]	3	–	3	–	ns
t_{HZCE}	$\overline{CE}$ HIGH to High Z [9, 10]	–	5	–	6	ns
t_{PU} [11]	$\overline{CE}$ LOW to Power Up	0	–	0	–	ns
t_{PD} [11]	$\overline{CE}$ HIGH to Power Down	–	10	–	12	ns
t_{DBE}	Byte Enable to Data Valid	–	5	–	6	ns
t_{LZBE}	Byte Enable to Low Z	0	–	0	–	ns
t_{HZBE}	Byte Disable to High Z	–	5	–	6	ns
Write Cycle [12, 13]						
t_{WC}	Write Cycle Time	10	–	12	–	ns
t_{SCE}	$\overline{CE}$ LOW to Write End	8	–	9	–	ns
t_{AW}	Address Setup to Write End	8	–	9	–	ns
t_{HA}	Address Hold from Write End	0	–	0	–	ns
t_{SA}	Address Setup to Write Start	0	–	0	–	ns
t_{PWE}	$\overline{WE}$ Pulse Width	7	–	8	–	ns
t_{SD}	Data Setup to Write End	5	–	6	–	ns
t_{HD}	Data Hold from Write End	0	–	0	–	ns
t_{LZWE}	$\overline{WE}$ HIGH to Low Z [9]	3	–	3	–	ns
t_{HZWE}	$\overline{WE}$ LOW to High Z [9, 10]	–	5	–	6	ns
t_{BW}	Byte Enable to End of Write	7	–	8	–	ns

Notes

7. Test conditions assume signal transition time of 3 ns or less, timing reference levels of 1.5 V, and input pulse levels of 0 to 3.0 V.
8. t_{POWER} gives the minimum amount of time that the power supply is at typical V_{CC} values until the first memory access is performed.
9. At any temperature and voltage condition, t_{HZCE} is less than t_{LZCE}, t_{HZOE} is less than t_{LZOE}, and t_{HZWE} is less than t_{LZWE} for any given device.
10. t_{HZOE}, t_{HZBE}, t_{HZCE}, and t_{HZWE} are specified with a load capacitance of 5 pF as in part (d) of Figure 3 on page 6. Transition is measured ±500 mV from steady state voltage.
11. This parameter is guaranteed by design and is not tested.
12. The internal write time of the memory is defined by the overlap of $\overline{WE}$, $\overline{CE}$, and $\overline{BHE}$/$\overline{BLE}$ LOW. All Signals must be ACTIVE to initiate a write and any of these signals can terminate a write by going INACTIVE.The data input setup and hold timing must be referenced to the edge of the signal that terminates the write.
13. The minimum write cycle pulse width for Write Cycle No. 3 ($\overline{WE}$ controlled, $\overline{OE}$ LOW) should be equal to the sum of t_{SD} and t_{HZWE}.

Switching Waveforms

Figure 4. Read Cycle No. 1 (Address Transition Controlled) [14, 15]

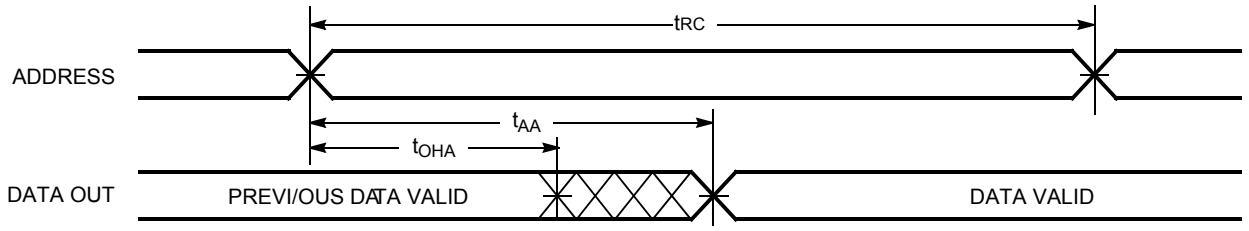
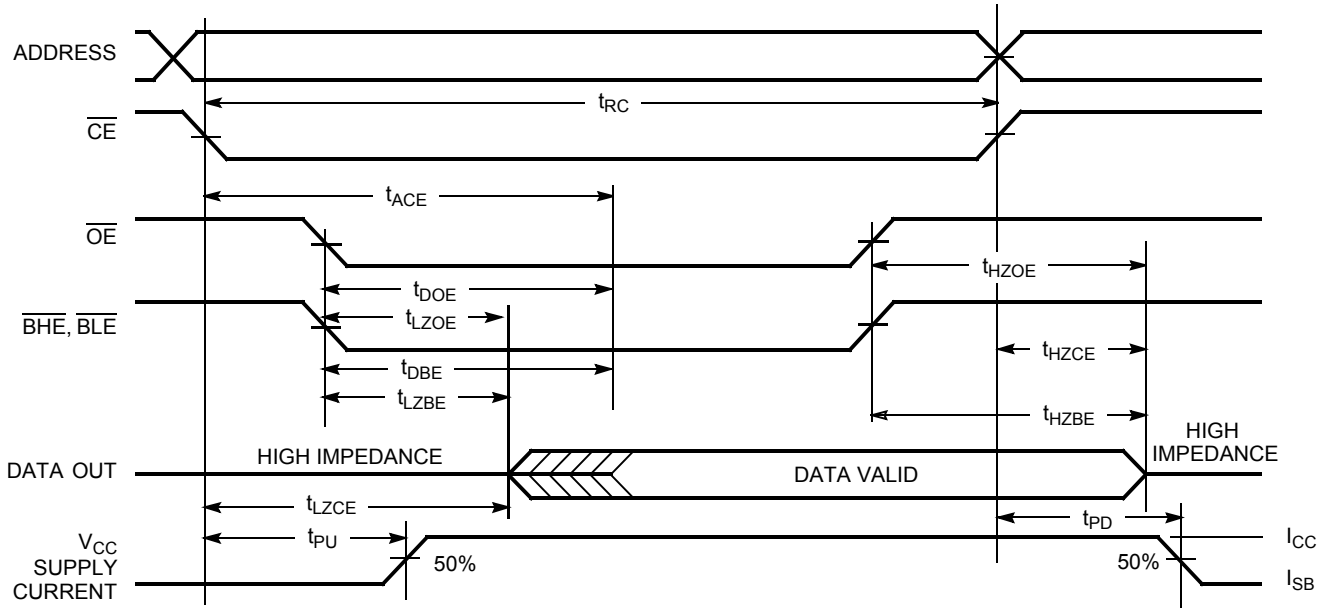


Figure 5. Read Cycle No. 2 (OE Controlled) [15, 16]



Notes
14. Device is continuously selected. $\overline{OE}$, $\overline{CE}$, $\overline{BHE}$, and/or $\overline{BLE}$ = V_{IL}.
15. $\overline{WE}$ is HIGH for read cycle.
16. Address valid prior to or coincident with $\overline{CE}$ transition LOW.

Switching Waveforms *(continued)*

Figure 6. Write Cycle No. 1 ($\overline{CE}$ Controlled) [17, 18]

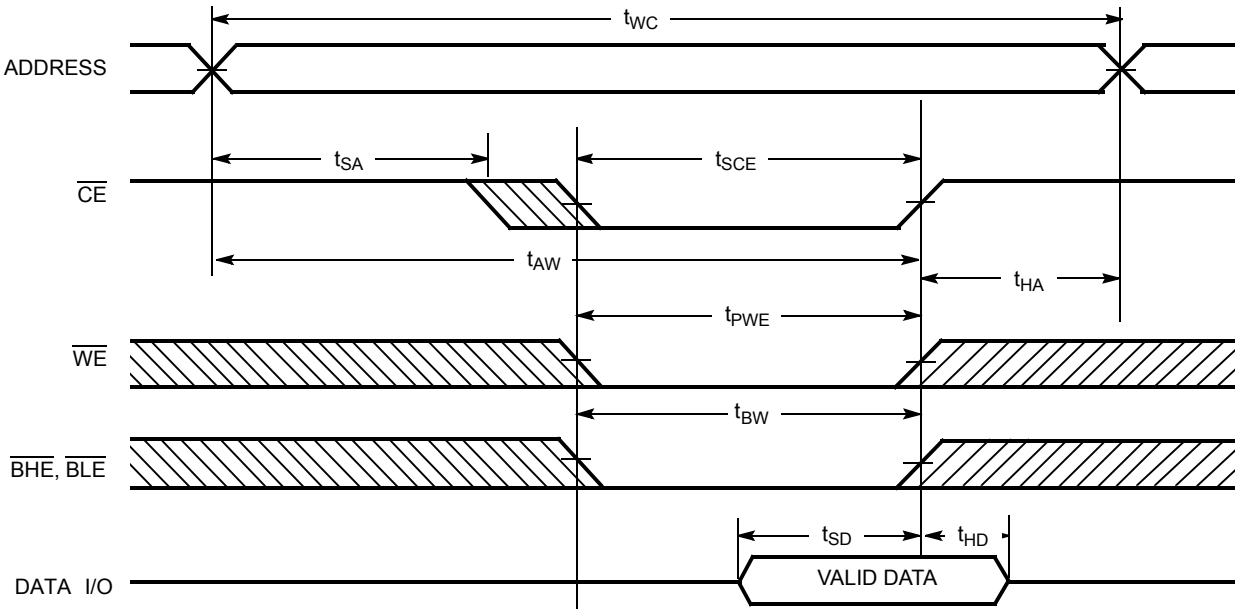
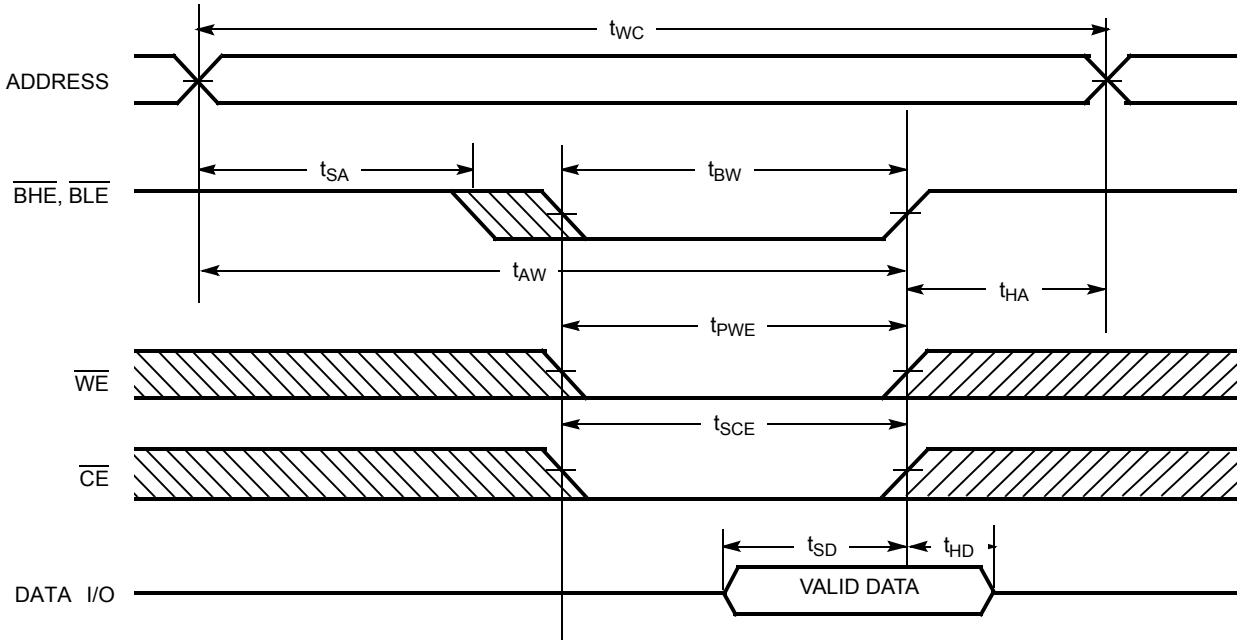


Figure 7. Write Cycle No. 2 ($\overline{BLE}$ or $\overline{BHE}$ Controlled)



Notes
17. Data I/O is high impedance if $\overline{OE}$, $\overline{BHE}$, and/or $\overline{BLE}$ = V_{IH}.
18. If $\overline{CE}$ goes HIGH simultaneously with $\overline{WE}$ going HIGH, the output remains in a high impedance state.

Switching Waveforms *(continued)*

Figure 8. Write Cycle No. 3 ($\overline{WE}$ Controlled)

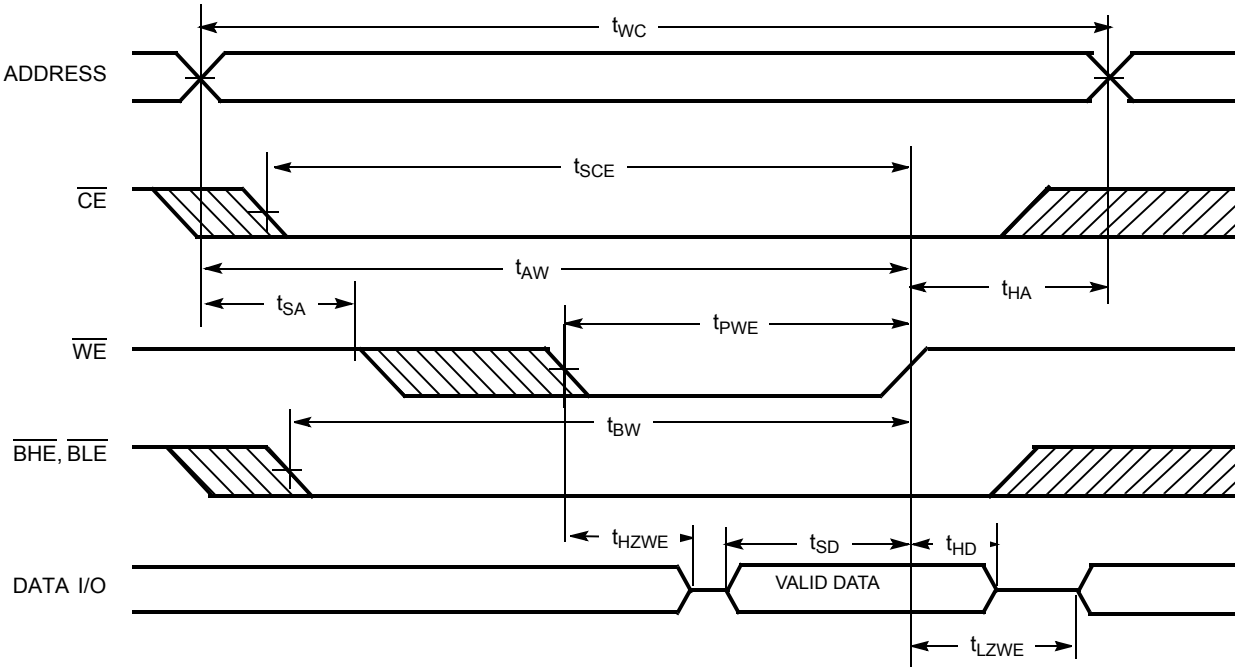
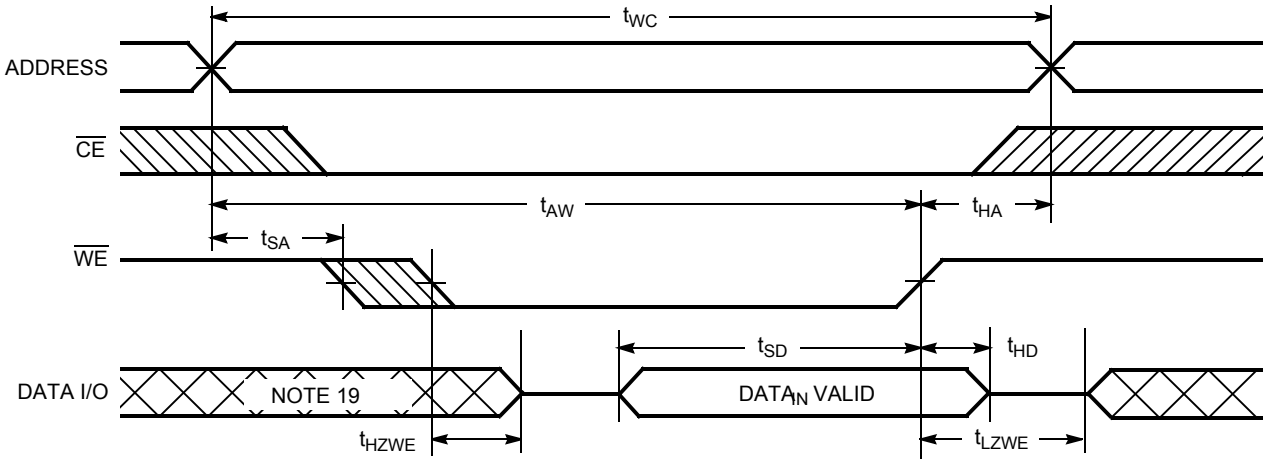


Figure 9. Write Cycle No. 3 ($\overline{WE}$ Controlled, $\overline{OE}$ LOW) [19]



Notes

19. The minimum write cycle pulse width should be equal to the sum of t_{SD} and t_{HZWE}.

Truth Table

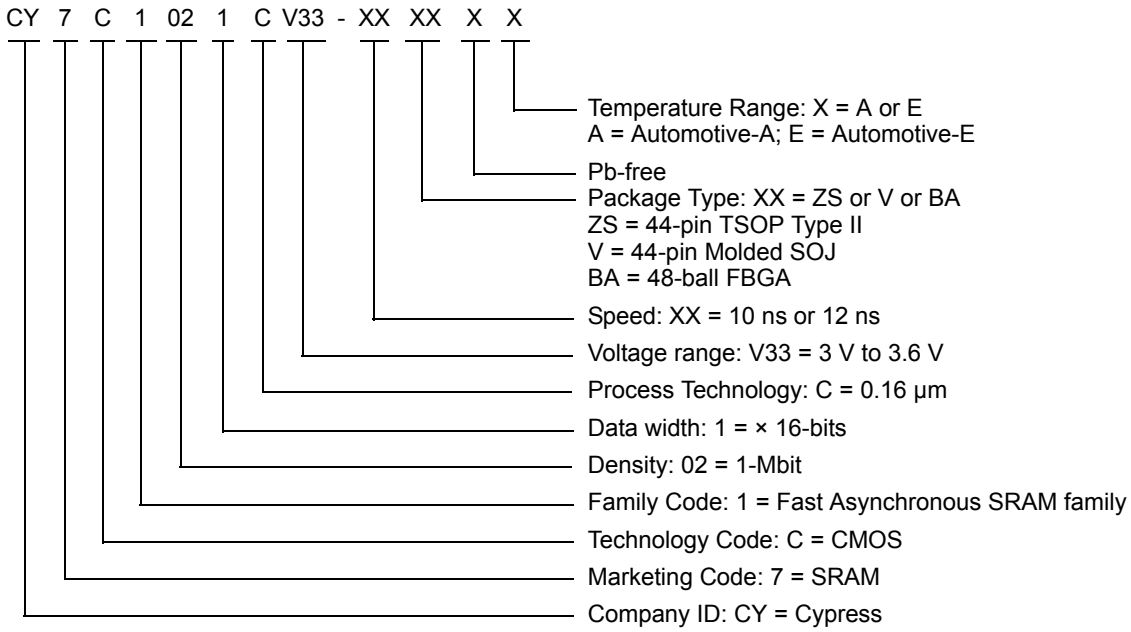
$\overline{CE}$	$\overline{OE}$	$\overline{WE}$	$\overline{BLE}$	$\overline{BHE}$	$I/O_1–I/O_8$ [20]	$I/O_9–I/O_{16}$ [20]	Mode	Power
H	X	X	X	X	High Z	High Z	Power Down	Standby (I_{SB})
L	L	H	L	L	Data Out	Data Out	Read – All Bits	Active (I_{CC})
			L	H	Data Out	High Z	Read – Lower Bits Only	Active (I_{CC})
			H	L	High Z	Data Out	Read – Upper Bits Only	Active (I_{CC})
L	X	L	L	L	Data In	Data In	Write – All Bits	Active (I_{CC})
			L	H	Data In	High Z	Write – Lower Bits Only	Active (I_{CC})
			H	L	High Z	Data In	Write – Upper Bits Only	Active (I_{CC})
L	H	H	X	X	High Z	High Z	Selected, Outputs Disabled	Active (I_{CC})
L	X	X	H	H	High Z	High Z	Selected, Outputs Disabled	Active (I_{CC})

Note
20. $I/O_1–I/O_{16}$ for SOJ/TSOP and $I/O_0–I/O_{15}$ for BGA packages.

Ordering Information

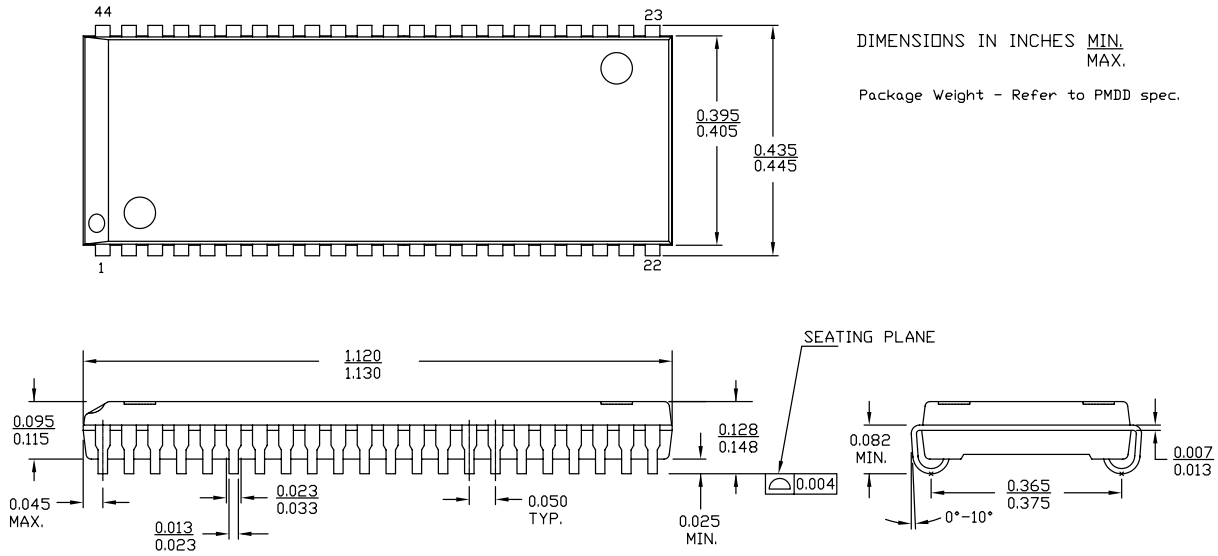
Speed (ns)	Ordering Code	Package Diagram	Package Type	Operating Range
10	CY7C1021CV33-10ZSXA	51-85087	44-pin TSOP Type II (Pb-free)	Automotive-A
12	CY7C1021CV33-12VXE	51-85082	44-pin (400-Mil) Molded SOJ (Pb-free)	Automotive-E
	CY7C1021CV33-12ZSXE	51-85087	44-pin TSOP Type II (Pb-free)	

Ordering Code Definitions



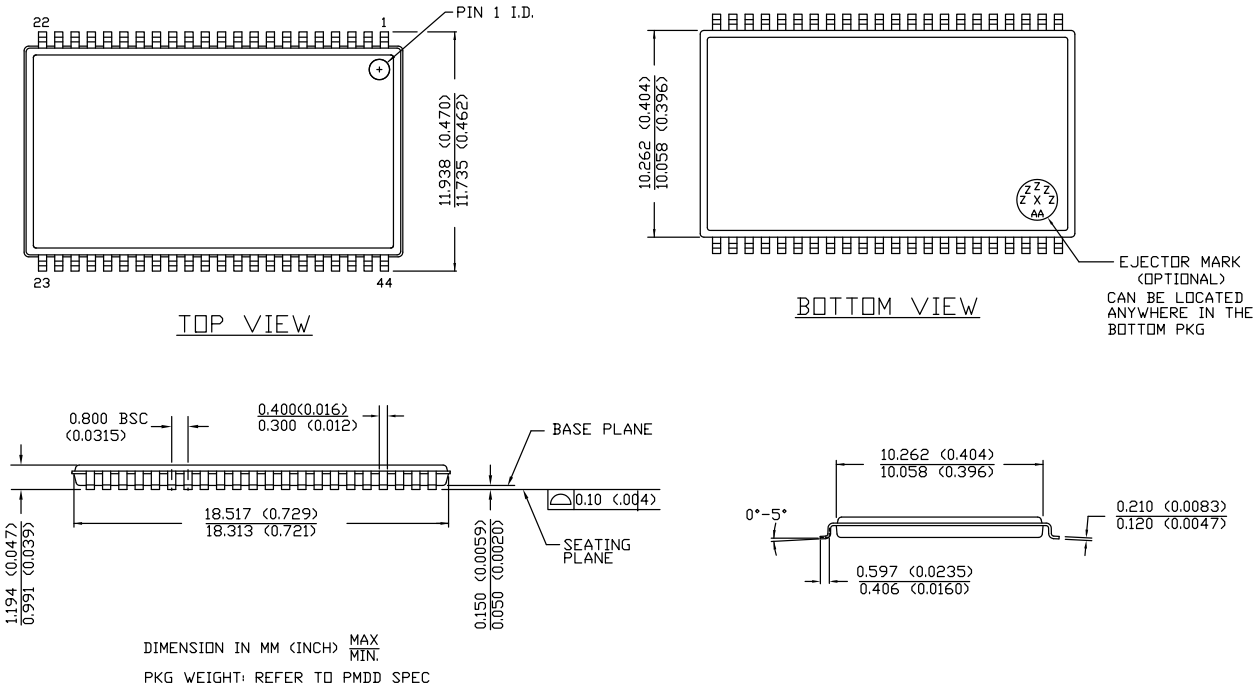
Package Diagrams

Figure 10. 44-pin SOJ (400 Mils) V44.4 Package Outline, 51-85082



Package Diagrams *(continued)*

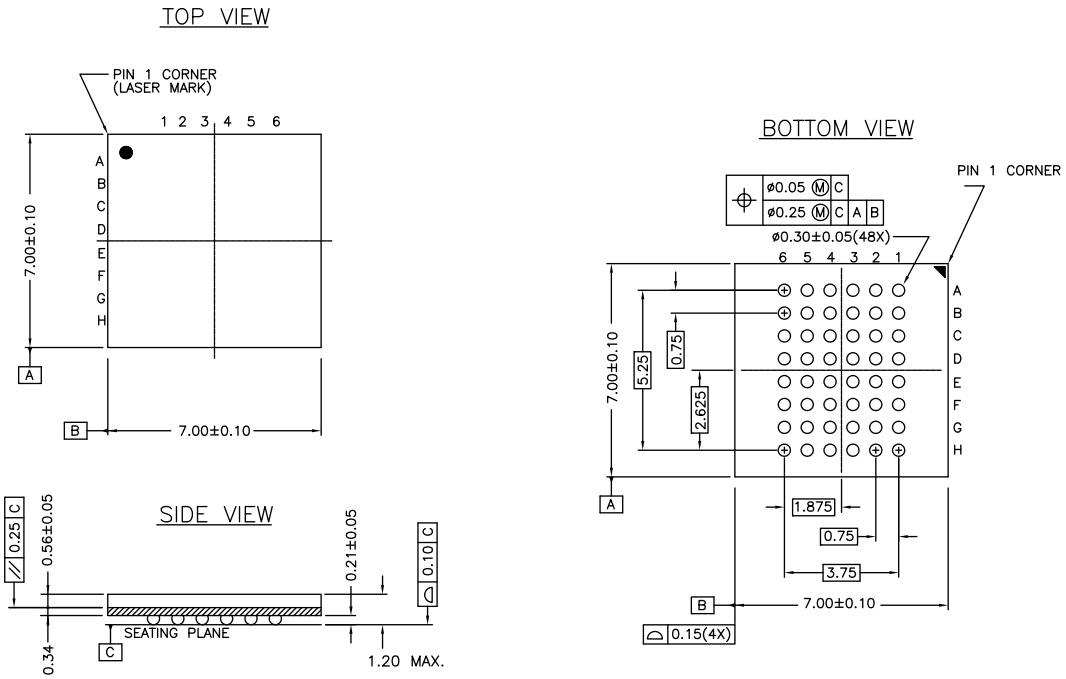
Figure 11. 44-pin TSOP Z44-II Package Outline, 51-85087



51-85087 *E

Package Diagrams *(continued)*

Figure 12. 48-ball FBGA (7 × 7 × 1.2 mm) BA48 Package Outline, 51-85096



51-85096 *J

Acronyms

Acronym	Description
BGA	ball grid array
$\overline{CE}$	chip enable
CMOS	complementary metal oxide semiconductor
FBGA	fine-pitch ball grid array
I/O	input/output
$\overline{OE}$	output enable
SOJ	small outline J-lead
SRAM	static random access memory
TQFP	thin quad flat pack
TSOP	thin small-outline package
TTL	transistor-transistor logic
$\overline{WE}$	write enable

Document Conventions

Units of Measure

Symbol	Unit of Measure
°C	degree Celsius
µA	microampere
µs	microsecond
mA	milliampere
mm	millimeter
mW	milliwatt
MHz	megahertz
ns	nanosecond
%	percent
pF	picofarad
V	volt
W	watt

Document History Page

Document Title: CY7C1021CV33 Automotive, 1-Mbit (64 K × 16) Static RAM Document Number: 38-05132				
Rev.	**ECN No.**	**Submission Date**	**Orig. of Change**	**Description of Change**
**	109472	12/06/01	HGK	New data sheet
*A	115044	05/08/02	HGK	Ram7 version C4K x 16 Async Removed “Preliminary”
*B	115808	06/25/02	HGK	I_{SB1} and I_{CC} values changed
*C	120413	10/31/02	DFP	Updated BGA pin E4 to NC
*D	238454	See ECN	RKF	Added Automotive Specifications to datasheet Added Pb-free devices in the Ordering Information
*E	334398	See ECN	SYT	Added Pb-free on page 9 and 10
*F	493565	See ECN	NXR	Added Automotive-A operating range Corrected typo in the Pin Definition table Changed the description of I_{IX} from Input Load Current to Input Leakage Current in DC Electrical Characteristics table Removed I_{OS} parameter from DC Electrical Characteristics table Updated the ordering information table
*G	563963	See ECN	VKN	Added t_{POWER} specification in the AC Switching Characteristics table Added footnote 8
*H	1390863	See ECN	VKN / AESA	Corrected TSOP II package outline
*I	1891366	See ECN	VKN / AESA	Added -10ZSXA part in the Ordering Information table Updated Ordering Information Table
*J	2880096	02/17/2010	VKN / AESA	Added “CY7C1021CV33-10ZXI” part in the Ordering Information table Updated package diagrams.
*K	2897691	03/23/2010	RAME	Updated Ordering Information Updated Package Diagrams
*L	3089939	11/18/2010	PRAS	Removed inactive parts from Ordering Information.
*M	3127893	01/04/2011	HMLA	Added Ordering Code Definitions. Added Acronyms and Units of Measure. Updated in new template.
*N	3272897	06/07/2011	HMLA	Updated Features (Removed the information associated with speed bins -8 and also the information associated with Commercial and Industrial parts.) Updated Functional Description (Removed “For best practice recommendations, refer to the Cypress application note AN1064, SRAM System Guidelines.”). Updated Selection Guide (Removed the information associated with Commercial and Industrial parts.) Updated Operating Range (Removed the information associated with Commercial and Industrial parts.) Updated Electrical Characteristics (Removed the information associated with Commercial and Industrial parts.) Updated Package Diagrams.
*O	3400821	10/10/2011	HMLA	Updated Operating Range (Straddled both rows under V_{CC} column so that the same condition is applicable for both Automotive-A and Automotive-E ranges). Updated Ordering Information (Removed the Note “The 44-pin TSOP II package containing the Automotive grade device is designated as “ZS”, while the same package containing the Commercial/Industrial grade device is “Z”.” below the Ordering Information table since Commercial/Industrial grade devices are not offered in this data sheet). Updated Package Diagrams.

Document History Page *(continued)*

Document Title: CY7C1021CV33 Automotive, 1-Mbit (64 K × 16) Static RAM Document Number: 38-05132				
Rev.	**ECN No.**	**Submission Date**	**Orig. of Change**	**Description of Change**
*P	3897056	02/13/2013	MEMJ	Updated Document Title to read as “CY7C1021CV33 Automotive, 1-Mbit (64 K × 16) Static RAM”. Updated Functional Description: Added Note 1 and referred the same note in I/O_0–I/O_7 and I/O_8–I/O_{15}. Updated Logic Block Diagram: Added Note 1 and referred the same note in I/O_0–I/O_7 and I/O_8–I/O_{15}. Updated Pin Definitions: Referred Note 3 in description of $\overline{BHE}$, $\overline{BLE}$ pin. Updated Switching Characteristics: Updated Note 12 only. Updated Switching Waveforms: Updated Figure 6, Figure 7, Figure 8. Updated Truth Table: Added Note 20 and referred the same note in I/O_1–I/O_8 and I/O_9–I/O_{16} columns. Updated Package Diagrams: spec 51-85082 – Changed revision from *D to *E. spec 51-85087 – Changed revision from *D to *E.
*Q	4585000	11/24/2014	MEMJ	Added related documentation hyperlink in page 1. Updated Figure 12 in Package Diagrams (spec 51-85096 *I to *J). Added Note 13 in Switching Characteristics. Added note reference 13 in the Switching Characteristics table. Added Note 19 in Switching Waveforms. Added note reference 19 in Figure 9.

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