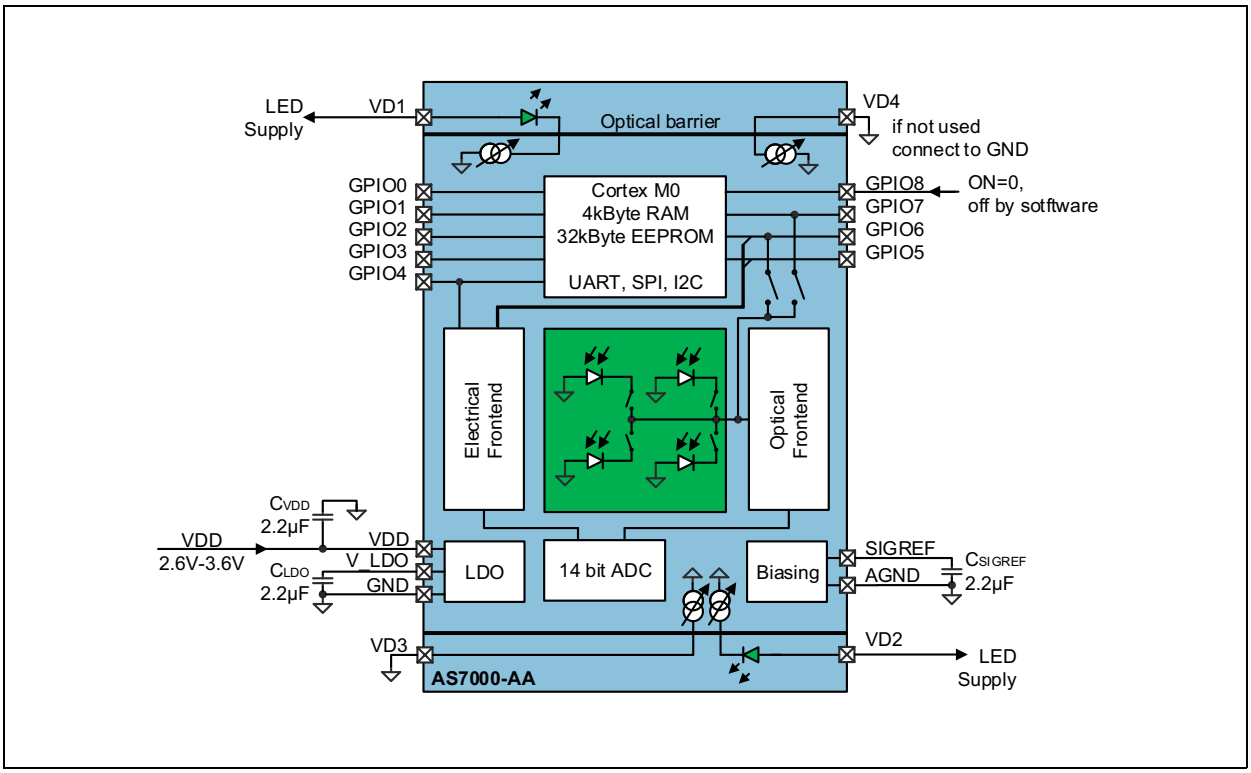
Block Diagram

The functional blocks of this device are shown below:

Figure 2:
Application Schematic AS7000-AA



Pin Assignments

Figure 3:
Optical Module Pinout (Top View) – AS7000-AA

Optical Module Pinout:
This drawing is not to scale

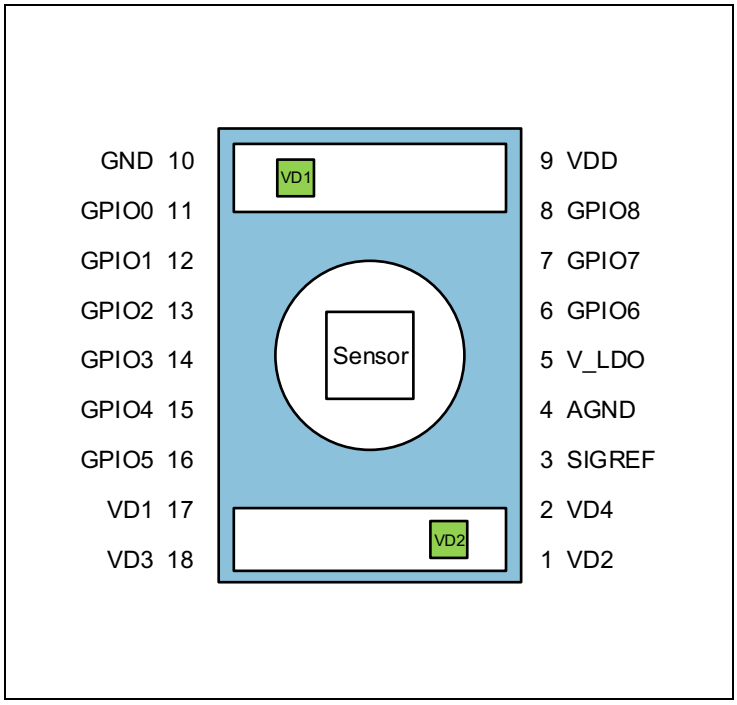


Figure 4:
Pin Description

Pin Number	Pin Name	Description
1	VD2	Supply voltage for LED D2 – connect unused current sinks to GND
2	VD4	Supply voltage for LED D4 – connect unused current sinks to GND
3	SIGREF	Analog reference output. Connect 2.2µF capacitor to GND (e.g. 0402 sized capacitor GRM153R60J225ME95 from Murata – needs to have >1µF specified for 1.0V voltage bias); do not load externally The typical operating voltage on this pin is 0.6V (sigref_en=1)
4	AGND	Analog ground. Connect to low noise GND
5	V_LDO	1.9V output voltage. Connect 2.2µF capacitor to GND (e.g. 0402 sized capacitor GRM153R60J225ME95 from Murata – needs to have >1µF with 1.0V voltage bias); do not load externally
6	GPIO6	General purpose input/output
7	GPIO7	General purpose input/output
8	GPIO8	General purpose input/output
9	VDD	Supply voltage.
10	GND	Power supply ground. All voltages are referenced to GND.

Pin Number	Pin Name	Description
11	GPIO0	General purpose input/output
12	GPIO1	General purpose input/output
13	GPIO2	General purpose input/output
14	GPIO3	General purpose input/output
15	GPIO4	General purpose input/output
16	GPIO5	General purpose input/output
17	VD1	Supply voltage for LED D1 – connect unused current sinks to GND
18	VD3	Supply voltage for LED D3 – connect unused current sinks to GND

Absolute Maximum Ratings

Stresses beyond those listed may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated in Electrical Characteristics is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Figure 5:
Absolute Maximum Ratings(1)

Symbol	Parameter	Min	Max	Units	Comments
Electrical Parameters					
VDD	Supply voltage to ground		3.63V	V	
V_LDO	Supply voltage to ground		1.98V max. VDD+0.3V	V	
V_{IN}	Input pin voltage to ground, all pins except VD1/VD2/VD3/VD4	-0.3	VDD+0.3V max. 3.8V	V	
$V_{IN-VD1-4}$	Input pin voltage to ground, pins VD1/VD2/VD3/VD4	-0.3	5.5	V	
V_{INLDO}	Input pin voltage to ground, pin SIGREF	-0.3	V_LDO+0.3V max. 1.98V	V	
I_{SCR}	Input current (latch-up immunity)	-100	100	mA	JEDEC JESD78
Electrostatic Discharge					
ESD_{HBM}	All pins except VD1/VD2/VD3 and VD4	±1.0		kV	Electrostatic discharge HBM: JEDEC JESD22-A114F
	Pins VD1/VD2/VD3 and VD4	±350		V	

Symbol	Parameter	Min	Max	Units	Comments
Temperature Ranges and Storage Conditions					
T_{AMB}	Operating temperature	-30	70	°C	
T_{STRG}	Storage temperature range	-40	85	°C	
T_{BODY}	Package body temperature		260	°C	IPC/JEDEC J-STD-020 The reflow peak soldering temperature (body temperature) is specified according to IPC/JEDEC J-STD-020 "Moisture/Reflow Sensitivity Classification for Non-hermetic Solid State Surface Mount Devices."
RH_{NC}	Relative humidity non-condensing	5	85	%	
MSL	Moisture sensitivity level	3			Maximum floor life time of 168h

Note(s):

1. All optical customer designs shall be reviewed by **ams** before production.

Electrical Characteristics

VDD=2.6 to 3.6V, typ. values are at T_{AMB}=25°C (unless otherwise specified).

All limits are guaranteed. The parameters with min and max values are guaranteed with production tests or SQC (Statistical Quality Control) methods.

Figure 6:
Operating Conditions

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
VDD	Supply voltage		2.6	3.3	3.6	V
VLED	LED Supply voltage	VD1, VD2, VD3, VD4 if a LED is used			5.0	V
V_{LDO}	LDO voltage, generated by AS7000	Pin V_LDO		1.9		V
T_{AMB}	Operating free-air temperature		–30		70	°C
IDD	Supply current	CPU + EEPROM running at 16MHz; from 1.8V supply; all periphery blocks off		1.4		mA
		CPU in sleep mode, 16MHz oscillator running; all periphery blocks off		360		µA
		ADC 14bit; only during conversion		2		mA
		Photodiode amplifier and Optical front end		430		µA
		Electrical front end		180		µA
		LED current sink per channel 25mA range		210		µA
		LED current sink per channel 50mA and 100mA range		340		µA
		Deep sleep mode (1), (2) 512Hz oscillator running, LDO operating, processor powered		25		µA
		Power down (3) GPIO8=VDD.		0.8		µA
VOL	GPIO0-8 output low voltage	With 3 mA load With 6 mA load	0 0		0.4 0.8	V
VOH	GPIO0-8 output high voltage	With 6 mA load, VDD>3.0V	2.4		VDD	V

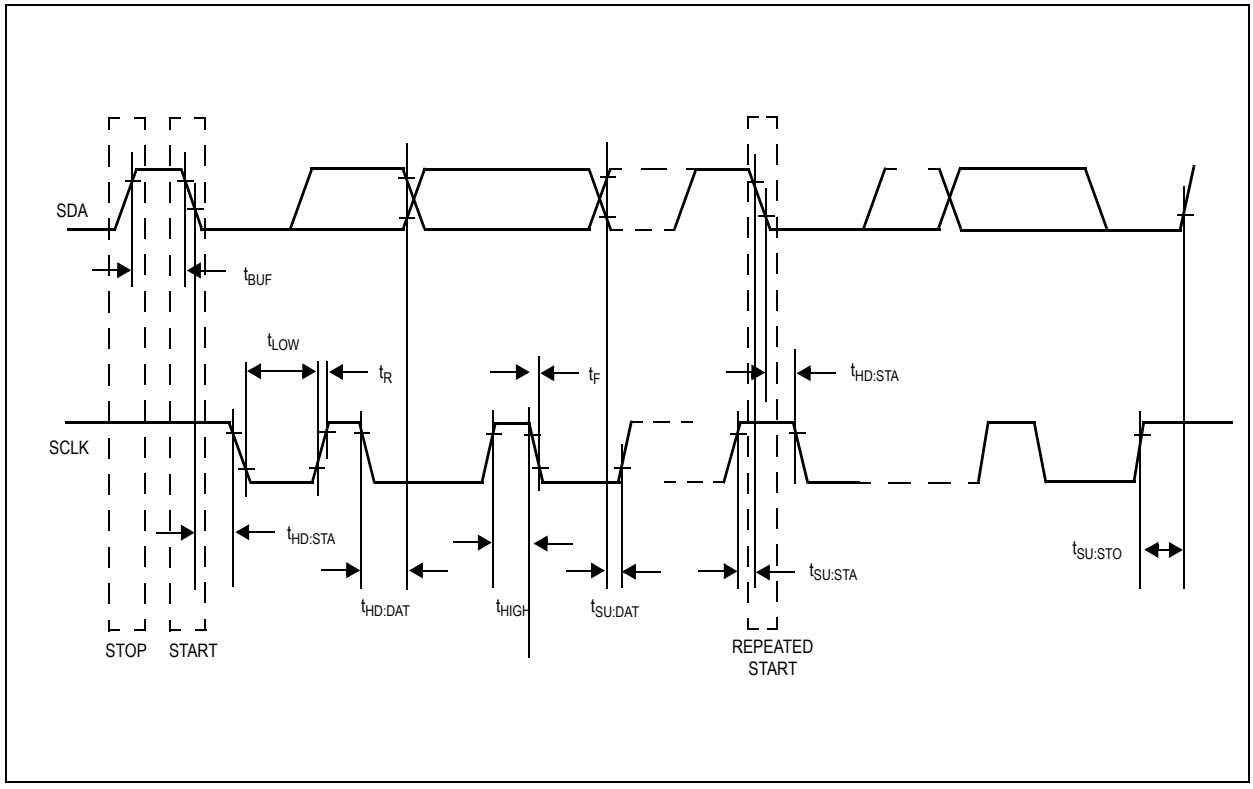
Symbol	Parameter	Conditions	Min	Typ	Max	Unit
VIH	GPIO0-8 input high voltage		1.25			V
VIL	GPIO0-8 input low voltage				0.54	V
R_{PULLUP}	Pullup Resistor to VDD	On GPIO0…8 if bit gpioX_pd=1 where X=0…8		75		kΩ
$R_{PULLDOWN}$	Pulldown Resistor to GND	On GPIO0…8 if bit gpioX_pd=2 where X=0…8		75		kΩ
ILEAK1	GPIO0-8		–1		1	µA
ILEAK2	VD1-4 pins	At 5.0 V, T_{AMB}=25°C			2	µA
E_f16M	Tolerance of internal 16MHz oscillator	T_{AMB}>0°C	-2		+2	%
E_f3k2	Tolerance of internal 512Hz oscillator		-35		+25	%
EEPROM						
n_{CYCLES}	Number of write cycles		100			cycles
$t_{RETENTION}$	Data retention time	At maximum 65°C			10	years
I²C Mode Timings (SCL / SDA Programmable to GPIO Pins – See I²C Mode)						
f_{SCLK}	SCL clock frequency		0		400	
t_{BUF}	Bus free time between a STOP and START condition		1.3			kHz
$t_{HD:STA}$	Hold time (repeated) START condition (3)		0.6			µs
t_{LOW}	LOW period of SCL clock		1.3			µs
t_{HIGH}	HIGH period of SCL clock		0.6			µs
$t_{SU:STA}$	Setup time for a repeated START condition		0.6			µs
$t_{HD:DAT}$	Data hold time (4)		0		0.9	µs
$t_{SU:DAT}$	Data Setup Time (5)		100			ns
t_R	Rise time of both SDA and SCL signals		20		300	ns
t_F	Fall time of both SDA and SCL signals		20		300	ns
$t_{SU:STO}$	Setup time for STOP condition		0.6			µs
C_B	Capacitive load for each bus Line	CB — total capacitance of one bus line in pF			400	pF

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$C_{I/O}$	I/O capacitance (SDA, SCL)				10	pF

Note(s):

1. Deep sleep mode. Use **ams** SDK (software development kit) to enter deep sleep, wakeup with low on GPIO8 pin (if gpio8_wakeup_en=1) or high on GPIO7 (if gpio7_wakeup_en=1) or 512Hz oscillator sleep_timer.
2. GPIO0-8 configured to draw minimum current (software dependent).
3. Power down mode. Entered by setting enter_powerdown=1; No oscillator running. Wakeup with low on GPIO8 pin (always) or high on GPIO7 (if gpio7_wakeup_en=1).
4. A device must internally provide a hold time of at least 300ns for the SDA signal (referred to the V_{IHMIN} of the SCL signal) to bridge the undefined region of the falling edge of SCL.
5. A fast-mode device can be used in a standard-mode system, but the requirement $t_{SU:DAT}$ = to 250ns must then be met. This is automatically the case if the device does not stretch the LOW period of the SCL signal. If such a device does stretch the LOW period of the SCL signal, it must output the next data bit to the SDA line t_R max + $t_{SU:DAT}$ = 1000 + 250 = 1250ns before the SCL line is released.

Figure 7:
I²C Mode Timing Diagram



I²C Mode Timing Diagram: This figure shows the different timings required for I²C communication.

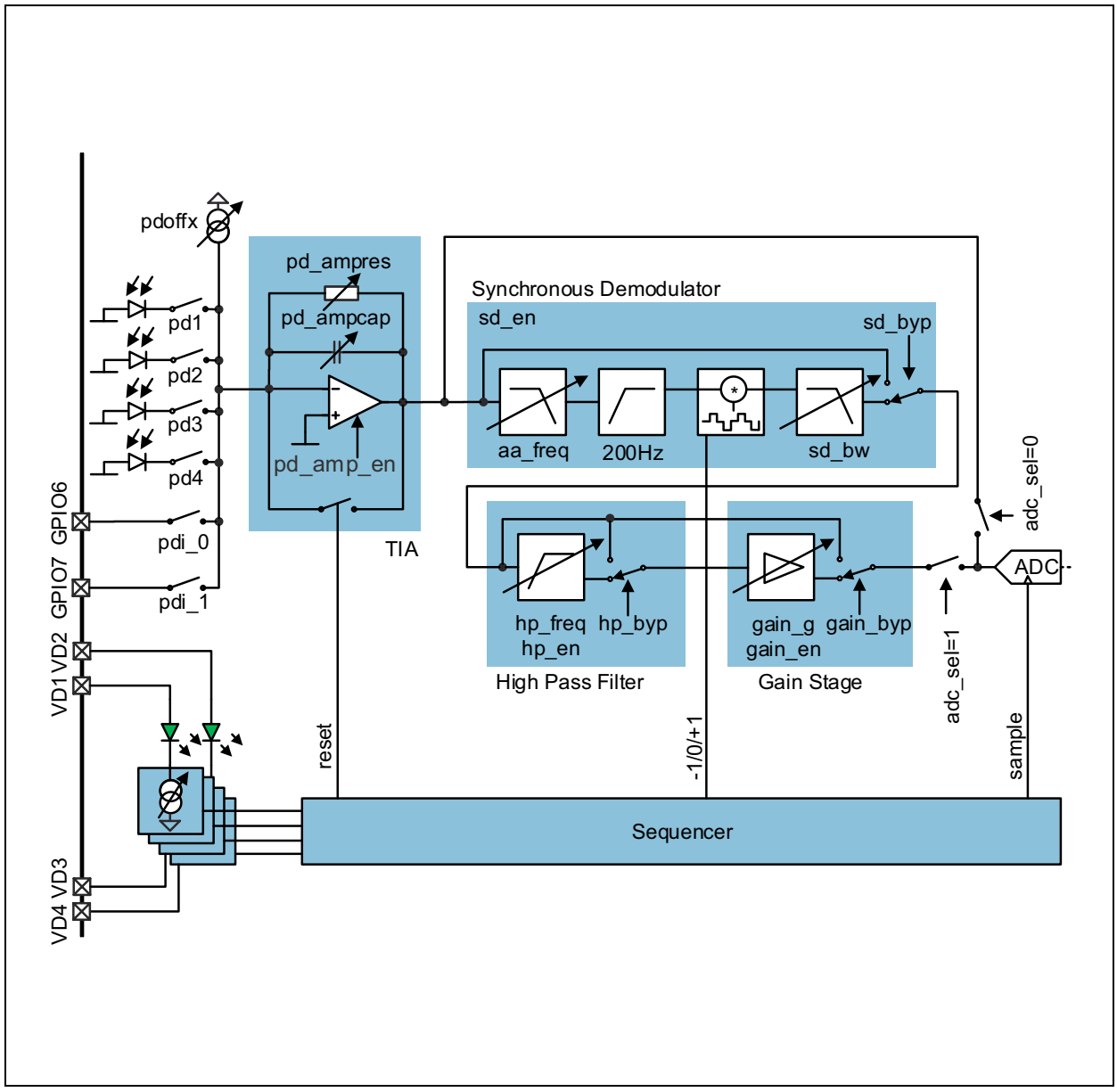
Note(s):

1. SCL / SDA Programmable to GPIO Pins – See I²C Mode.

Detailed Description

Optical Analog Front End

Figure 8:
Optical Analog Front End – AS7000-AA Configuration



Note(s):

1. Dual Green LED Configuration is shown.

The number of LEDs inside the module depends on the application – Figure 8 shows 2 LEDs. If a LED is not populated, the current sink is connected directly to the pin (VD3 and VD4 in above figure).

LEDs

AS7000-AA Dual Green LED Configuration

Two green LEDs are used (pins VD1/VD2). The other two current sinks are available on pins VD3 and VD4.

LED Characteristics

Figure 9:
LED Characteristics at T_{AMB} =25°C

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Green LED (AS7000-AA)						
I_{LED_GREEN}	Allowed operating LED current range (1)	Continuous	0		50	mA
		1/10 duty cycle @ 1 kHz			100	mA
VF_{LED_GREEN}	Forward voltage (2)	I_{LED}=20mA	2.9	3.2		V
$VF_{LED+DRIVER\_GREEN}$	Voltage on VD1/VD2 where operation of the LED and current source is guaranteed	I_{LED}= 10mA			3.6	V
		I_{LED}= 50mA			4.5	
$\lambda p_{\_GREEN}$	Dominant wavelength			527		nm
$\Delta\lambda 1/2_{\_GREEN}$	Spectral halfwidth			35		nm

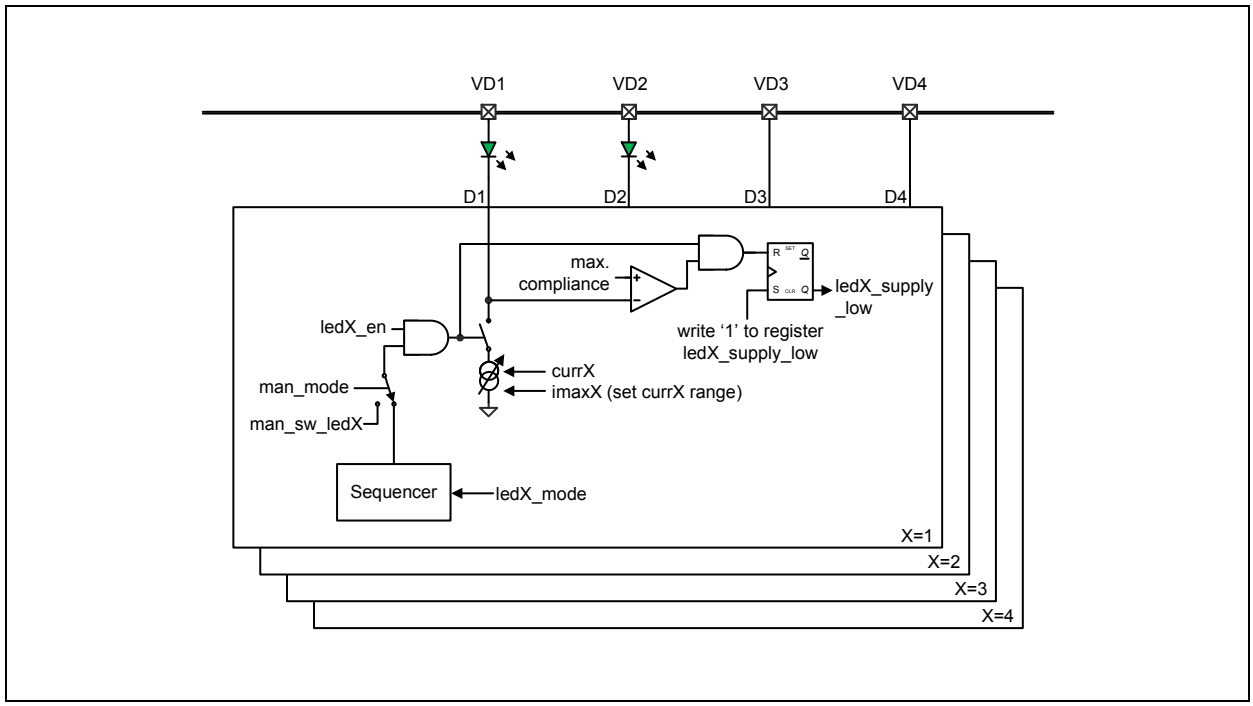
Note(s):

1. The maximum allowed LED current (DC and peak) is specified for 25°C. Lower values apply for higher temperatures.
2. Add 280mV and use LED current range ≤100mA for designing the VD1/VD2 LED supply (DC-DC converter).

LED-Driver

The four LED-driver outputs can be controlled manually or by the built in sequencer. See Optical Front End Operating Modes

Figure 10:
LED Drivers



Note(s):

1. Dual Green LED Configuration.

Figure 11:
Operating Characteristics of Each LED Current Sink, VDD=3V, T_{AMB}=25°C (unless otherwise noted)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$I_{LED1/2/3/4}$	LED output current range	imax1/2/3/4 = 00 imax1/2/3/4 = 01 imax1/2/3/4 = 10	0 0 0		25 50 100	mA mA mA
	Tolerance	25mA range imax1/2/3/4 = 00	-5		5	%
		50mA range imax1/2/3/4 = 01	-10		10	
		100mA range (1) imax1/2/3/4 = 10	-10		10	
V_Dmin	Output voltage compliance	Voltage compliance of current sinks D1,D2,D3,D4		0.28		V
V_Dmax	Output voltage maximum	Pins VD1, VD2, VD3 and VD4		5	5.5	V

Note(s):

1. Not production tested. Only guaranteed by lab characterization.

LED Configuration Registers

For ledX_supply_low registers see register AFE_PD_CFG.

Figure 12:
AFE_LED_CFG

0x00: AFE_LED_CFG					
Field	**Name**	**Rst**	**Type**	**Description**	
18	sigref_en	0	RW	Signal reference: Is required for all analog blocks 0...Disable signal reference 1...Enable signal reference	
11	led4_en	0	RW	0...Disables LED4 output source. 1...Enables LED4 output source.	
10	led3_en	0	RW	0...Disables LED3 output source. 1...Enables LED3 output source.	
9	led2_en	0	RW	0...Disables LED2 output source. 1...Enables LED2 output source.	
8	led1_en	0	RW	0...Disables LED1 output source. 1...Enables LED1 output source.	
7:6	imax4	1	RW	Defines IMAX of LED4.	
				Setting	**IMAX**
				0	25mA
				1	50mA
				2	100mA
				3	Do not use
5:4	imax3	1	RW	Defines IMAX of LED3. same encoding as imax4	
3:2	imax2	1	RW	Defines IMAX of LED2. same encoding as imax4	
1:0	imax1	1	RW	Defines IMAX of LED1. same encoding as imax4	

The LED_CFG register is used to configure the operating mode of the LED outputs.

AFE_LED_CURR Register (Addr: 0x04)

The AFE_LED_CURR defines the LED output current.

Figure 13:
AFE_LED_CURR Register

Addr: 0x04		AFE_LED_CURR		
Bit	**Bit Name**	**Default**	**Access**	**Description**
31:24	curr4	0x00	R/W	LED4 output current – do not use code=0 (will generate no output current) ILED4 = (curr4 + 1) * imax4 / 256
23:16	curr3	0x00	R/W	LED3 output current – do not use code=0 (will generate no output current) ILED3 = (curr3 + 1) * imax3 / 256
15:8	curr2	0x00	R/W	LED2 output current – do not use code=0 (will generate no output current) ILED2 = (curr2 + 1) * imax2 / 256
7:0	curr1	0x00	R/W	LED1 output current – do not use code=0 (will generate no output current) ILED1 = (curr1 + 1) * imax1 / 256

Figure 14:
AFE_MAN_SEQ_CFG

<table>
<tr><th colspan="10">0x20: AFE_MAN_SEQ_CFG</th></tr>
<tr><th>Field</th><th>Name</th><th>Rst</th><th>Type</th><th colspan="6">Description</th></tr>
<tr><td>26</td><td>man_mode</td><td>0</td><td>RW</td><td colspan="6">0...Enables Sequencer
1...Enables Manual control of optical front end</td></tr>
<tr><td>23</td><td>man_sw_itg</td><td>0</td><td>RW</td><td colspan="6">If man_mode=1
0...All integrator capacitors are shorted. Integrator is reset
1...Integrator capacitors are charging up. Integrator is running</td></tr>
<tr><td>22</td><td>man_sw_led4</td><td>0</td><td>RW</td><td colspan="6">If man_mode=1
0...LED output D4 disabled. (High impedance)
1...LED output D4 enabled</td></tr>
<tr><td>21</td><td>man_sw_led3</td><td>0</td><td>RW</td><td colspan="6">If man_mode=1
0...LED output D3 disabled. (High impedance)
1...LED output D3 enabled</td></tr>
<tr><td>20</td><td>man_sw_led2</td><td>0</td><td>RW</td><td colspan="6">If man_mode=1
0...LED output D2 disabled. (High impedance)
1...LED output D2 enabled</td></tr>
<tr><td>19</td><td>man_sw_led1</td><td>0</td><td>RW</td><td colspan="6">If man_mode=1
0...LED output D1 disabled. (High impedance)
1...LED output D1 enabled</td></tr>
<tr><td rowspan="7">18:17</td><td rowspan="7">diode_ctrl</td><td rowspan="7">0</td><td rowspan="7">RW</td><td colspan="6">Connection of Photodiodes PD1, PD2, PD3, PD4 to the photodiode amplifier.
0...PD1-PD4 are connected
1...PD1 synchronous to LED1, PD2 sync/to LED2, PD3 sync/to LED3, PD4 sync/to LED4
2...PD1 synchronous to LED1, PD2 sync/to LED1, PD3 sync/to LED2, PD4 sync/to LED2
3...PD1 synchronous to LED1, PD2 sync/to LED1, PD3 sync/to LED4, PD4 sync/to LED4
Note that AFE_PD_CFG.pdX takes precedence - to turn OFF one photo diode, the respective bit (pd1…pd4) has to be de-asserted in the AFE_PD_CFG register.</td></tr>
<tr><td>AFE_PD_CFG.pdX</td><td>diode_ctrl</td><td>Photo Diode1</td><td>Photo Diode2</td><td>Photo Diode3</td><td>Photo Diode4</td></tr>
<tr><td>0</td><td>xx</td><td>OFF</td><td>OFF</td><td>OFF</td><td>OFF</td></tr>
<tr><td>1</td><td>00</td><td>ON</td><td>ON</td><td>ON</td><td>ON</td></tr>
<tr><td>1</td><td>01</td><td>LED1</td><td>LED2</td><td>LED3</td><td>LED4</td></tr>
<tr><td>1</td><td>10</td><td>LED1</td><td>LED1</td><td>LED2</td><td>LED2</td></tr>
<tr><td>1</td><td>11</td><td>LED1</td><td>LED1</td><td>LED4</td><td>LED4</td></tr>
</table>

0x20: AFE_MAN_SEQ_CFG					
Field	**Name**	**Rst**	**Type**	**Description**	
13	dma_disable	0	RW	ADC DMA disable 1...ADC result has to be read from adc_data 0...ADC result(s) is/are written to memory	
12:10	led4_mode	0	RW	LED4 mode	
				Setting	**Behavior**
				0	Always OFF
				1	Always ON when sequencer is active
				2	Controlled by sequencer
				3	Controlled by sequencer, only ON in even iterations: 0, 2, 4 etc.
				4	Controlled by sequencer, only ON in odd iterations: 1, 3, 5 etc.
				5	Controlled by sequencer, only ON in every fourth iteration, starting at 3: 3, 7, 11 etc.
9:7	led3_mode	0	RW	LED3 mode	
				Setting	**Behavior**
				0	Always OFF
				1	Always ON when sequencer is active
				2	Controlled by sequencer
				3	Controlled by sequencer, only ON in even iterations: 0, 2, 4 etc.
				4	Controlled by sequencer, only ON in odd iterations: 1, 3, 5 etc.
				5	Controlled by sequencer, only on in every fourth iteration, starting at 2: 2, 6, 10 etc.

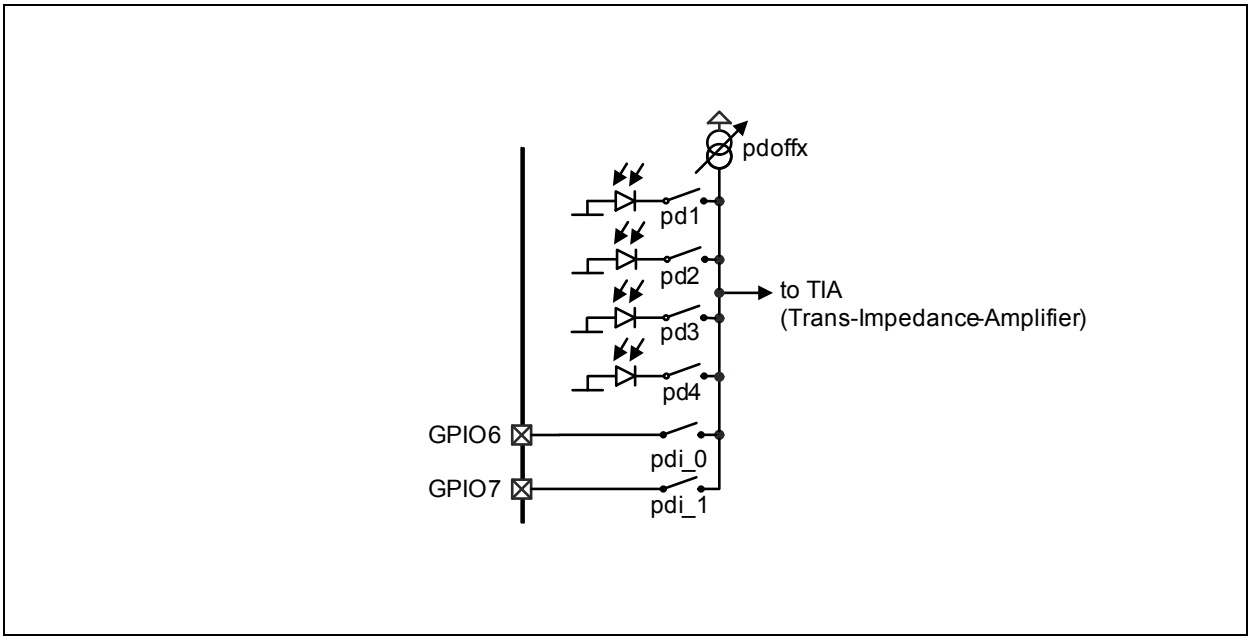
<table>
<tr><th colspan="5">0x20: AFE_MAN_SEQ_CFG</th></tr>
<tr><th>Field</th><th>Name</th><th>Rst</th><th>Type</th><th>Description</th></tr>
<tr><td rowspan="8">6:4</td><td rowspan="8">led2_mode</td><td rowspan="8">0</td><td rowspan="8">RW</td><td colspan="2">LED2 mode</td></tr>
<tr><td>Setting</td><td>Behavior</td></tr>
<tr><td>0</td><td>Always OFF</td></tr>
<tr><td>1</td><td>Always ON when sequencer is active</td></tr>
<tr><td>2</td><td>Controlled by sequencer</td></tr>
<tr><td>3</td><td>Controlled by sequencer, only ON in even iterations: 0, 2, 4 etc.</td></tr>
<tr><td>4</td><td>Controlled by sequencer, only ON in odd iterations: 1, 3, 5 etc.</td></tr>
<tr><td>5</td><td>Controlled by sequencer, only ON in every fourth iteration, starting at 1: 1, 5, 9 etc.</td></tr>
<tr><td rowspan="8">3:1</td><td rowspan="8">led1_mode</td><td rowspan="8">0</td><td rowspan="8">RW</td><td colspan="2">LED1 mode</td></tr>
<tr><td>Setting</td><td>Behavior</td></tr>
<tr><td>0</td><td>Always OFF</td></tr>
<tr><td>1</td><td>Always ON when sequencer is active</td></tr>
<tr><td>2</td><td>Controlled by sequencer</td></tr>
<tr><td>3</td><td>Controlled by sequencer, only ON in even iterations: 0, 2, 4 etc.</td></tr>
<tr><td>4</td><td>Controlled by sequencer, only ON in odd iterations: 1, 3, 5 etc.</td></tr>
<tr><td>5</td><td>Controlled by sequencer, only ON in every fourth iteration, starting at 0: 0, 4, 8 etc.</td></tr>
<tr><td>0</td><td>seq_en</td><td>0</td><td>RW</td><td colspan="2">0...Disables sequencer
1...Enables sequencer</td></tr>
</table>

Photodiode Selection

In order to have flexible arrangement of the use photodiodes, PD1-PD4 can be individually connected to the photodiode amplifier input. The optional offset current allows cancellation of constant light sources like sunlight. In case of an external photodiode or any other sensor with (low) current output, the pins GPIO6 and GPIO7 can be used as input.

Additionally the sequencer can control the diodes – see diode_ctrl described in register AFE_MAN_SEQ_CFG .

Figure 15:
Photodiode Selection



AFE_PD_CFG Register (Addr: 0x08)

The AFE_PD_CFG register is used to configure the input to the photo amplifier.

Figure 16:
AFE_PD_CFG Register

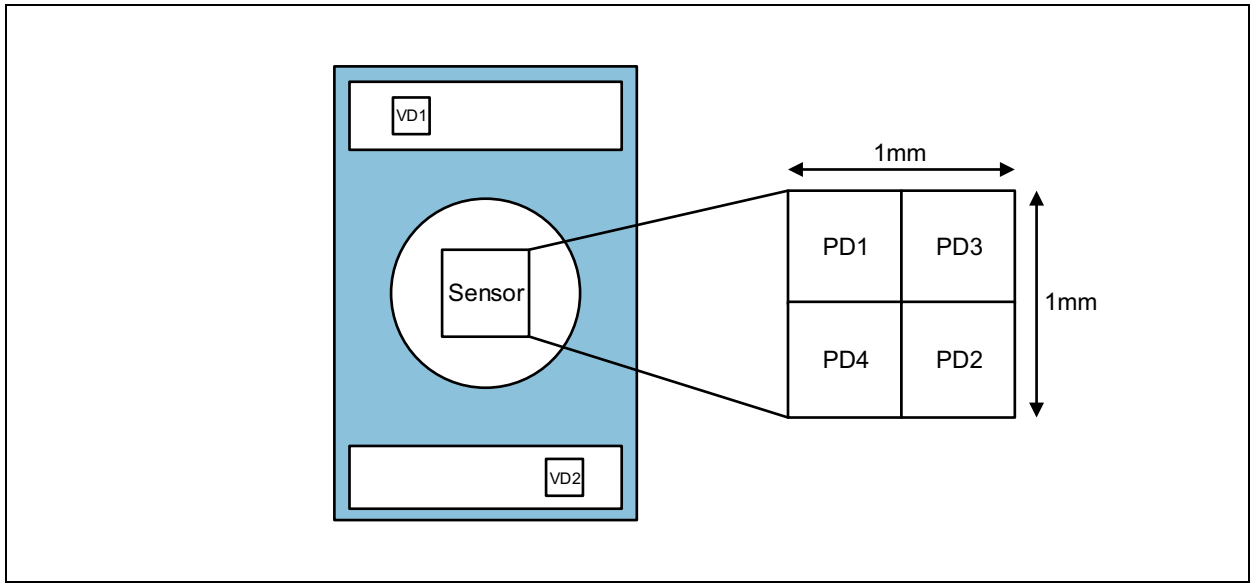
Addr: 0x08		AFE_PD_CFG		
Bit	**Bit Name**	**Default**	**Access**	**Description**
25	sd_hld	0	R/W	SD hold 0 …Output of synchronous demodulator is forced to SIGREF if not set to +1 or -1 1… Output of synchronous demodulator is tristated if not set to +1 or -1
23	led4_ supply_low	0	SC_WS (1)	If this bit is cleared, LED4 current sink voltage was below its compliance voltage
22	led3_ supply_low	0	SC_WS (1)	If this bit is cleared, LED3 current sink voltage was below its compliance voltage.
21	led2_ supply_low	0	SC_WS (1)	If this bit is cleared, LED2 current sink voltage was below its compliance voltage.
20	led1_ supply_low	0	SC_WS (1)	If this bit is cleared, LED1 current sink voltage was below its compliance voltage.
15:8	pdoffx	0x00	R/W	Input offset current Ioffset = pdoffx*10nA 00000000…Offset source is turned OFF
5	pd4	0	R/W	0 …Photodiode PD4 is disconnected from photo amplifier 1 …Photodiode PD4 is connected to photo amplifier (as defined in diode_ctrl)
4	pd3	0	R/W	0 …Photodiode PD3 is disconnected from photo amplifier 1 …Photodiode PD3 is connected to photo amplifier (as defined in diode_ctrl)
3	pd2	0	R/W	0 …Photodiode PD2 is disconnected from photo amplifier 1 …Photodiode PD2 is connected to photo amplifier (as defined in diode_ctrl)
2	pd1	0	R/W	0 …Photodiode PD1 is disconnected from photo amplifier 1 …Photodiode PD1 is connected to photo amplifier (as defined in diode_ctrl)
1	pdi_1	0	R/W	0 …GPIO7-input is disconnected from photo amplifier 1 …GPIO7-input is connected to photo amplifier
0	pdi_0	0	R/W	0 …GPIO6-input is disconnected from photo amplifier 1 …GPIO6-input is connected to photo amplifier

Note(s):

1. SC_WS: Self clear, write sets: These registers are reset by the hardware. Set to '1' before using them.

Photodiode Characteristics

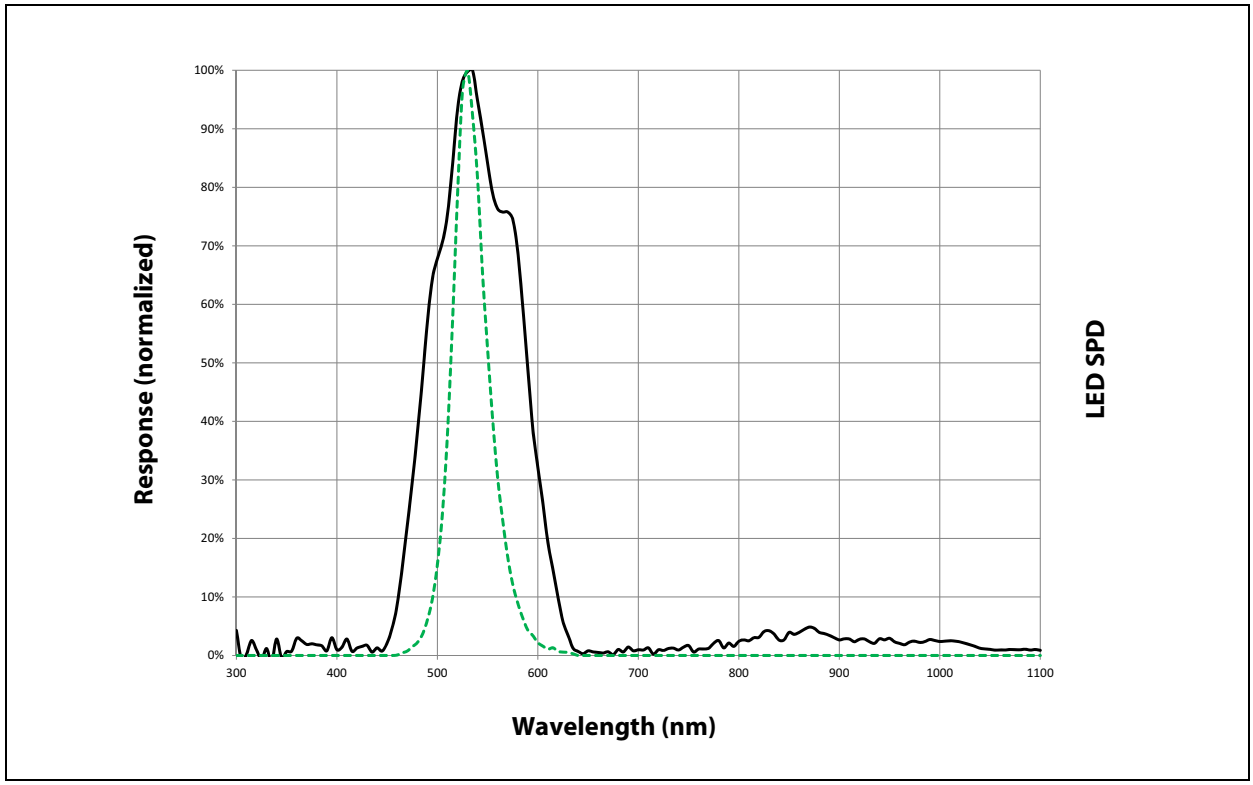
Figure 17:
Photodiode Arrangement



Note(s):

1. Orientation as in Figure 115 or Figure 3.

Figure 18:
AS7000-AA Photodiode Sensitivity (Solid Black) and LED Emission Spectrum (Dotted Green) – Dual Green LED Configuration



Note(s):

1. Perpendicular light source.
2. LEDs and Filters are shown for Dual Green LED Configuration.

Figure 19:
Operating Characteristics of Each Photodiode, VDD=3V, T_{AMB}=25°C (unless otherwise noted)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Re	Irradiance responsivity	λ_p=525nm, 4 photodiodes used pd1/2/3/4=1, gain_g=4x, gain_en=1, pd_ampres=7MΩ dual green LED configuration filters		76		mV/ (µW /cm^2)
Id	Dark current	E_e=0	0		1	nA
Ios	Extrapolated offset current		–1		1	nA

Note(s):

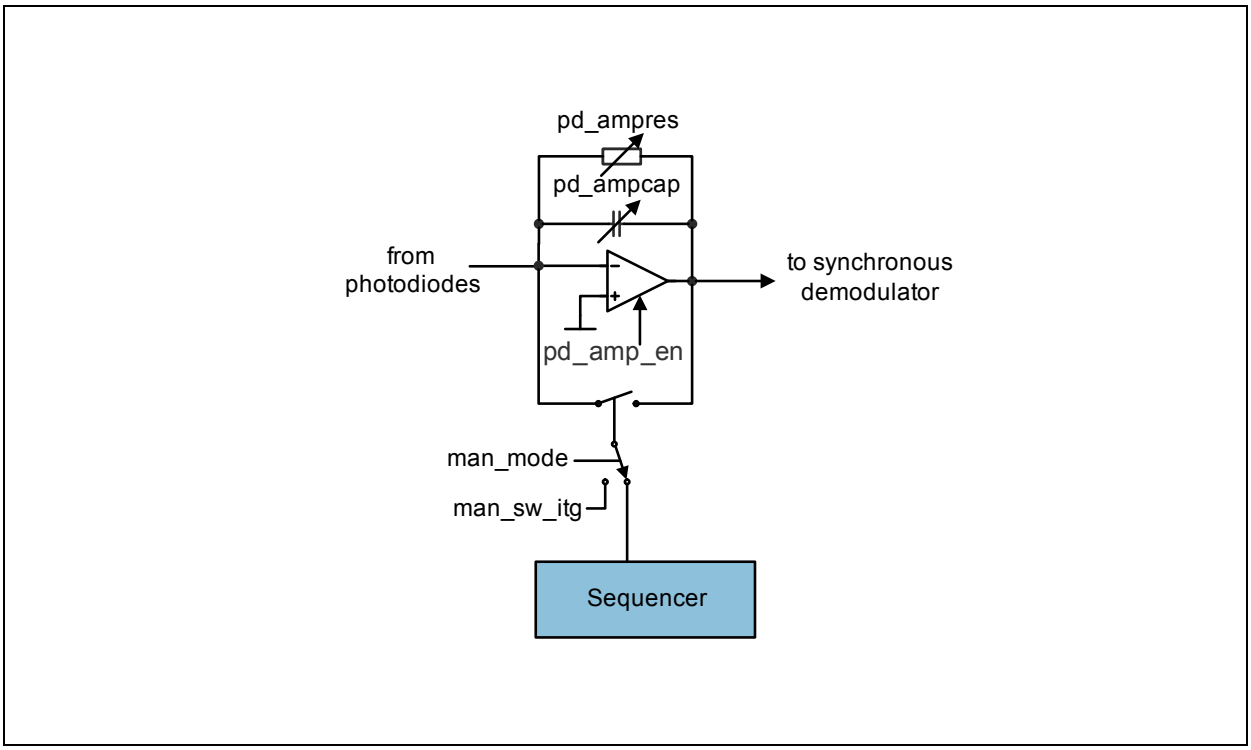
1. For monochromatic light of 555nm, one lux corresponds to 0.146 µW/cm2. That is, one obtains 6.5 lux per µW/cm2

Photodiode Trans-Impedance Amplifier (TIA)

The photodiode amplifier can be configured in three different modes:

- Photocurrent to frequency converter
- Photocurrent to voltage converter
- Photocurrent integrator

Figure 20:
Trans-Impedance-Amplifier (TIA)



The integration time t_{INT} is defined either by the sequencer (man_mode=0) of manually through the bit sw_itg if man_mode=1.

Figure 21:
Settings for the Programming of the TIA

pd_ampres	pd12341	pd_ampcap	pd_ampcomp	pd_ampvo	Gain
1	1…4	13	1	15	1V/µA
2	1…4	7	1	15	2V/µA
3	1…4	5	1	15	3V/µA
4	1…2	2	0	15	5V/µA
	3…4	3			
5	1…2	2	0	15	7V/µA
	3…4	3			
6	1	1	0	15	10V/µA
	2…4	2			
7	1…2	1	0	15	15V/µA
	3…4	2			
Low Bandwidth Mode					
5	1…4	31	3	15	7V/µA
Integrating Mode (pd_ampres=0)					
0	1…4	10	3	15	1V/pQ
0	1…4	20	3	15	1/2V/pQ
0	1…4	30	3	15	1/3V/pQ

Note(s):

1. pd1234 … number of active photodiodes (for example, pd1=1, pd2=0, pd3=1, pd4=0 -> pd1234=2)

AFE_PD_AMPCFG Register (Addr: 0x0c)

The AFE_PD_AMPCFG register is used to configure the operating mode of the photo-amplifier

Figure 22:
AFE_PD_AMPCFG Register

Addr: 0x0c		AFE_PD_AMPCFG		
Bit	**Bit Name**	**Default**	**Access**	**Description**
31	pd_amp_en	0	R/W	0…Activates power down mode of photo-amplifier 1…Enables photo-amplifier
13:10	pd_amp_vo	15	R/W	Opamp offset. Use **ams** device drivers – these automatically configure this register.
9:8	pd_ ampcomp	3	R/W	Opamp compensation. Use **ams** device drivers – these automatically configure this register.
7:5	pd_ampres	0x0	R/W	Feedback resistor 000…No resistor in feedback of amplifier 001…1MΩ 010…2MΩ 011…3MΩ 100…5MΩ 101…7MΩ 110…10MΩ 111…15MΩ
4:0	pd_ampcap	0x0	R/W	Feedback capacitor – automatically set by **ams** device drivers for modes using pd_ampres not 000b. Capacitor = pd_ampcap*0.1pF

For registers man_mode and man_sw_itg see AFE_MAN_SEQ_CFG .

Voltage Mode of the Photodiode Amplifier

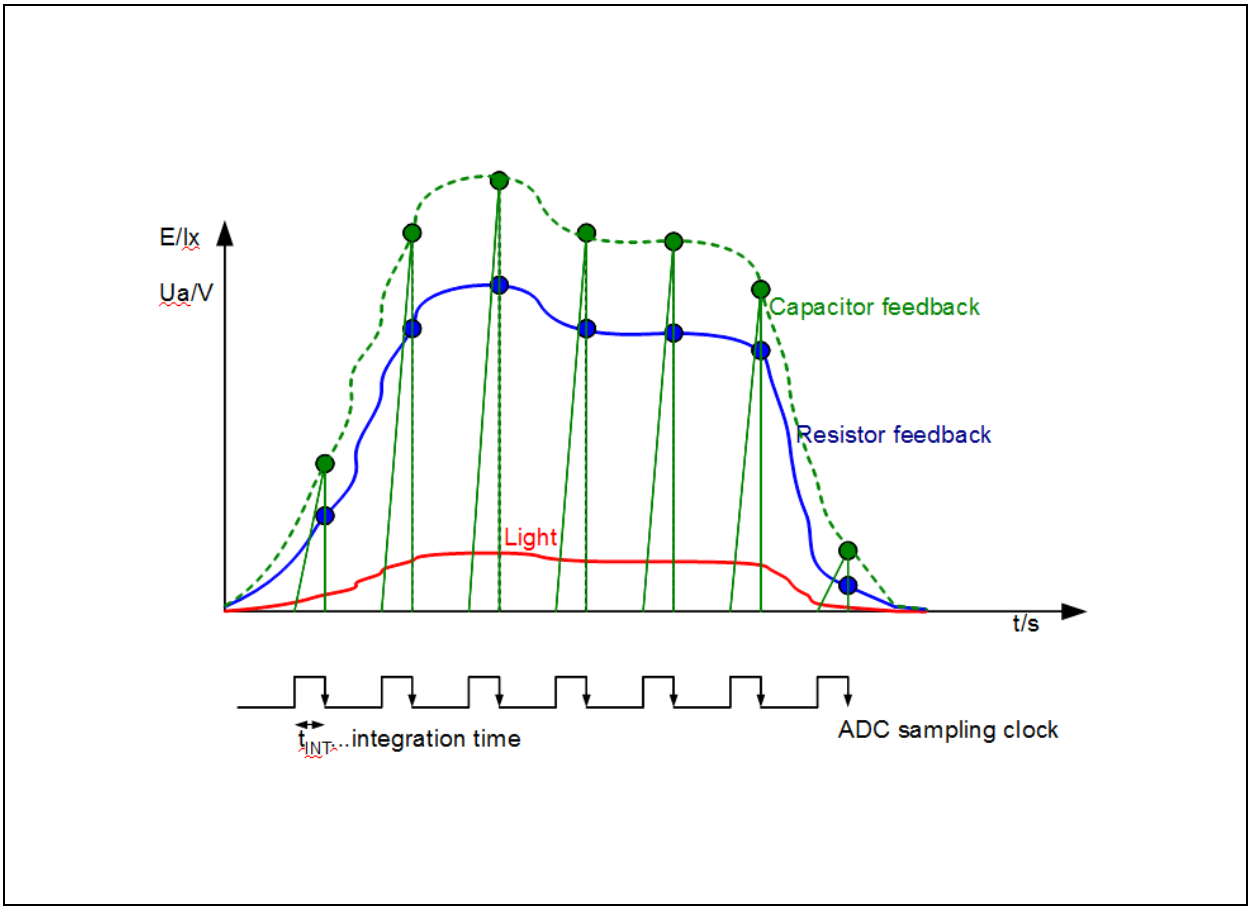
The output voltage of the photodiode amplifier is depending on the feedback component:

(EQ1) Feedback resistor: $U_{out} = I_{photo} \cdot R_{fb}$

(EQ2) Feedback capacitor: $U_{out} = I_{photo} \cdot \frac{t_{INT}}{C_{fb}}$

Note(s): The integration time t_{INT} is defined either by the sequencer (man_mode=0) of manually through the bit sw_itg if man_mode=1.
For the synchronous demodulator only use the resistive feedback.

Figure 23:
Difference Between Resistive and Capacitive Feedback



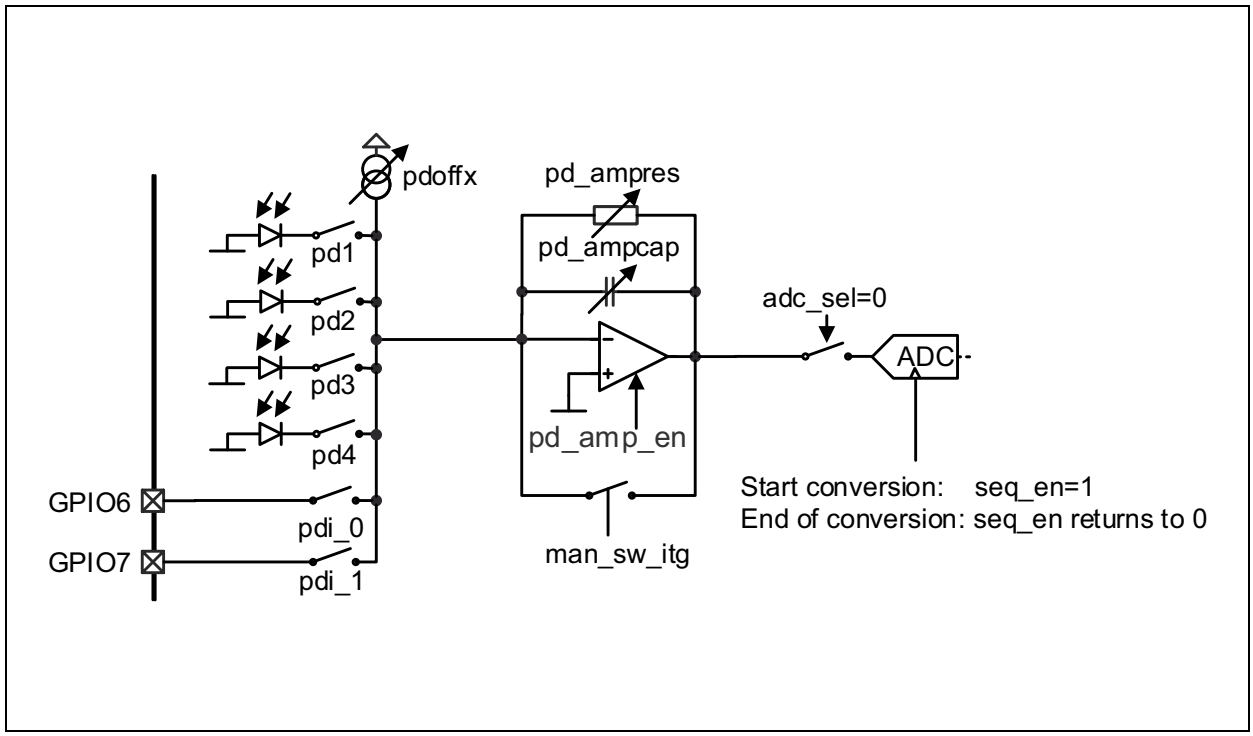
Optical Front End Operating Modes

Once the photodiode amplifier is configured the measurement can be done in two different ways. Either the LED-outputs, the photodiode amplifier and the ADC are controlled manually by means of register bits, or they are controlled by a built in sequencer.

Manual Operation of The Optical Frontend:

The optical front end can be manually controlled via the AFE_MAN_SEQ_CFG register using man_mode=1.

Figure 24:
Manual Operation of the Optical Frontend and LED



Note(s):

1. Applies only if man_mode=1.

For manual operation of the LEDs and its current sinks see LED-Driver.

Sequencer

In order to synchronize the LED-currents, the integration time and the ADC-sampling time, a built in sampling Sequencers can be used. The sequencer generates the 16 bit-timings based on a 1µs clock. The results of the analog to digital conversion are automatically stored in a pipeline buffer or in register adc_data.

The timings can be programmed with following registers (apply for man_mode=0):

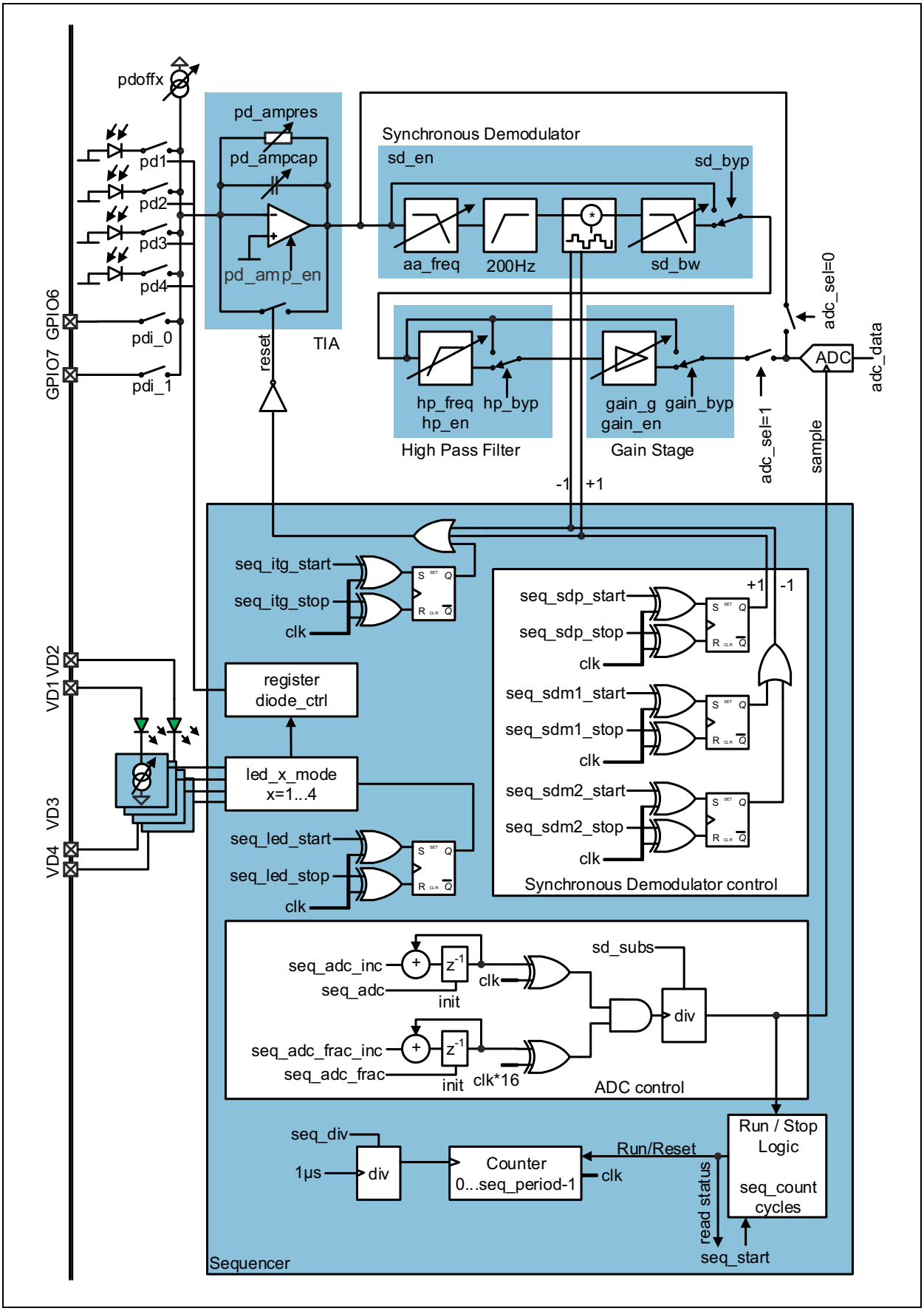
Figure 25:
Sequencer Control Registers Overview

Register	Description
seq_div	Divider of the 1µs input clock
seq_count	Number of measurements in one sequence
seq_start	Writing 1 starts the sequencer, 0 stops the sequencer
seq_period	Time of one measurement cycle
seq_led_start	Start time of the LED drivers within one cycle
seq_led_stop	Stop time of the LED drivers within one cycle
seq_itg_start	Start time of the integrator
seq_itg_stop	Stop time of the integrator
seq_sdp_start	Start time of the synchronous demodulator's positive multiplication
seq_sdp_stop	Stop time of the synchronous demodulator's positive multiplication
seq_sdm1_start	Start time of the synchronous demodulator's negative multiplication 1
seq_sdm1_stop	Stop time of the synchronous demodulator's negative multiplication 1
seq_sdm2_start	Start time of the synchronous demodulator's negative multiplication 2
seq_sdm2_stop	Stop time of the synchronous demodulator's negative multiplication 2
seq_adc, seq_adc_fract	Sampling position of the ADC in single steps / in 1/16th steps
seq_adc_inc, seq_adc_inc_fract	Increment of the sampling position of the ADC after each measurement in single steps / in 1/16th steps
sd_subs	Subsampling ratio between sequencer frequency and ADC sampling frequency – use for adjusting the ADC sampling frequency at a lower speed than the sequencer cycle frequency

Note(s):

1. The lowest data value of all registers except seq_count, seq_div, seq_adc_inc, seq_adc_inc_fract and seq_adc_fract is 1.

Figure 26:
Block Diagram of Sequencer



Sequencer Registers

For registers man_mode, man_sw_sdmult, man_sw_sdpol, man_sw_itg, man_sw_led4, man_sw_led3, man_sw_led2, man_sw_led1, diode_ctrl, dma_disable, led4_mode, led3_mode, led2_mode and led1_mode,seq_en
see AFE_MAN_SEQ_CFG .

For register sd_subs see AFE_SC_CFG .

AFE_SEQ_DIV_CNT Register (Addr: 0x24)

The AFE_SEQ_DIV_CNT register sets the input divider for the main clock.

Figure 27:
AFE_SEQ_DIV_CNT Register

Addr: 0x24		AFE_SEQ_DIV_CNT		
Bit	**Bit Name**	**Default**	**Access**	**Description**
23:8	seq_div	0x0000	R/W	Divider value; Sequencer time increment $t_{clk} = (seq\_div + 1) * 1\mu s$
7:0	seq_count	0x00	R/W	Number of measurements in one sequence. IF seq_count = 0x00 the sequencer is running continuously.

AFE_SEQ_START Register (Addr: 0x28)

In AFE_SEQ_START register the configured sequencer can be started.

Figure 28:
AFE_SEQ_START Register

Addr: 0x28		AFE_SEQ_START		
Bit	**Bit Name**	**Default**	**Access**	**Description**
0	seq_start	0	R/W	1…Starts the sequencer. Sequencer is running according to the configurations in the sequencer registers Writing 0 stops the sequencer(s). In manual mode, writing 1 starts one ADC conversion. Reading returns 1 if the sequencer is running (sequencer mode), respectively if the ADC is converting (manual mode) and it returns to 0 once the ADC has finished its conversion

AFE_SEQ_PER Register (Addr: 0x2C)

The AFE_SEQ_PER register sets one measurement cycle of the sequencer.

Figure 29:
AFE_SEQ_PER Register

Addr: 0x2C		AFE_SEQ_PER		
Bit	**Bit Name**	**Default**	**Access**	**Description**
15:0	seq_period	0x0000	R/W	Sequencer period *T = seq_period * seq_div * 1µs*

AFE_SEQ_LED Register (Addr: 0x30)

The AFE_SEQ_LED register sets the LED drive timing. Data is stored as 16-bit value

Figure 30:
AFE_SEQ_LED Register

Addr: 0x30		AFE_SEQ_LED		
Bit	**Bit Name**	**Default**	**Access**	**Description**
31:16	seq_led_start	0x0000	R/W	LED start time; the LED starts one cycle later to allow the analog biasing to settle before the current is enabled.
15:0	seq_led_stop	0x0000	R/W	LED stop time

AFE_SEQ_ITG Register (Addr: 0x34)

The AFE_SEQ_ITG register sets the photoamplifier integration time if using capacitive feedback respectively removes the short of the resistive feedback. Data is stored as 16-bit value

Figure 31:
AFE_SEQ_ITG Register

Addr: 0x34		AFE_SEQ_ITG		
Bit	**Bit Name**	**Default**	**Access**	**Description**
31:16	seq_itg_start	0x0001	R/W	Integrator start time (start time=1 and stop time=0 means that it's - by default - always ON) Turning OFF the integrator actually means discharge the capacitor for capacitive integration mode, without the synchronous demodulator.
15:0	seq_itg_stop	0x0000	R/W	Integrator stop time

AFE_SEQ_SDP Register (Addr: 0x38)

The AFE_SEQ_SDP register sets the synchronous demodulator positive multiplication time. Data is stored as 16-bit value

Figure 32:
AFE_SEQ_SDP Register

Addr: 0x38		AFE_SEQ_SDP		
Bit	Bit Name	Default	Access	Description
31:16	seq_sdp_start	0x0000	R/W	Positive multiplication start time
15:0	seq_sdp_stop	0x0000	R/W	Positive multiplication stop time

AFE_SEQ_SDM1 Register (Addr: 0x3C)

The AFE_SEQ_SDM1 register sets the synchronous demodulator negative multiplication time 1. Data is stored as 16-bit value

Figure 33:
AFE_SEQ_SDM1 Register

Addr: 0x3C		AFE_SEQ_SDM1		
Bit	Bit Name	Default	Access	Description
31:16	seq_sdm1_start	0x0000	R/W	Negative multiplication start time 1
15:0	seq_sdm1_stop	0x0000	R/W	Negative multiplication stop time 1

AFE_SEQ_SDM2 Register (Addr: 0x40)

The AFE_SEQ_SDM2 register sets the synchronous demodulator negative multiplication time 2. Data is stored as 16-bit value

Figure 34:
AFE_SEQ_SDM2 Register

Addr: 0x40		AFE_SEQ_SDM2		
Bit	Bit Name	Default	Access	Description
31:16	seq_sdm2_start	0x0000	R/W	Negative multiplication start time 2
15:0	seq_sdm2_stop	0x0000	R/W	Negative multiplication stop time 2

AFE_SEQ_ADC Register (Addr: 0x44)

The AFE_SEQ_ADC register defines the time when the ADC starts sampling during each measurement cycle. The fraction setting permits a definition of the sampling point as a 1/16 fraction of a sequencer cycle. If seq_div=0 (1us sequencer clock), then one unit is equivalent to 62.5ns. If, e.g. seq_div=4 (5us) then the resolution of the fract register is 62.5ns*5=312.5ns

Figure 35:
AFE_SEQ_ADC Register

Addr: 0x44		AFE_SEQ_ADC		
Bit	**Bit Name**	**Default**	**Access**	**Description**
31:28	seq_adc_inc_fract	0x0	R/W	ADC delay increment : seq_adc_inc_fract/16 fractional
27:24	seq_adc_fract	0x0	R/W	ADC start delay: seq_adc_fract/16 fractional
23:16	seq_adc_inc	0x00	R/W	ADC increment to the adc sample time after each conversion.
15:0	seq_adc	0x0000	R/W	ADC Sampling time; changes of this register have no effect as long as the sequencer is running (seq_en=1).

AFE_SEQ_COUNTER Register (Addr: 0x80)

The AFE_SEQ_COUNTER register shows the counter value of the sequence counter and period counter

Figure 36:
AFE_SEQ_COUNTER Register

Addr: 0x80		AFE_SEQ_COUNTER		
Bit	**Bit Name**	**Default**	**Access**	**Description**
31:24	subs_counter	0x00	R	Current subsampling counter value
23:16	sequence_counter	0x00	R	Current sequence counter value
15:0	cycle_counter	0x0000	R	Current cycle counter value

AFE_ADC_COUNTER Register (Addr: 0x84)

The AFE_ADC_COUNTER register shows the current value of the ADC counter

Figure 37:
AFE_ADC_COUNTER Register

Addr: 0x84		AFE_ADC_COUNTER		
Bit	**Bit Name**	**Default**	**Access**	**Description**
7:0	adc_counter	0x00	R	Current ADC counter value

Example Sequencer Configurations

Used adc_clock = 0 and adc_highres=0 for the examples to shorten the ADC settling time. As seq_div = 1 and seq_period=40, one sequence is 80µs.

Example 1

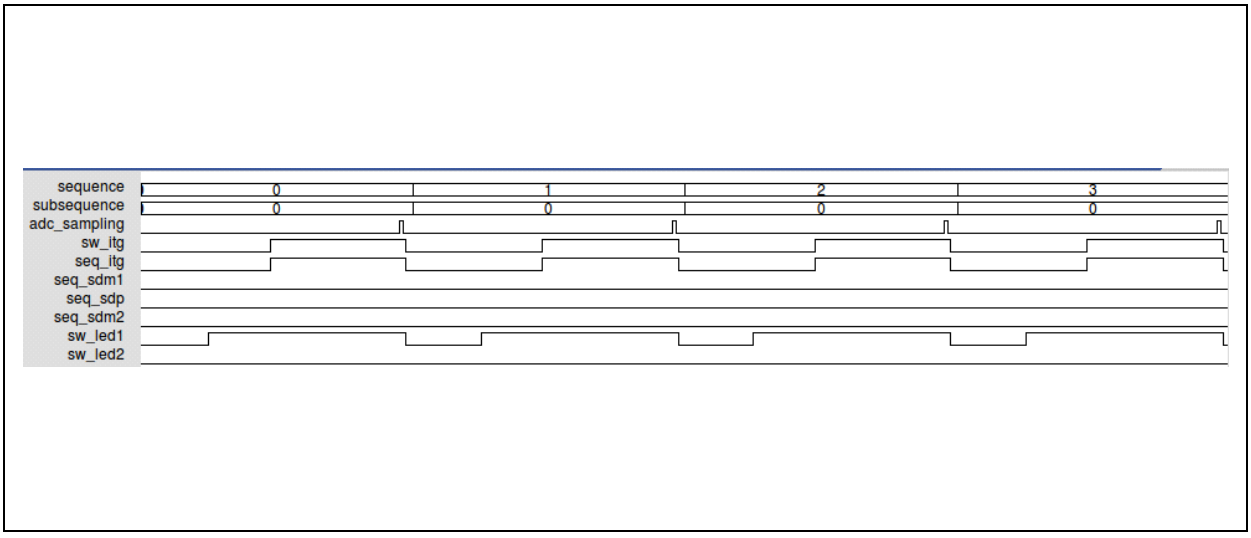
Making 4 measurements with LED1 only.

Integration time is 20 cycles. LED is turned on 10 cycles before integration starts to avoid current bouncing errors.

Figure 38:
Sequencer Example 1

seq_ period	seq_ div	seq_ count	seq_ led_ start	seq_ led_ stop	seq_ itg_ start	seq_ itg_ stop	seq_ adc	seq_ adc_inc	led1_ mode	led2_ mode
40	1	4	10	40	20	40	39	0	2	0

Figure 39:
Sequencer Example 1 Waveform



Example 2

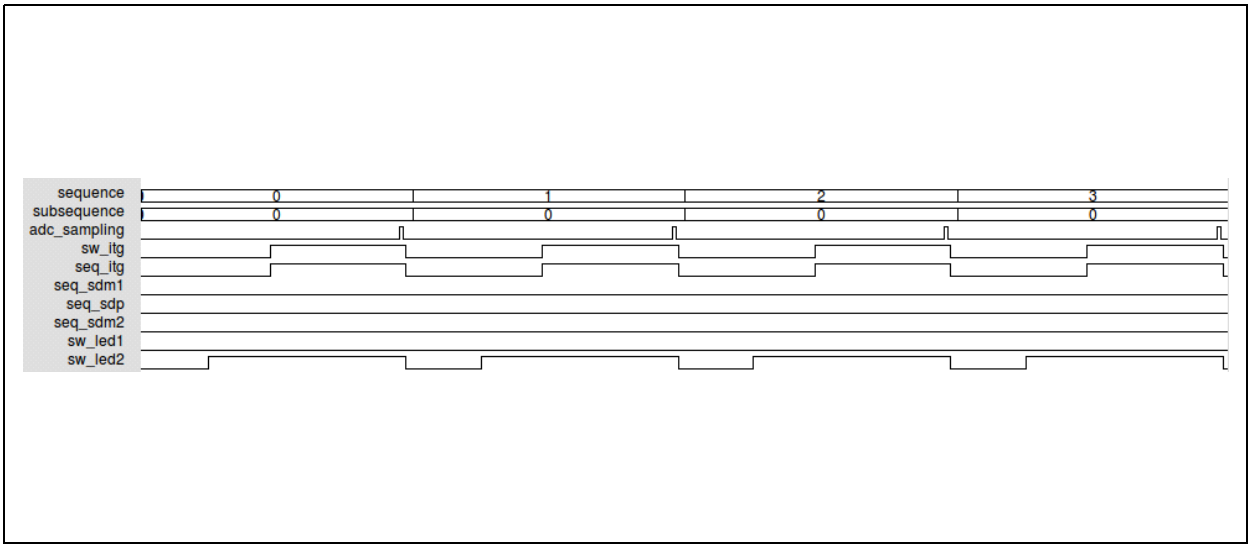
Making 4 measurements with LED2 only.

Integration time is 20 cycles. LED is turned ON 10 cycles before integration starts to avoid current bouncing errors.

Figure 40:
Sequencer Example 2

seq_ period	seq_ div	seq_ count	seq_ led_ start	seq_ led_ stop	seq_ itg_ start	seq_ itg_ stop	seq_ adc	seq_ adc_inc	led1_ mode	led2_ mode
40	1	4	10	40	20	40	39	0	0	2

Figure 41:
Sequencer Example 2 Waveform



Example 3

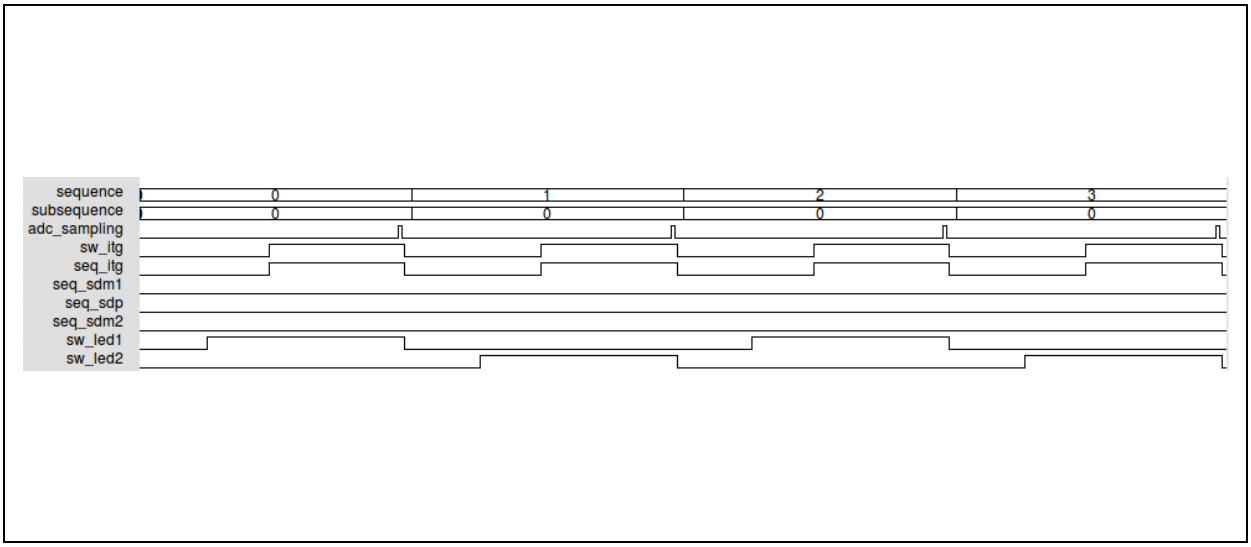
Making 4 measurements, switching between LED1 and LED2.

Integration time is 20 cycles. LED is turned ON 10 cycles before integration starts to avoid current bouncing errors.

Figure 42:
Sequencer Example 3

seq_ period	seq_ div	seq_ count	seq_ led_ start	seq_ led_ stop	seq_ itg_ start	seq_ itg_ stop	seq_ adc	seq_ adc_inc	led1_ mode	led2_ mode
40	1	4	10	40	20	40	39	0	3	4

Figure 43:
Sequencer Example 3 Waveform



Example 4

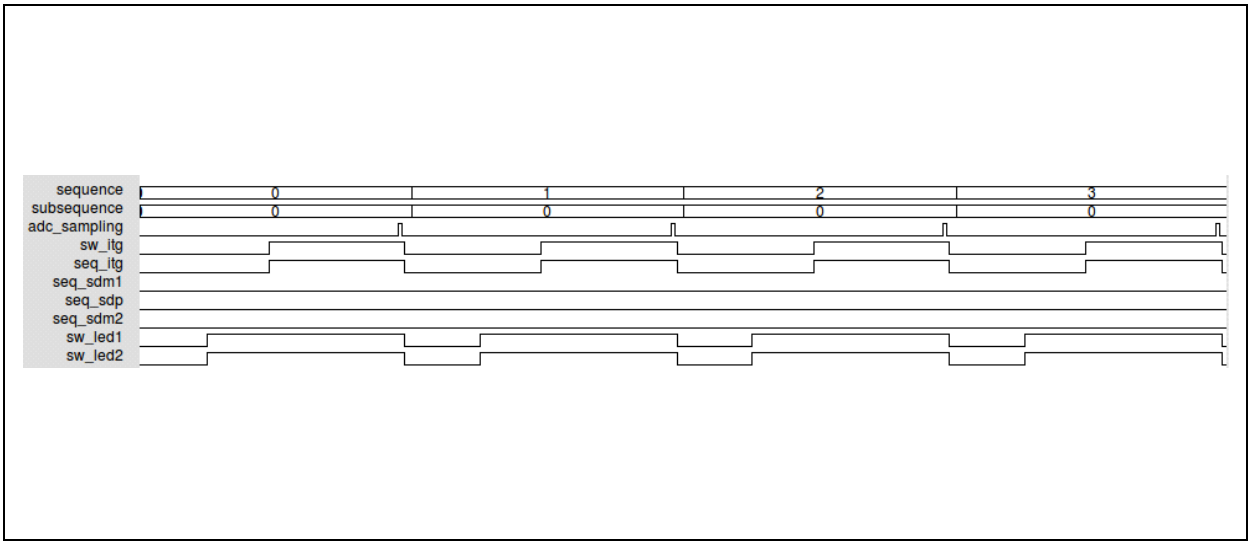
Making 4 measurements, switching LED1 and LED2 simultaneously.

Integration time is 20 cycles. LED is turned ON 10 cycles before integration starts to avoid current bouncing errors.

Figure 44:
Sequencer Example 4

seq_ period	seq_ div	seq_ count	seq_ led_ start	seq_ led_ stop	seq_ itg_ start	seq_ itg_ stop	seq_ adc	seq_ adc_inc	led1_ mode	led2_ mode
40	1	4	10	40	20	40	39	0	2	2

Figure 45:
Sequencer Example 4 Waveform



Example 5

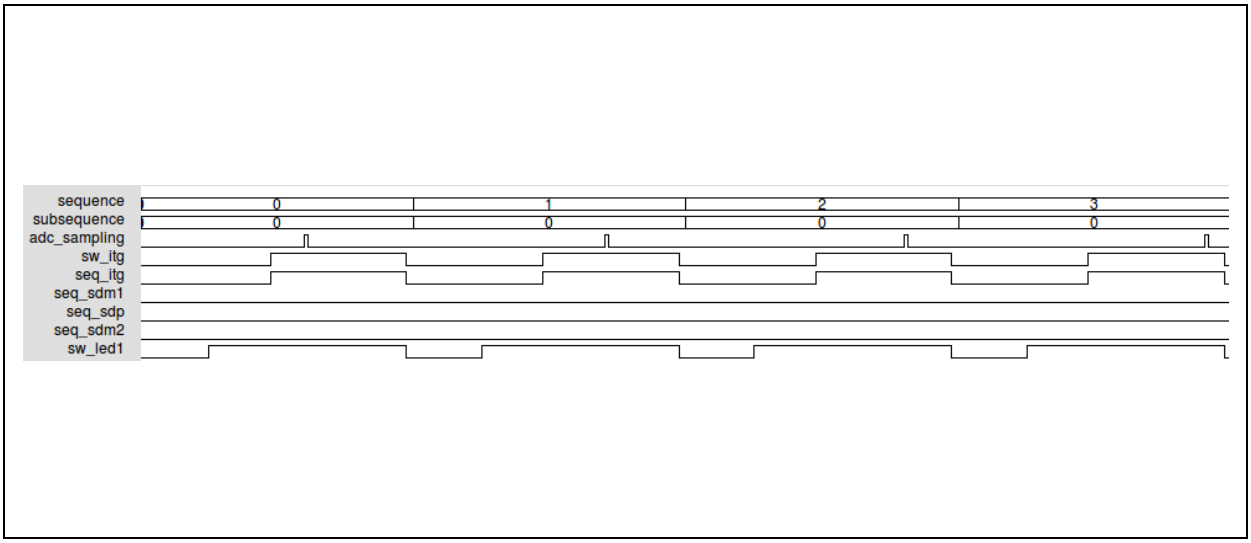
Making 4 measurements with LED1 only and subsampling.

Integration time is 20 cycles. LED is turned ON 10 cycles before integration starts to avoid current bouncing errors. ADC sampling starts 5 cycles delayed every measurement.

Figure 46:
Sequencer Example 5

seq_ period	seq_ div	seq_ count	seq_ led_ start	seq_ led_ stop	seq_ itg_ start	seq_ itg_ stop	seq_ adc	seq_ adc_inc	led1_ mode	led2_ mode
40	1	4	10	40	20	40	25	4	2	0

Figure 47:
Sequencer Example 5 Waveform



Example 6

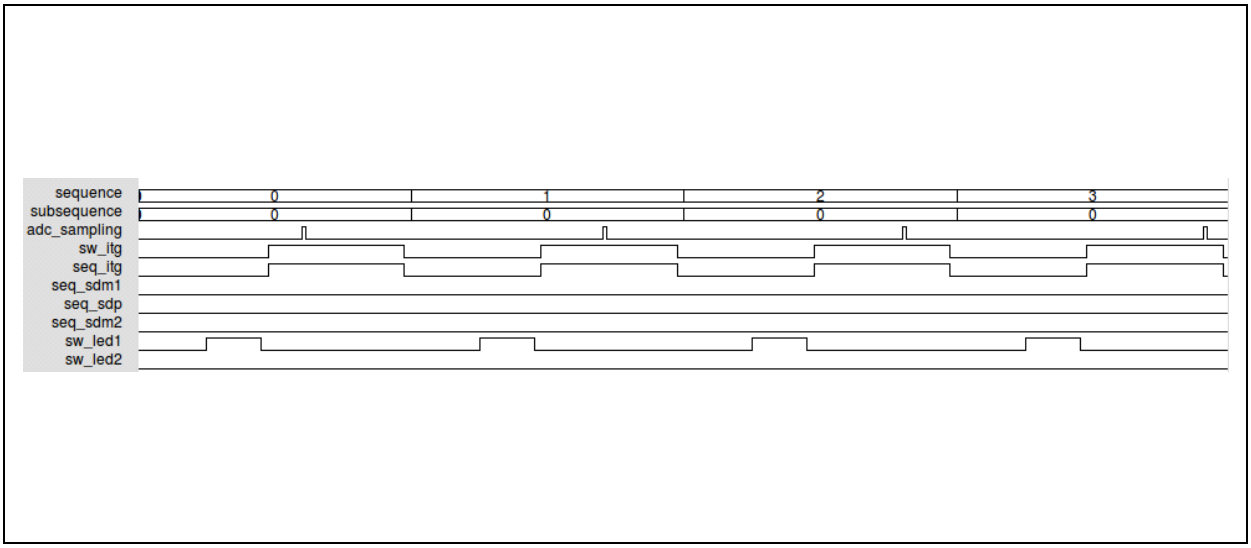
Making 4 measurements with LED1 only and subsampling.

Integration time is 20 cycles. LED is turned OFF 10 cycles before integration starts to measure fluorescent response of a sensor. ADC sampling starts 5 cycles delayed every measurement.

Figure 48:
Sequencer Example 6

seq_ period	seq_ div	seq_ count	seq_ led_ start	seq_ led_ stop	seq_ itg_ start	seq_ itg_ stop	seq_ adc	seq_ adc_inc	led1_ mode	led2_ mode
40	1	4	10	19	20	40	25	4	2	0

Figure 49:
Sequencer Example 6 Waveform



Example 7

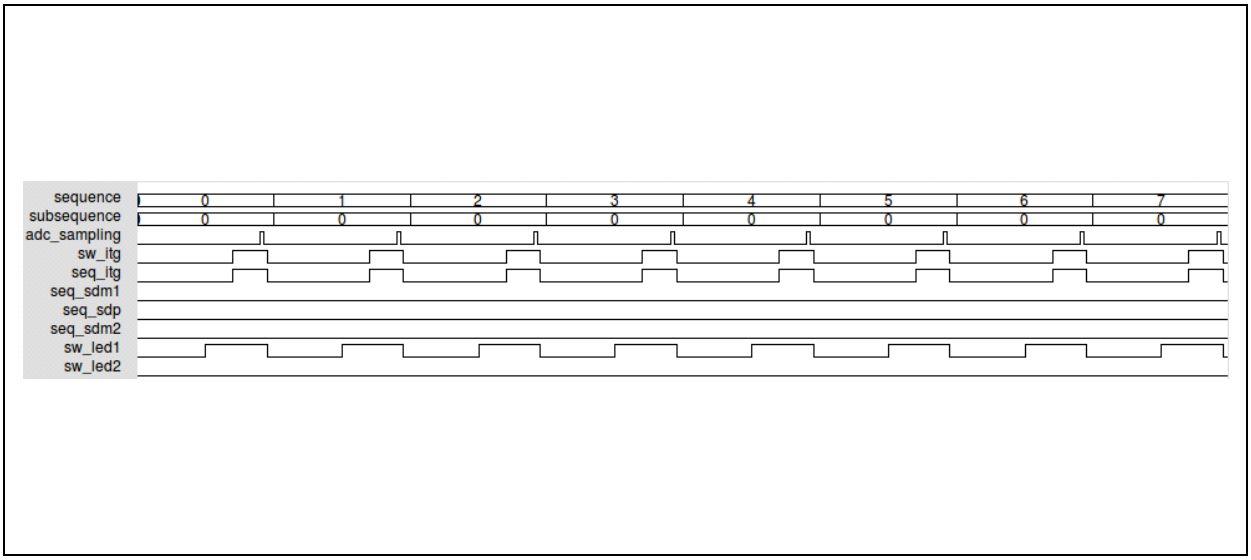
Making 8 measurements with LED1 only. Reduced cycle time to 40µs.

Integration time is 5 cycles. LED is turned ON 5 cycles before integration starts to avoid current bouncing errors.

Figure 50:
Sequencer Example 7

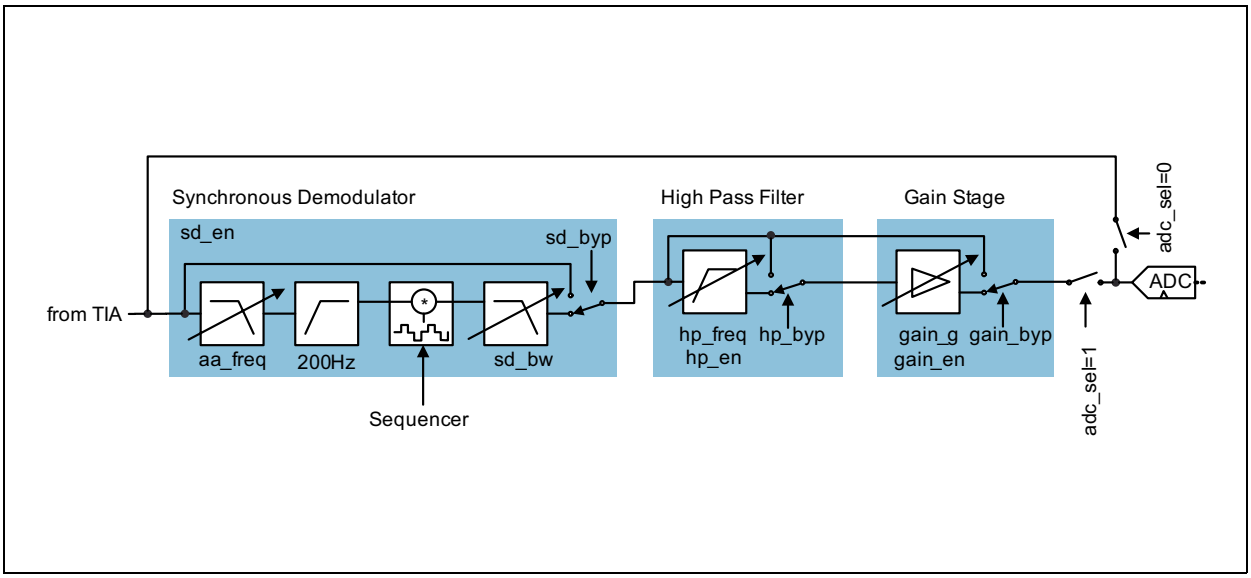
seq_ period	seq_ div	seq_ count	seq_ led_ start	seq_ led_ stop	seq_ itg_ start	seq_ itg_ stop	seq_ adc	seq_ adc_inc	led1_ mode	led2_ mode
20	1	8	10	20	15	20	19	0	2	0

Figure 51:
Sequencer Example 7 Waveform



Optical Signal Conditioning

Figure 52:
Optical Signal Conditioning



Synchronous Demodulator

An optional synchronous demodulator can be used to detect small optical signals in the presence of large unwanted noise (ambient light). Since the detector synchronizes to the LED frequency, the demodulator can only be used of the measurement sequencer is running.

It includes input filer (high pass at 200Hz, adjustable low pass) and an 2nd order adjustable output low pass. The demodulator itself multiplies the signal by +1 / 0 / -1 with a timing which is controlled by the sequencer.

Note(s): The optical signal conditioning stage need sigref_ en=1 for operation.

High Pass Filter

An optional high pass filter can be used to remove unwanted DC-components from the signal and allows further amplification. In order to guarantee fast settling times of the filter, four cutoff frequencies can be chosen.

Gain Stage

An optional gain stage can be used to amplify the signal after the DC-component has been removed.

Optical Signal Conditioning Registers

Register bit sigref_en see register AFE_LED_CFG.

Figure 53:
AFE_SC_CFG

0x70: AFE_SC_CFG					
Field	**Name**	**Rst**	**Type**	**Description**	
26	sd_pol_init	0	RW	The low level driver shall ensure that this register is 0 if one of the seq_sdm pulses is first, and is 1 if the seq_sdp is first within a sequence.	
25:24	aa_freq	0	RW	Anti-aliasing filter cut-off frequency	
				Setting	**Signal**
				0	10kHz
				1	20kHz
				2	40kHz
				3	60kHz
20:13	sd_subs	0	RW	Synchronous demodulator subsampling ratio between sequencer frequency and ADC sampling frequency. ADC-Fsample = Sequencyer_Frequency/(sd_subs+1) When setting to 0, then in every sequencer iteration the ADC will run. When setting to 1, then the first sequencer iteration will not trigger the ADC, but the second one will. Setting to N will make N iterations without ADC, followed by one iteration with the ADC measurement executed. It is recommended to use the ADC interrupt in this case and not the sequencer interrupt.	
12:11	sd_bw	0	RW	Synchronous demodulator low pass filter.	
				Setting	**Frequency**
				0	10Hz
				1	20Hz
				2	40Hz
				3	80Hz
10	hp_en	0	RW	0...Power down of the high pass filter 1...Enable high pass filter	
9	hp_byp	0	RW	0...HP filter is used 1...HP filter is bypassed	

0x70: AFE_SC_CFG					
Field	**Name**	**Rst**	**Type**	**Description**	
8:7	hp_freq	0	RW	High pass filter cutoff frequency	
				Setting	**Cutoff frequency**
				0	0.33Hz
				1	1.32Hz
				2	5.28Hz
				3	10.56Hz
6	sd_en	0	RW	0...Power down of the synchronous demodulator 1...Enable synchronous demodulator	
5	sd_byp	0	RW	0...Synchronous demodulator is used 1...Synchronous demodulator is bypassed	
4	gain_en	0	RW	0...Power down of the Gain stage 1...Enable Gain stage	
3	gain_byp	0	RW	0...Gain stage is used 1...Gain stage is bypassed	
2:0	gain_g	0	RW	Gain	
				Setting	**Gain**
				0	1
				1	2
				2	4
				3	8
				4	16
				5	32
				6	64
				7	don‘t use

Sync Demodulator Example

LED1 and LED2 should be modulated with 2kHz

Demodulated signal should be sampled with 20Hz for 1 second.

Calculation of sequencer values:

1. Modulation Frequency = 2kHz. Period = 500us.
2. Set sequencer period to 250us.
   -> seq_div=0, seq_period=500
3. Operation of LEDs between 0us and 100us (depends on LED and Amp-settings)
   -> seq_led_start=1, seq_led_stop=100
4. Operation of photo-amplifier and synchronous demodulator multipl. by +1 between 50us and 100us
   -> seq_sdp_start=50, seq_sdp_stop=100
5. Operation of photo-amplifier and synchronous demodulator multipl. by -1 between 300us and 350us
   -> seq_sdm1_start=300, seq_sdm1_stop=350
6. Sampling position at 495us + settling
   -> seq_adc=490
7. ADC should only sample at 20Hz (50ms). This means sampling at every 50ms/500us = 100th sequencer run.
   sd_subs=100
8. ADC values should be stored for 1 second. This means 1s/50ms = 20 samples must be stored.
   ->seq_count=20

Figure 54:
Sync Demodulator Example Detail

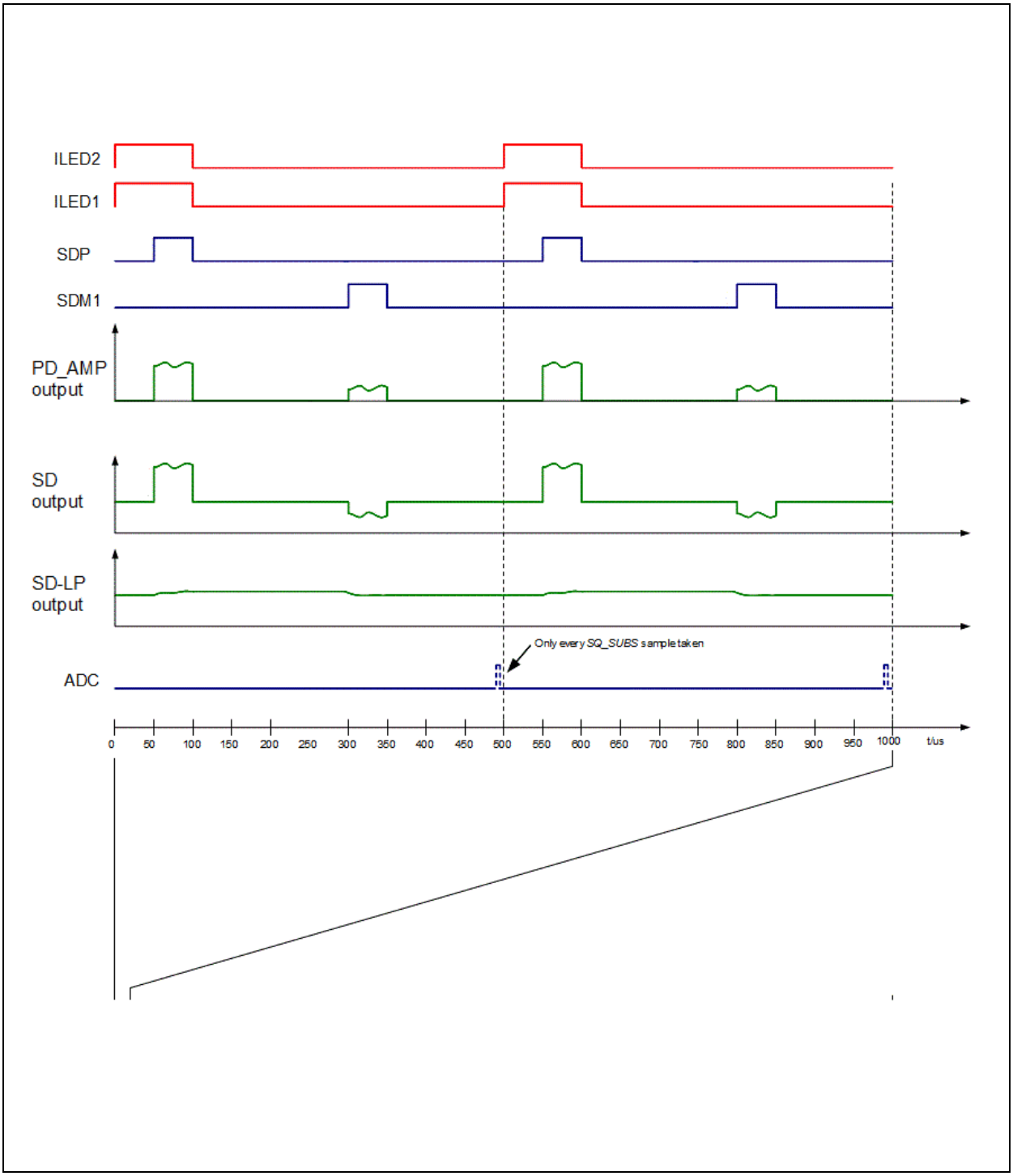
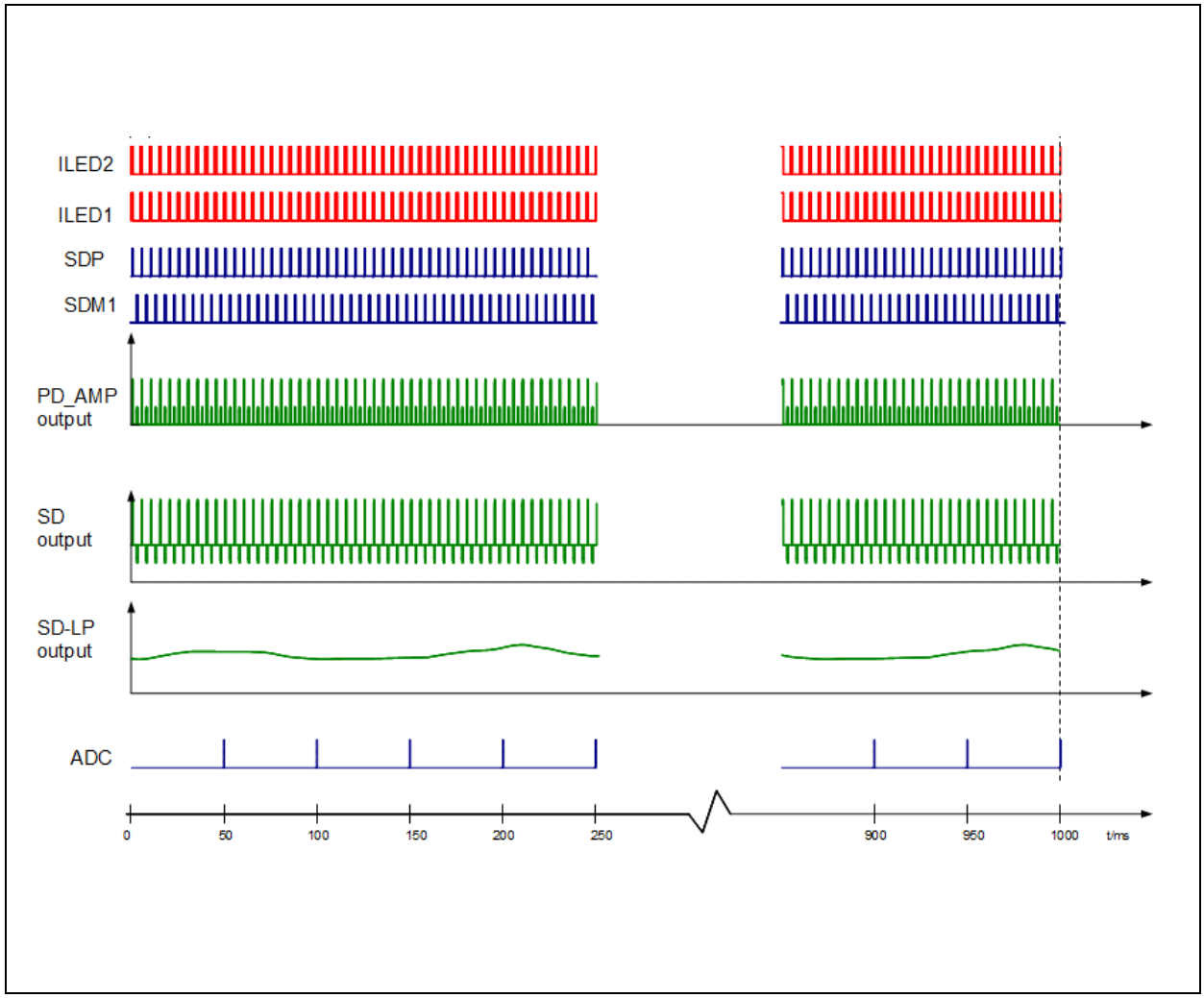


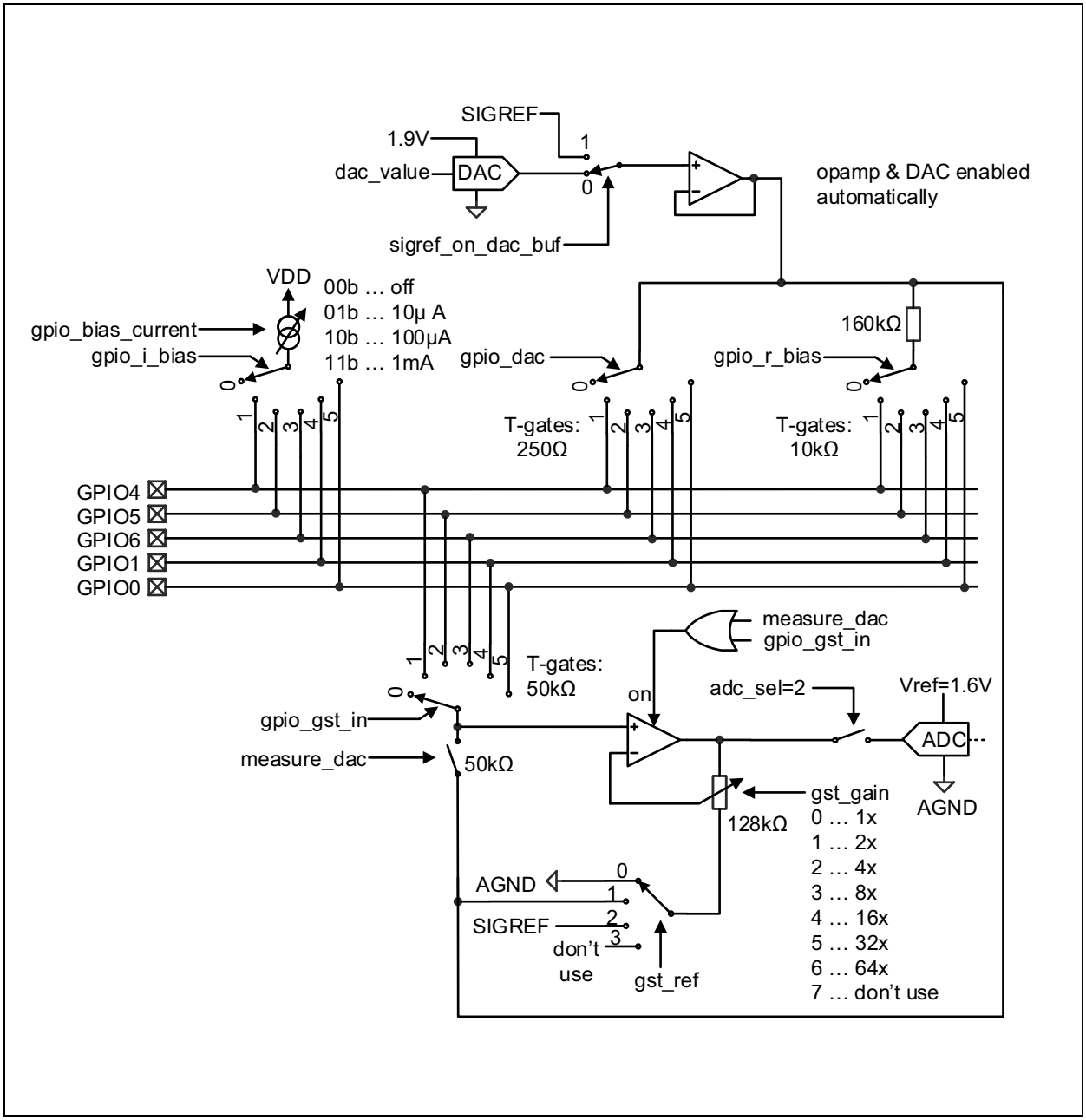
Figure 55:
Sync Demodulator Example



Electrical Analog Front End

The electrical analog front end consists of three identical signal paths with independent settings of bias condition, gain and offset.

Figure 56:
Electrical Analog Front End Internal Circuit



Note(s):

1. Resistor / T-gates resistance values are given as indication – do not rely on absolute values

Input Pins

Five general purpose pins can be used either as configurable GPIO for the processor or as analog input pins for the electrical analog front end. The analog inputs can be configured to setup different amplifier topologies.

AFE Registers

Figure 57:
AFE_LED_CFG

0x00: AFE_LED_CFG				
Field	**Name**	**Rst**	**Type**	**Description**
18	sigref_en	0	RW	Signal reference: Is required for all analog blocks 0...Disable signal reference 1...Enable signal reference

Figure 58:
AFE_EAF

0x90: AFE_EAF					
Field	**Name**	**Rst**	**Type**	**Description**	
25	sigref_on_dac_buf	0	RW	If asserted, connect SIGREF to DAC buffer.	
24	measure_dac	0	RW	If this bit is asserted, the DAC output is connected to the gain stage input (independent of gpio_gst_in selection, therefore the DAC output is measureable on the GPIO pin)	
18:16	gpio_dac	0	RW	DAC on GPIO	
				Setting	**Meaning**
				0	No DAC biasing
				1	DAC on GPIO4
				2	DAC on GPIO5
				3	DAC on GPIO6
				4	DAC on GPIO1
				5	DAC on GPIO0

0x90: AFE_EAF					
Field	**Name**	**Rst**	**Type**	**Description**	
15:13	gpio_r_bias	0	RW	Resistive biasing	
				Setting	**Meaning**
				0	No resistive biasing
				1	Resistive biasing on GPIO4
				2	Resistive biasing on GPIO5
				3	Resistive biasing on GPIO6
				4	Resistive biasing on GPIO1
				5	Resistive biasing on GPIO0
12:10	gpio_i_bias	0	RW	Current biasing	
				Setting	**Meaning**
				0	No current biasing
				1	Current biasing on GPIO4
				2	Current biasing on GPIO5
				3	Current biasing on GPIO6
				4	Current biasing on GPIO1
				5	Current biasing on GPIO0
9:8	gpio_bias_ current	0	RW	Current setting of gpio current bias	
				Setting	**Current**
				0	OFF
				1	10µA
				2	100µA
				3	1mA

0x90: AFE_EAF					
Field	**Name**	**Rst**	**Type**	**Description**	
7:5	gpio_gst_in	0	RW	Gain stage input selection	
				Setting	**Meaning**
				0	Not connected
				1	GPIO4
				2	GPIO5
				3	GPIO6
				4	GPIO1
				5	GPIO0
4:3	gst_ref	0	RW	Gain stage reference voltage	
				Setting	**Meaning**
				0	AGND
				1	DAC buffer
				2	SIGREF
				3	Reserved – do not use
2:0	gst_gain	0	RW	Gain stage gain	
				Setting	**Meaning**
				0	1
				1	2
				2	4
				3	8
				4	16
				5	32
				6	64
				7	Reserved – do not use

The AFE_EAF register is used to configure the electrical frontend

Figure 59:
AFE_EAF_DAC

0x94: AFE_EAF_DAC				
Field	**Name**	**Rst**	**Type**	**Description**
9:0	dac_value	0	RW	DAC value (10 bit) 0x000 … 0V 0x1FF … 1.9V

The AFE_EAF_DAC register is used to configure the dac value

Possible Configurations of Every Amplifier Stage

Figure 60:
Non Inverting Amplifier With Offset and Input Voltage Divider (Temperature Sensor)

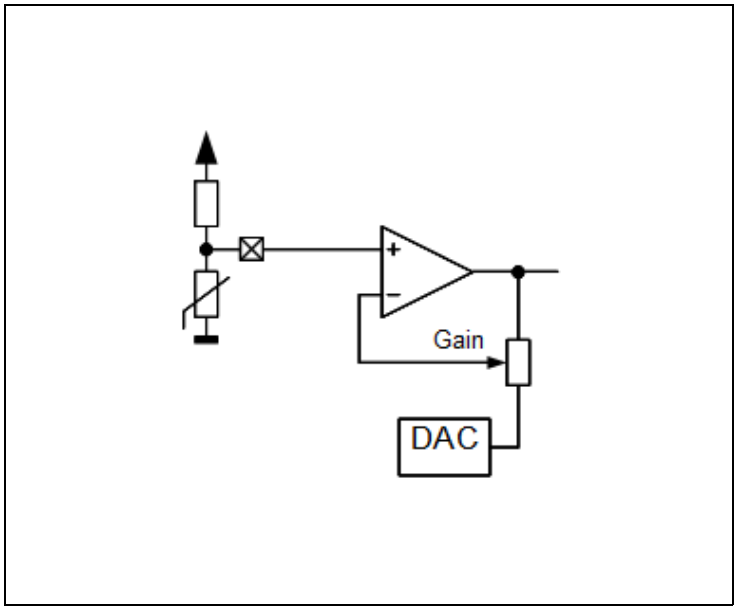


Figure 61:
Non Inverting Amplifier With Current Source and Offset (Temperature Sensor)

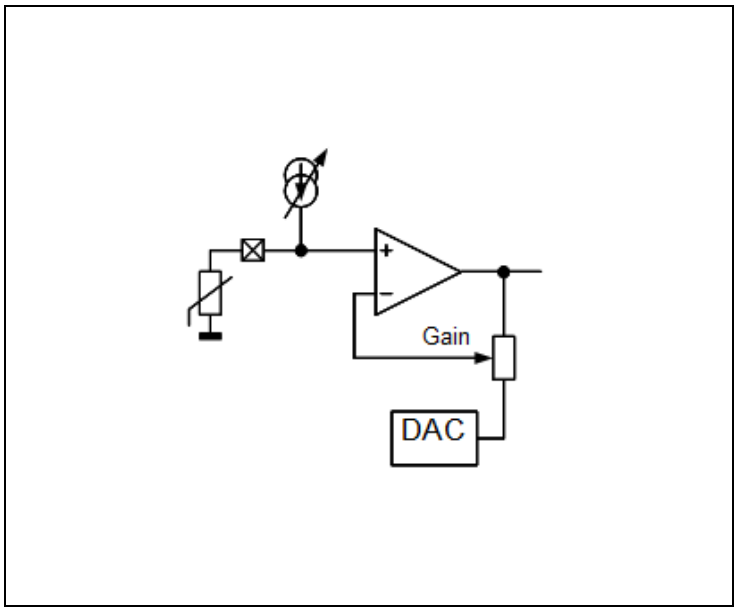


Figure 62:
Non Inverting Amplifier With Current Source and Reference Path (Temperature Sensor)

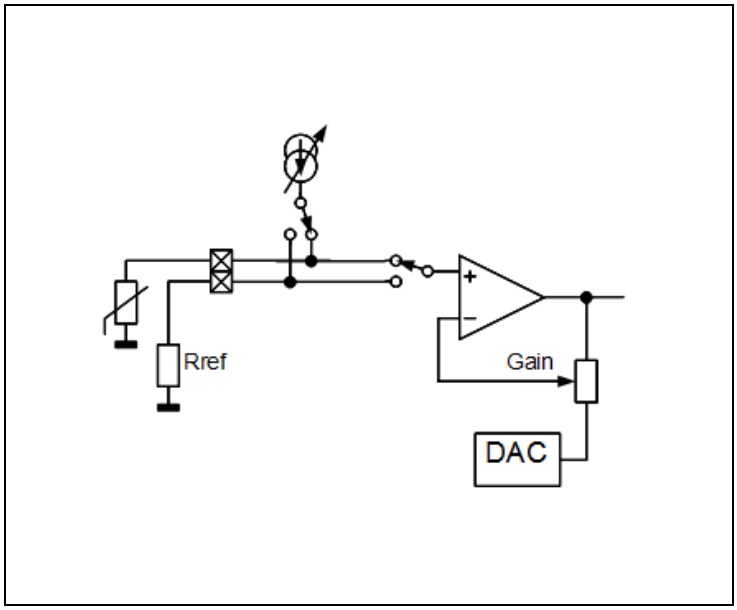


Figure 63:
Non Inverting Amplifier High Impedance, GND Referenced

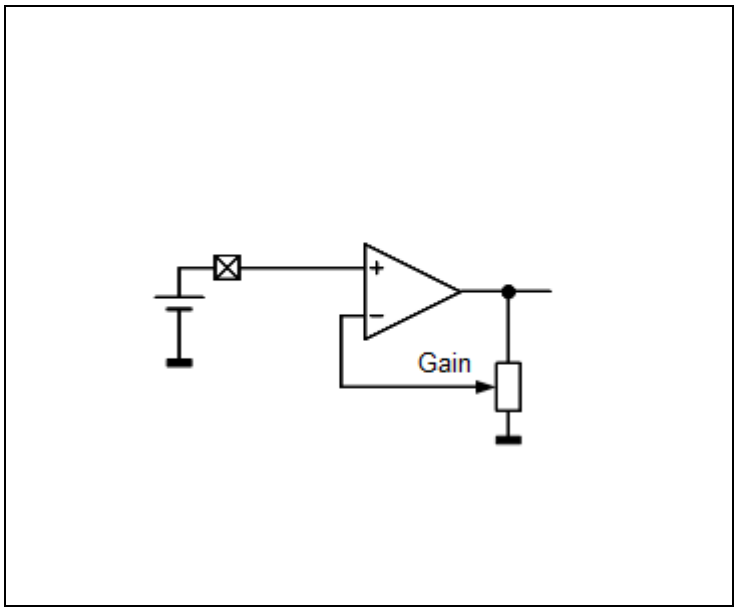


Figure 64:
Non Inverting Amplifier With DC-Blocking, Referenced to V_ADCRef/2

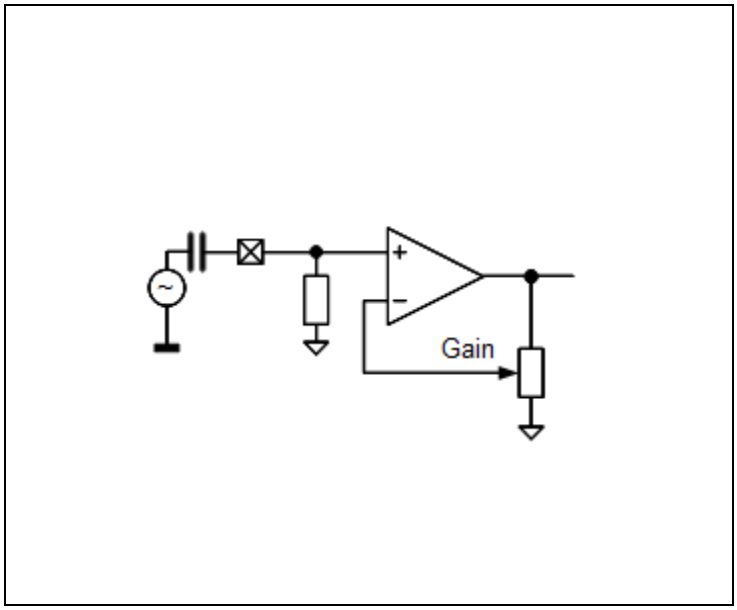
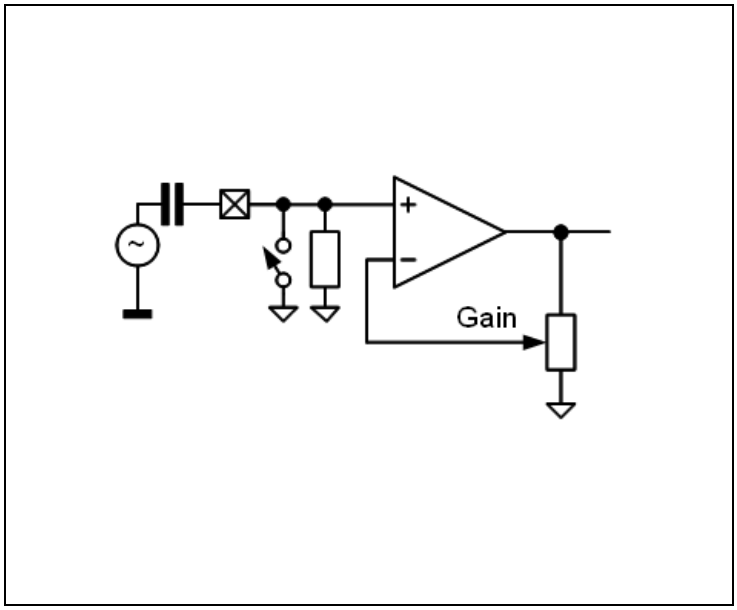


Figure 65:
Non Inverting Amplifier With DC-Blocking and Fast Settling Time, Referenced to ADCRef /2

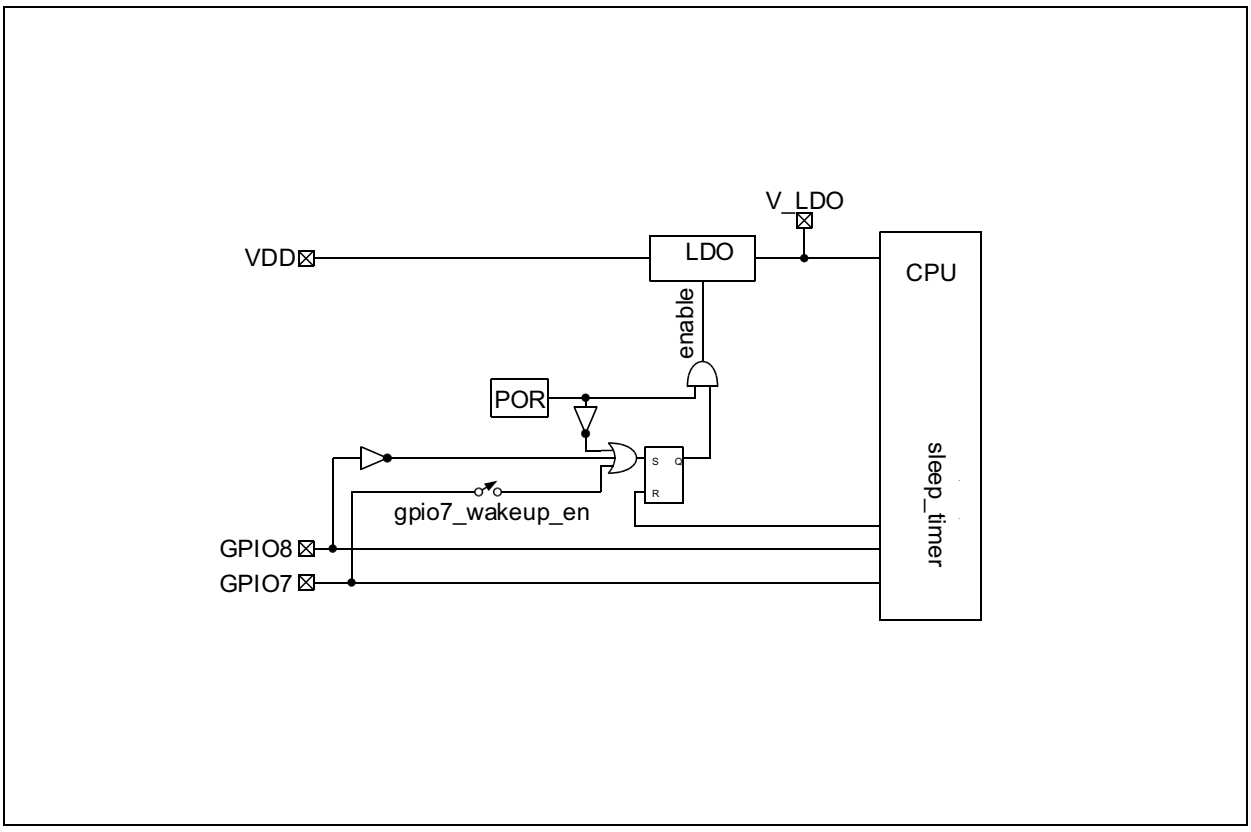


ADC

The ADC is a 14bit successive-approximation register (SAR) type. It supports 12 bit with very fast conversion time up to 1Msps and 14bit with moderate conversion time up to 250ksps.

The ADC is started by the sequencer and its timing or in manual mode (man_mode=1) by setting seq_start=1 (seq_start stays '1' as long as the conversion runs). The AS7000 can be configured to trigger an interrupt upon end of conversion.

Figure 66:
ADC Internal Circuit and Multiplexer



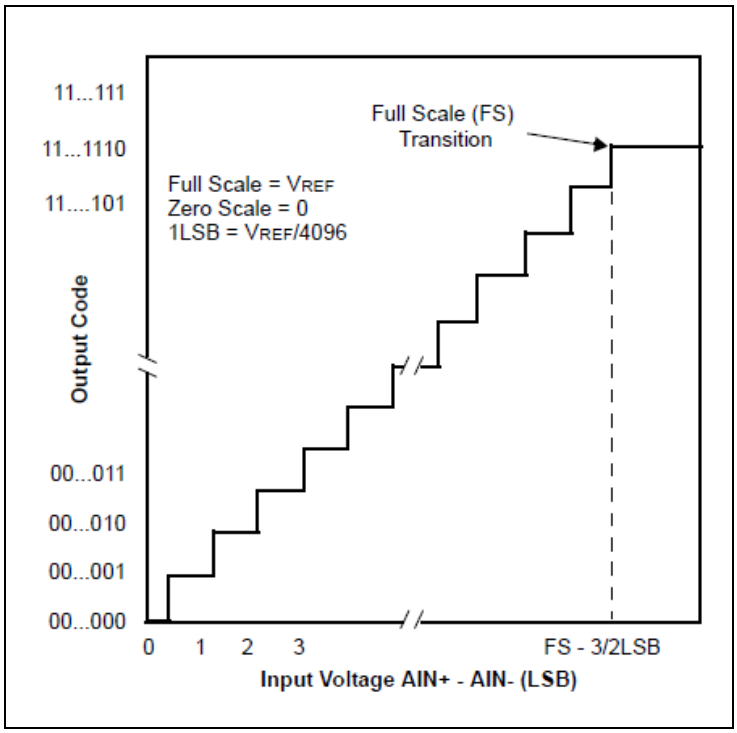
For best accuracy the ADC needs to recalibrate itself – use **ams** SDK to initiate the calibration procedure.

Figure 67:
Operating Characteristics of the ADC, VDD=3V, T_{AMB}=25°C (unless otherwise noted)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Vref	Reference voltage V_ADCRef			1.6		V
TCvref	Reference voltage temperature coefficient			±50		ppm/°C
	Resolution	adc_clock ≤ 1MHz Otherwise	14 12			Bit
INL	Relative accuracy		-8		8	LSB
DNL	Differential nonlinearity			±2		LSB
	Offset error			±8		LSB
	Gain error			±8		LSB
SNR	Signal-to-noise ratio	Fsample = 1kHz, Fsignal=100Hz		80		dB
THD	Total harmonic distortion	Fsample = 1kHz, Fsignal=100Hz		-70		dB
Tconv	Conversion rate	12 bit resolution	1			µs
Vin	Input voltage range		0		Vref	V

Figure 68:
ADC Output Codes (12 Bit Resolution Setting Range)

ADC Output Codes:
For 14 bit resolution the output data range is 0 to 16383, one LSB represents Vref/16384.



ADC Registers

Figure 69:
AFE_ADC_DATA

0x88: AFE_ADC_DATA				
Field	**Name**	**Rst**	**Type**	**Description**
13:0	adc_data	0	RO	Current ADC output signals

The ADC_DATA register shows the current raw output of the ADC.

Figure 70:
AFE_ADC_CFG

0xa4: AFE_ADC_CFG				
Field	**Name**	**Rst**	**Type**	**Description**
21	adc_selfpd	1	RW	1…Power down ADC when not converting; use this to conserve power, but set adc_settling_time to minimum 64µs to permit settling of the ADC reference buffer. 0 … Always enabled ADC
20	adc_discharge	1	RW	0…Suppress ADC capacitor discharging 1…Discharge ADC capacitor before tracking If asserted, the capacitor is discharged before the tracking phase. If zero, the discharge phase is suppressed and the tracking phase is started one cycle earlier.

<table>
<tr><th colspan="8">0xa4: AFE_ADC_CFG</th></tr>
<tr><th>Field</th><th>Name</th><th>Rst</th><th>Type</th><th colspan="4">Description</th></tr>
<tr><td rowspan="13">19:17</td><td rowspan="13">adc_settling_
time</td><td rowspan="13">5</td><td rowspan="13">RW</td><td colspan="4">ADC settling time: Do not use in interleaved mode. It defines the number of ADC clock cycles the sampling window is kept open additionally to its 4 ADC clock cycles. If the gain stage in the optical frontend is used (gain_ byp=0), set this to minimum 8µs. If adc_selfpd=1, set this to minimum 64µs and set adc_discharge=1.</td></tr>
<tr><td>Setting</td><td>Periods</td><td>µs (@4MHz)</td><td>µs (@2MHz)</td><td>µs (@1MHz)</td></tr>
<tr><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td></tr>
<tr><td>1</td><td>4</td><td>1</td><td>2</td><td>4</td></tr>
<tr><td>2</td><td>8</td><td>2</td><td>4</td><td>8</td></tr>
<tr><td>3</td><td>16</td><td>4</td><td>8</td><td>16</td></tr>
<tr><td>4</td><td>32</td><td>8</td><td>16</td><td>32</td></tr>
<tr><td>5</td><td>64</td><td>16</td><td>32</td><td>64</td></tr>
<tr><td>6</td><td>128</td><td>32</td><td>64</td><td>128</td></tr>
<tr><td>7</td><td>256</td><td>64</td><td>128</td><td>256</td></tr>
<tr><td colspan="4">If adc_discharge=0 and adc_selfpd=0 and the TIA is connected directly to the ADC using following minimum settling times:</td></tr>
<tr><td colspan="2">pd_ampres</td><td colspan="2">minimum adc_settling_time</td></tr>
<tr><td colspan="2">1MΩ</td><td colspan="2">1µs</td></tr>
<tr><td colspan="2">2MΩ-7MΩ</td><td colspan="2">2µs</td></tr>
<tr><td colspan="2">10MΩ-15MΩ</td><td colspan="2">3µs</td></tr>
</table>

<table>
<tr><th colspan="5">0xa4: AFE_ADC_CFG</th></tr>
<tr><th>Field</th><th>Name</th><th>Rst</th><th>Type</th><th>Description</th></tr>
<tr><td rowspan="17">15:12</td><td rowspan="17">adc_clock</td><td rowspan="17">7</td><td rowspan="17">RW</td><td>ADC clock divider: The ADC clock is freely configurable. Note that values other than 4MHz, 2MHz, 1MHz and 500kHz will make the resulting timing very confusing for the human observer.</td></tr>
<tr><td>
<table>
<tr><th>Setting</th><th>Periods</th><th>ns</th><th>kHz</th></tr>
<tr><td>0</td><td>2</td><td>125</td><td>8000</td></tr>
<tr><td>1</td><td>4</td><td>250</td><td>4000</td></tr>
<tr><td>2</td><td>6</td><td>375</td><td>2666</td></tr>
<tr><td>3</td><td>8</td><td>500</td><td>2000</td></tr>
<tr><td>4</td><td>10</td><td>625</td><td>1600</td></tr>
<tr><td>5</td><td>12</td><td>750</td><td>1333</td></tr>
<tr><td>6</td><td>14</td><td>875</td><td>1142</td></tr>
<tr><td>7</td><td>16</td><td>1000</td><td>1000</td></tr>
<tr><td>8</td><td>18</td><td>1125</td><td>888</td></tr>
<tr><td>9</td><td>20</td><td>1250</td><td>800</td></tr>
<tr><td>10</td><td>22</td><td>1375</td><td>727</td></tr>
<tr><td>11</td><td>24</td><td>1500</td><td>666</td></tr>
<tr><td>12</td><td>26</td><td>1625</td><td>615</td></tr>
<tr><td>13</td><td>28</td><td>1750</td><td>571</td></tr>
<tr><td>14</td><td>30</td><td>1875</td><td>533</td></tr>
<tr><td>15</td><td>32</td><td>2000</td><td>500</td></tr>
</table>
</td></tr>
<tr><td>11</td><td>adc_calibration</td><td>0</td><td>RW</td><td>To activate self calibration, this bit must be asserted, and an ADC “conversion” has to be started in manual mode (man_mode=1) by asserting seq_start. It is suggested to let the CPU sleep and wait for the ADC interrupt. Also, a slow ADC clock should be used.</td></tr>
<tr><td>10</td><td>adc_interleave</td><td>0</td><td>RW</td><td>Interleave mode</td></tr>
<tr><td>9</td><td>adc_en</td><td>0</td><td>RW</td><td>0...Reset ADC
1...Enable ADC
Warning: In reset state the ADC clears its calibration data. Re-calibration is necessary next time it is enabled again.</td></tr>
</table>

<table>
<tr><th colspan="5">0xa4: AFE_ADC_CFG</th></tr>
<tr><th>Field</th><th>Name</th><th>Rst</th><th>Type</th><th>Description</th></tr>
<tr><td>8:6</td><td>adc_sel</td><td>0</td><td>RW</td><td>ADC Input Select
0… Trans impedance amplifier – see Figure 8

1… Optical frontend – see Figure 8

2… Electrical front end – see Figure 56

3… Do not use
4… Do not use
5… Temperature sensor (diode with approx. -2mV/K)
6… Do not use
7… Do not use</td></tr>
<tr><td rowspan="3">4</td><td rowspan="3">adc_highres</td><td rowspan="3">1</td><td rowspan="3">RW</td><td colspan="2">ADC resolution depending on the Sampling speed</td></tr>
<tr><td>Setting</td><td>Selection</td></tr>
<tr><td>0</td><td>12 bit</td></tr>
<tr><td rowspan="10">3:1</td><td rowspan="10">adc_multi_n</td><td rowspan="10">0</td><td rowspan="10">RW</td><td colspan="2">Defines number of samples that are taken in multimode (adc_multimode =1)</td></tr>
<tr><td>Setting</td><td>Sample Period</td></tr>
<tr><td>1</td><td>4</td></tr>
<tr><td>2</td><td>8</td></tr>
<tr><td>3</td><td>16</td></tr>
<tr><td>4</td><td>32</td></tr>
<tr><td>5</td><td>48</td></tr>
<tr><td>6</td><td>64</td></tr>
<tr><td>7</td><td>96</td></tr>
</table>

0xa4: AFE_ADC_CFG				
Field	Name	Rst	Type	Description
0	adc_multimode	0	RW	0...If ADC is started one sample is measured 1...If ADC is started multiple samples are measured with "adc_multi_fs" interval and stored to memory by the DMA controller. The number of samples is defined with adc_multi_n. In interleaved mode, the sampling time is 4x higher than in non-interleave mode. In non-interleave mode, if adc_multimode=0, only 1 sample is taken. In interleave mode, if adc_multimode=0, then ADC conversions are executed until the end of the sequencer period. If adc_multimode=1, then adc_multi_n is always taken into account.

Power Management and Operating Modes

After the supply (VDD) is asserted the AS7000 automatically starts up. It is up to the application software into which operating mode the AS7000 is changed (e.g. to power down mode).

The AS7000 can operate in following modes:

Figure 71:
AS7000 Operating Modes

Mode	Internal LDO (V_LDO)	512Hz Oscillator	16MHz Oscillator	CPU	Wake Up CPU to Active Mode By	Entered By
Active	✓	✓	✓	Running	-	-
Sleep mode	✓	✓	✓	Idle	Any interrupt (any timer, GPIO)	__WFI() command of CPU
Deep sleep mode	✓	✓	×	× = reset; registers keep content	512Hz sleep_counter, GPIO7(1) and GPIO8(2)	Use **ams** SDK for entering deep sleep
Power down	×	×	×	× = reset; registers are reset	GPIO7(1) and GPIO8(3)	enter_powerdown=1

Note(s):

1. Wakeup by GPIO7=high if gpio7_wakeup_en=1; applies for power down and deep sleep mode.
2. Wakeup by GPIO8=low if gpio8_wakeup_en=1.
3. In power down mode the AS7000 will always wakeup if GPIO8=low independent of previous setting of gpio8_wakeup_en.

For operation of the sequencer the 16MHz oscillator is required, therefore the sequencer only operates in active or wait for interrupt mode.

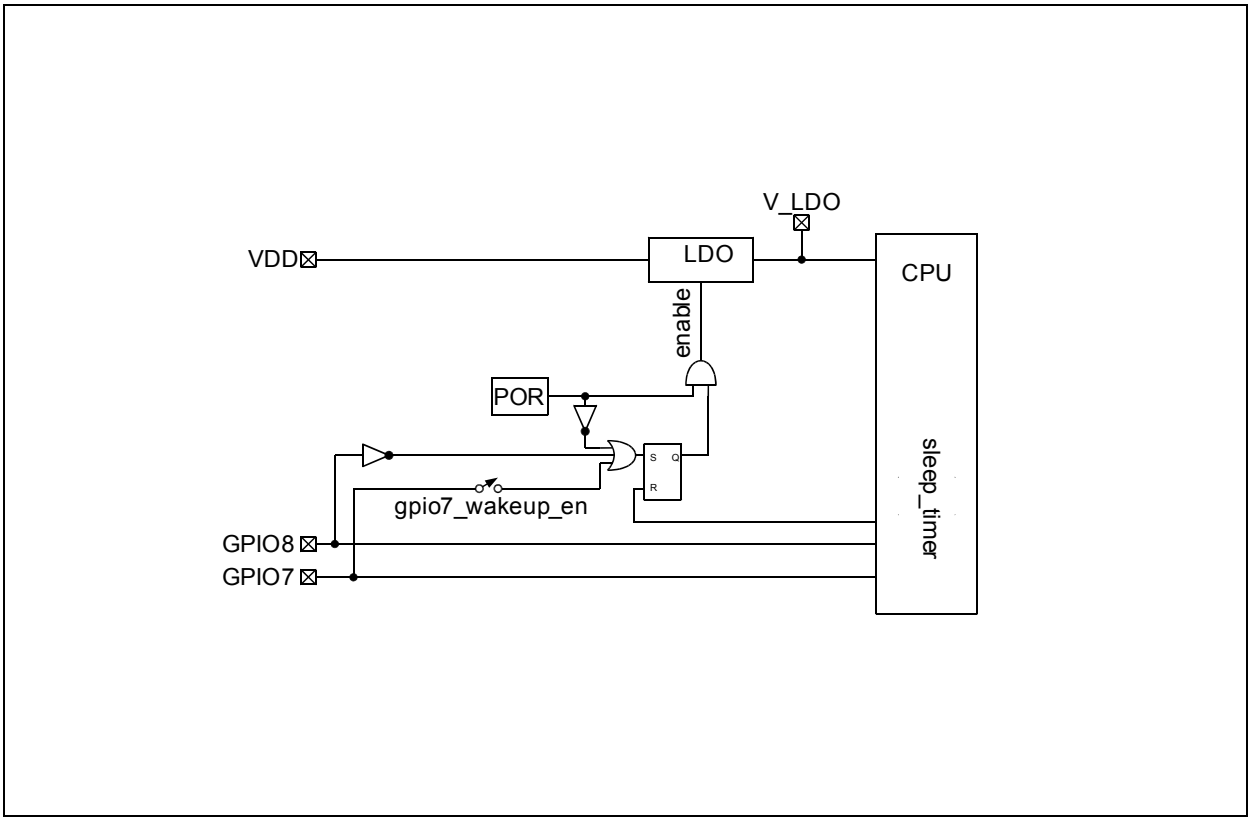
Clock Control Unit (CCU) for Peripheral Blocks

All peripheral block have a reset bit and a clock enable bit. The purpose of these register bits is to disable clock to them when they are not used and therefore reduce power consumption.

Note(s): Access to the register is not possible if the clock to the peripheral is disabled or reset is asserted.
e.g. to access any register of AFE (like optical analog front end) set the register bits afe_resetn=1 and afe_enable=1.

Wake-Up From Power Down Mode

Figure 72:
Wake-Up Logic From Power Down Mode



Power Management And Operating Modes Registers

In order to operate the different blocks inside the AS7000, the block has to be enabled (e.g. gpio_enable=1) and the reset de-asserted (e.g. gpio_resetn=1).

Figure 73:
CCU_DEVICEID

0x00: CCU_DEVICEID				
Field	**Name**	**Rst**	**Type**	**Description**
31:16	device_id	0	RO	Reads back 0x1b58 (decimal 7000) ("AS7000")
3:0	revision	0	RO	Reads back the silicon revision

Figure 74:
CCU_GPIO

0x20: CCU_GPIO				
Field	**Name**	**Rst**	**Type**	**Description**
0	gpio_resetn	0	RW	0=reset 1=running
1	gpio_enable	0	RW	0=clock OFF 1=clock ON

Figure 75:
CCU_I2CM

0x2c: CCU_I2CM				
Field	**Name**	**Rst**	**Type**	**Description**
0	i2cm_resetn	0	RW	0=reset 1=running
1	i2cm_enable	0	RW	0=clock OFF 1=clock ON

Figure 76:
CCU_I2CS

0x30: CCU_I2CS				
Field	Name	Rst	Type	Description
0	i2cs_resetn	0	RW	0=reset 1=running
1	i2cs_enable	0	RW	0=clock OFF 1=clock ON

Figure 77:
CCU_UART

0x34: CCU_UART				
Field	Name	Rst	Type	Description
0	uart_resetn	0	RW	0=reset 1=running
1	uart_enable	0	RW	0=clock OFF 1=clock ON

Figure 78:
CCU_TMR

0x38: CCU_TMR				
Field	Name	Rst	Type	Description
0	tmr_resetn	0	RW	0=reset 1=running
1	tmr_enable	0	RW	0=clock OFF 1=clock ON

Figure 79:
CCU_AFE

0x3c: CCU_AFE				
Field	Name	Rst	Type	Description
0	afe_resetn	0	RW	0=reset 1=running
1	afe_enable	0	RW	0=clock OFF 1=clock ON

Figure 80:
CCU_WD_CTRL

0x40: CCU_WD_CTRL				
Field	**Name**	**Rst**	**Type**	**Description**
0	wd_en	0	RW	Enable watchdog timer
1	wd_irq_msk	0	RW	If 1, pass wd_irq to system NMI input
2	wd_reset_msk	0	RW	If 1, then reset system in case of wd_reset

Figure 81:
CCU_WD_STATUS

0x44: CCU_WD_STATUS				
Field	**Name**	**Rst**	**Type**	**Description**
0	wd_irq	0	SS_WC	Watchdog timer has reached interrupt level
1	wd_reset	0	SS_WC	Watchdog has reached zero
2	wd_irq_intr	0	RO	NMI is currently asserted by watchdog

Figure 82:
CCU_WD_VAL

0x48: CCU_WD_VAL				
Field	**Name**	**Rst**	**Type**	**Description**
23:0	wd_value	0	R_PUSH	Reload the watchdog counter with this value. The watchdog counter counts down, and it triggers a system reset as soon as it reaches zero.

Figure 83:
CCU_WD_IRQVAL

0x4c: CCU_WD_IRQVAL				
Field	**Name**	**Rst**	**Type**	**Description**
23:0	wd_irq_value	0	RW	If the watchdog counter reached this value, it will trigger an NMI as an early warning, if wd_irq_msk is set.

Figure 84:
CCU_LP_CFG

0x60: CCU_LP_CFG				
Field	**Name**	**Rst**	**Type**	**Description**
15:0	sleep_counter	0	RW	When going into low power sleep, this the sleep counter start value in slow clock ticks. As soon as it reaches zero, the CPU will wake up (if the register was written with a non zero value)
16	gpio7_wakeup_en	0	RW	If asserted, setting GPIO7 to high can wake up the chip as well (from both sleep and powerdown)
17	gpio8_wakeup_en	0	RW	If asserted, setting GPIO8 to low can wake up the chip from deep sleep (GPIO8=low always wakes up from powerdown)

The CCU_LP registers controls the low power modes

Figure 85:
CCU_LP_CTRL

0x64: CCU_LP_CTRL				
Field	**Name**	**Rst**	**Type**	**Description**
0	enter_sleep	0	W	Writing a 1 here makes the system enter deep sleep mode (wakeup by counter reaching zero) (1)
1	enter_powerdown	0	W	Writing a 1 here makes the system enter power down mode (wakeup by GPIO)

Note(s):

1. Only use **ams** SDK to enter deep sleep mode, do not set bit directly.

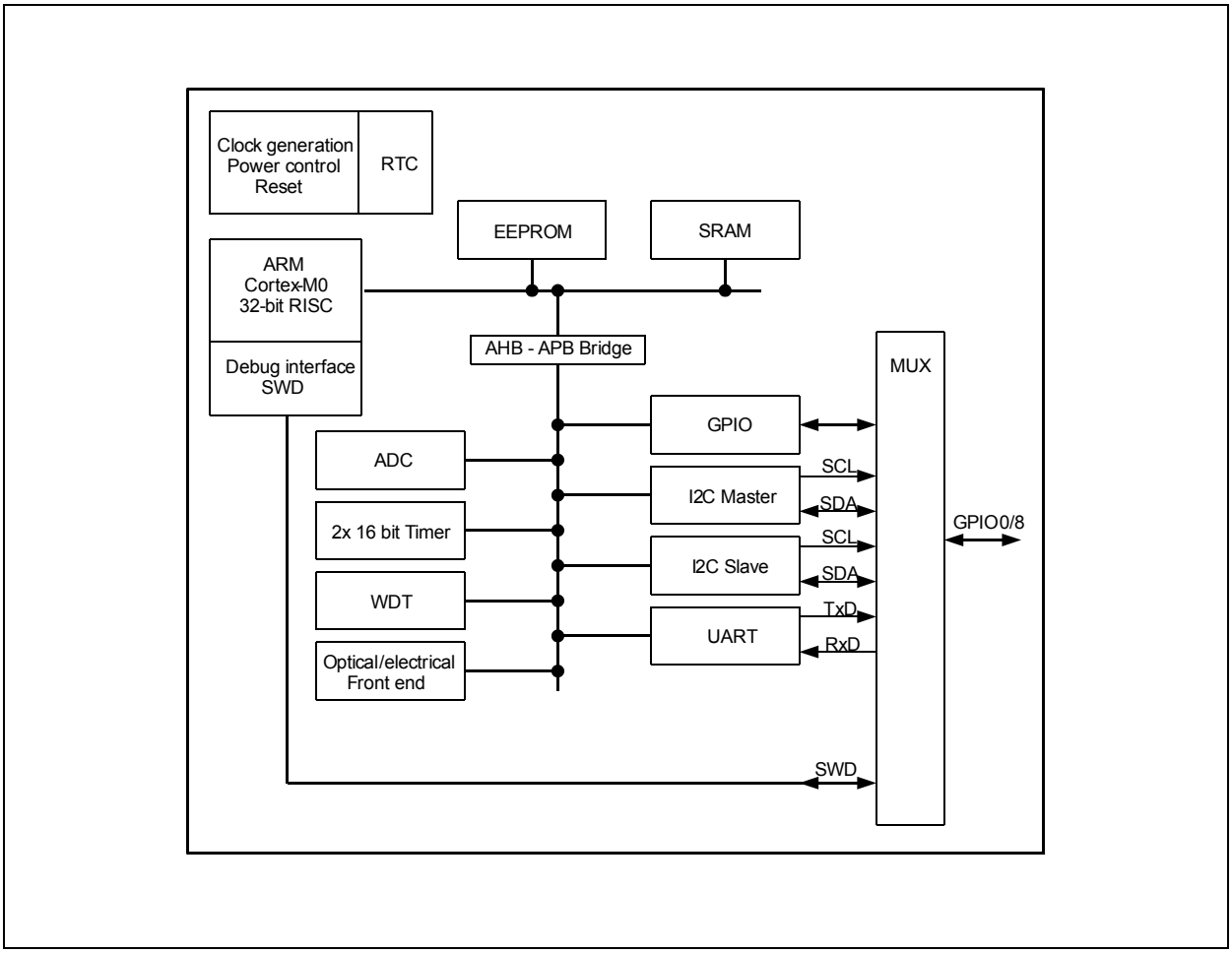
MCU

The MCU is a 32-bit ARM Cortex-M0-based RISC processor with 32kB of EEPROM memory and 4kB of RAM data memory. Details of the core processor can be found under infocenter.arm.com.

The MCU offers the following features:

- System:
  - ARM Cortex M0 processor with single cycle 32 bit multiplication instruction
  - System tick timer
  - Hardware protection to disable the read or read/write of the internal EEPROM and SRAM
  - Unique ID for every device delivered
- Memory:
  - 32kByte EEPROM memory
  - 4kByte RAM
- Peripherals:
  - 9 general-purpose (GPIO) pins with configurable output structure
  - UART
  - I^2C Master
  - I^2C Slave
  - 14 bit ADC
  - Watchdog timer
  - 2 general purpose 16 bit timer
- Clock:
  - Internal 16MHz RC oscillator
  - Internal 512Hz watchdog oscillator and timer
- Debug:
  - Serial wire Debug
- Power control:
  - Reduced power modes Sleep, Stop
  - Power ON reset

Figure 86:
CPU Internal Block Diagram



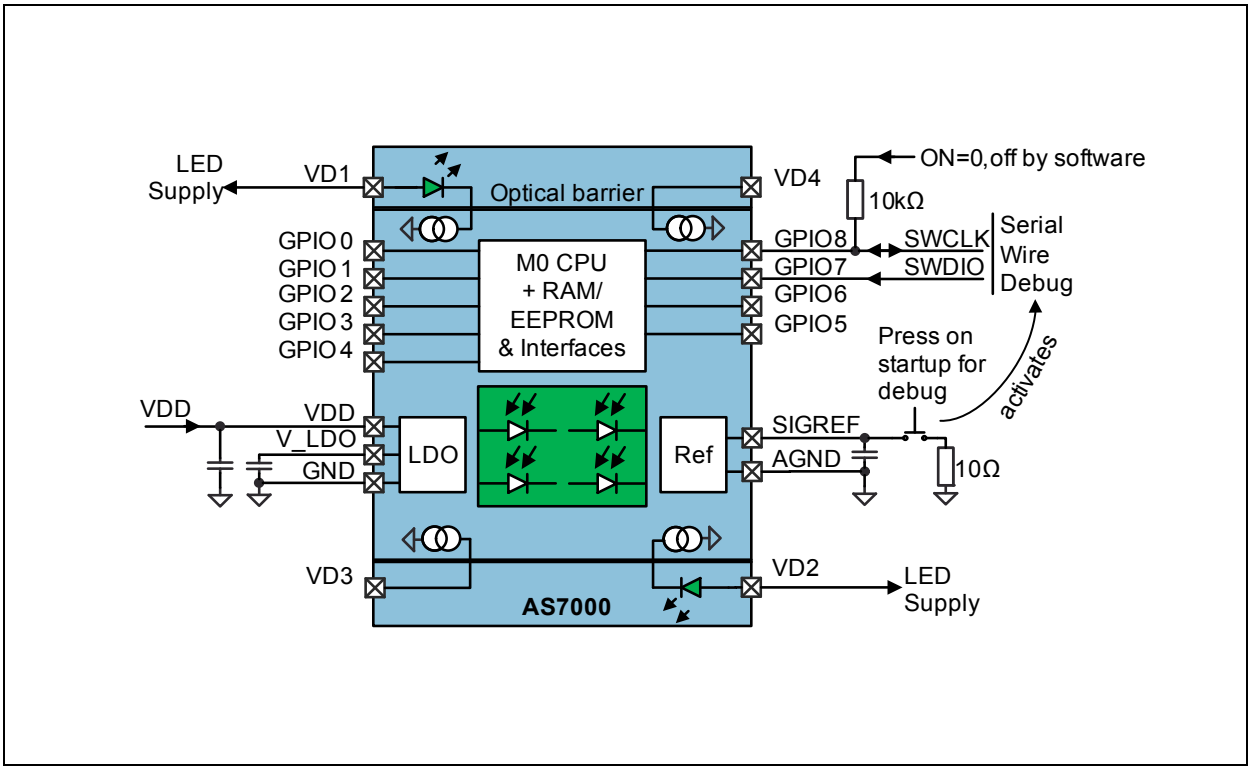
ams delivers a SDK (Software Development Kit) for easy access of the internal digital and analog blocks. The SDK includes detailed documentation of the hardware (like I^2C, UART) and includes low level drivers.

For accessing of the peripheral registers, a base address needs to added. The base address depends on the block used (see also **ams** provided SDK – software development kit).

Base Address	Function
0x40000000	CCU: Chip control unit
0x40010000	GPIO
0x40040000	I2CM: I2C Master
0x40050000	I2CS: I2C Slave
0x40060000	UART
0x40070000	Timers
0x40080000	AFE: Analog frontend controller

Debug – SWD

Figure 87:
Program/Debug



Note(s):

1. Press debug button on power-up (VDD ON).

During power up of the AS7000 the device checks if the pin SIGREF is shorted to GND (e.g. by a resistance of 10Ω) – see Figure 87. If this condition is detected and the security bit is not set, a monitor mode is entered.

In this monitor mode the AS7000 waits 5s where a debugger can be connected. If the 10s expires without a debugger connected, the AS7000 continues startup.

If a debugger is connected, the debugger can control AS7000 as required.

Note(s): If the security bit is set inside the EEPROM the debugger is bypassed even if SIGREF is shorted to GND upon startup.

GPIO Pins and Output Switch Matrix

A flexible output switch matrix allows dynamic assignment of the internal digital blocks to the GPIO pins:

Figure 88:
Output Switch Matrix

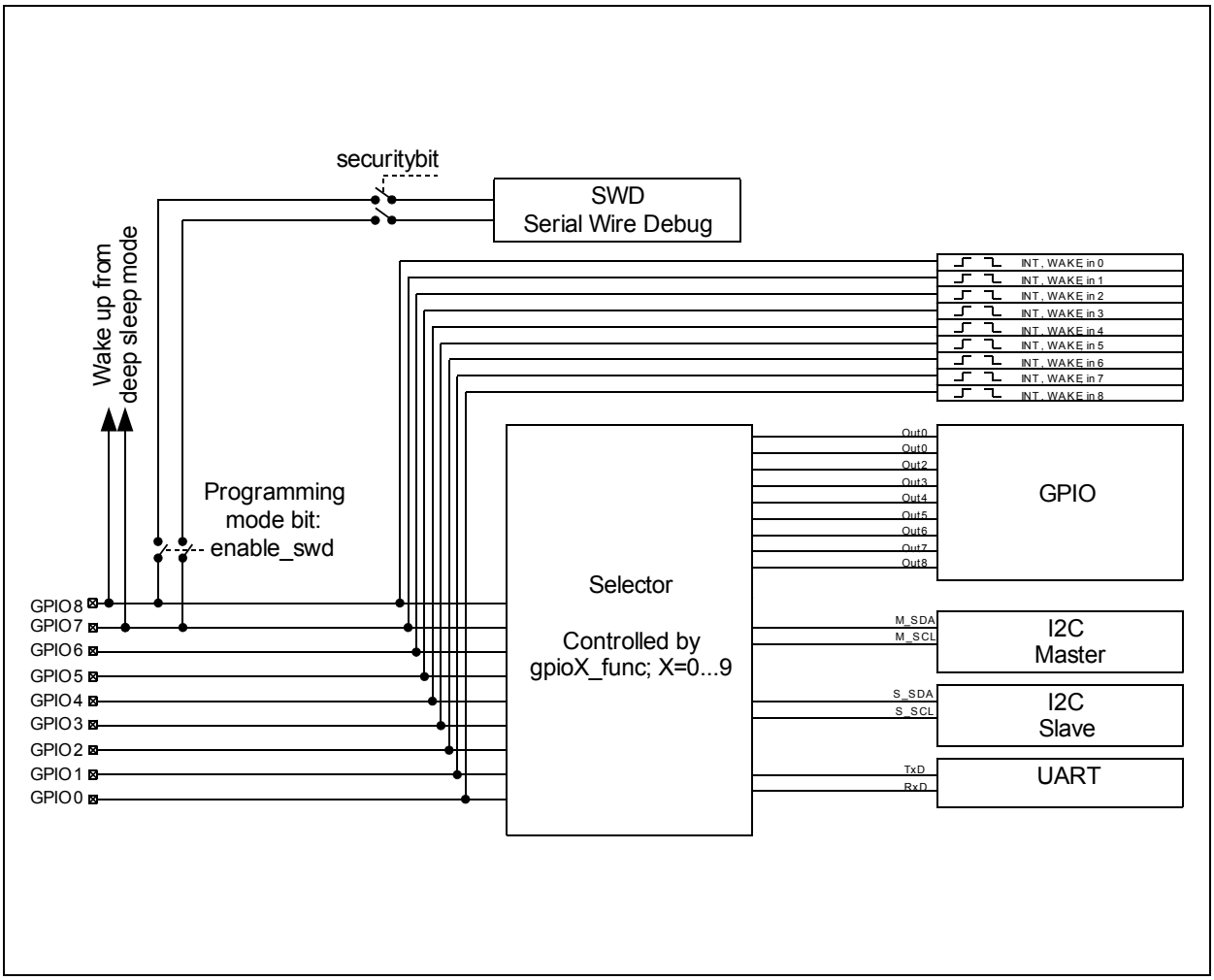
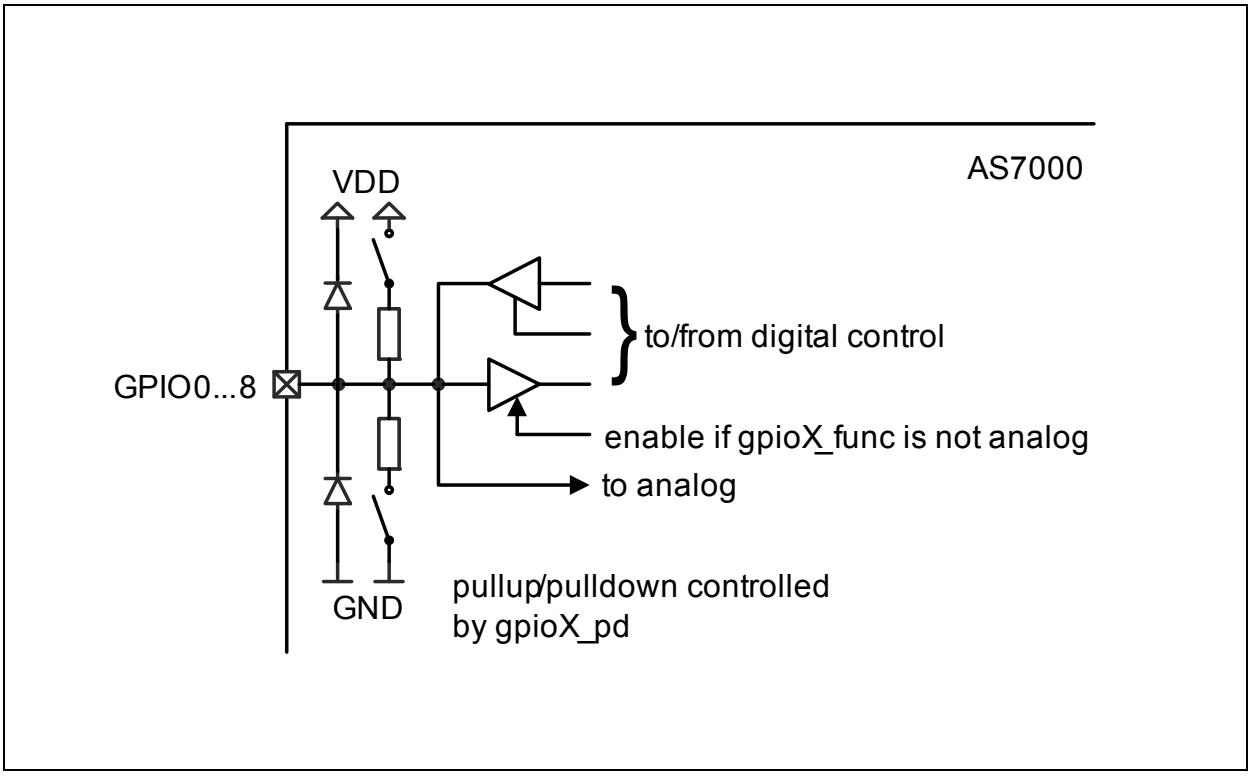


Figure 89:
Selector Assignments

Interface	GPIO	I²C Master	I²C Slave	UART	Analog
gpioX_func; X=0…8	000	011	100	101	111
GPIO0	I/O	M_SDA	S_SDA	TxD	Ana0
GPIO1	I/O	M_SCL	S_SCL	RxD	Ana1
GPIO2	I/O	M_SDA	S_SDA	TxD	Ana2
GPIO3	I/O	M_SCL	S_SCL	RxD	Ana3
GPIO4	I/O	M_SDA	S_SDA	TxD	Ana4
GPIO5	I/O	M_SCL	S_SCL	RxD	Ana5
GPIO6	I/O	M_SDA	S_SDA	TxD	Ana6
GPIO7	I/O	M_SCL	S_SCL	RxD	Ana7
GPIO8	I/O	M_SDA	S_SDA	TxD	Ana8

Each of the GPIO pins is capable of adding a pullup and/or pulldown:

Figure 90:
GPIO Internal Circuit



I²C Mode

The AS7000 includes an I²C master and slave (independent) hardware block. The pins name SDA and SCL in this section can be mapped during runtime to the GPIO pins according to Figure 89. **ams** SDK operates the I²C slave on GPIO2 (=SDA) and GPIO3 (=SCL) and uses a default I²C address of 0x30 (7-bit format; R/W bit has to be added) respectively 60h (8-bit format for writing) and 61h (8-bit format for reading). It expects external pullup resistors.

I²C Serial Control Interface

I²C Feature List:

Fast mode (400kHz) and standard mode (100kHz) support

7+1-bit addressing mode

Write formats: Single-Byte-Write, Page-Write

Read formats: Current-Address-Read, Random-Read, Sequential-Read

SDA input delay and SCL spike filtering by integrated RC-components

I²C Protocol

Figure 91:
I²C Symbol Definition

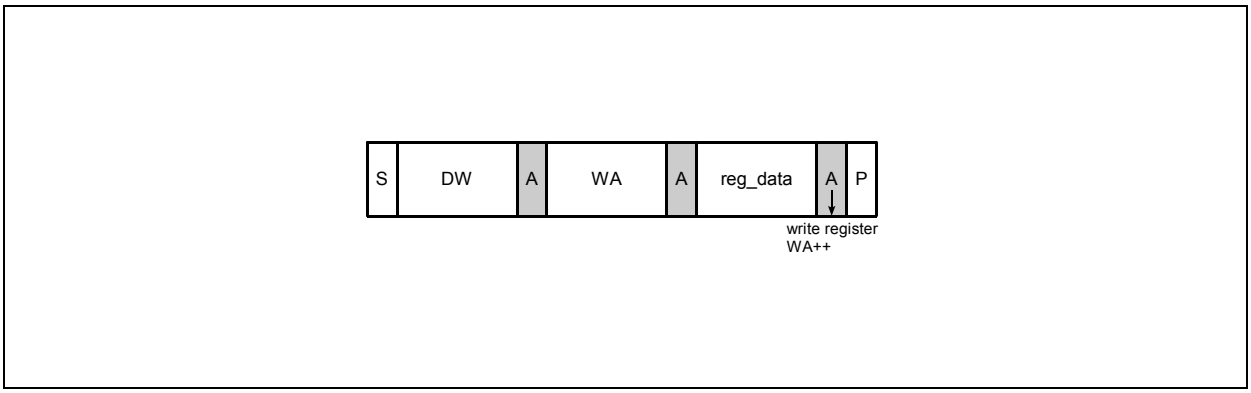
Symbol	Definition	RW	Note
S	Start condition after stop	R	1 bit
Sr	Repeated start	R	1 bit
DW	Device address for write	R	0110 0000b (60h)
DR	Device address for read	R	0110 0001b (61h)
WA	Word address	R	8 bit
A	Acknowledge	W	1 bit
N	No Acknowledge	R	1 bit
reg_data	Register data/write	R	8 bit
data (n)	Register data/read	W	8 bit
P	Stop condition	R	1 bit
WA++	Increment word address internally	R	During acknowledge

I²C Symbol Definition: Shows the symbols used in the following mode descriptions.

I²C Write Access

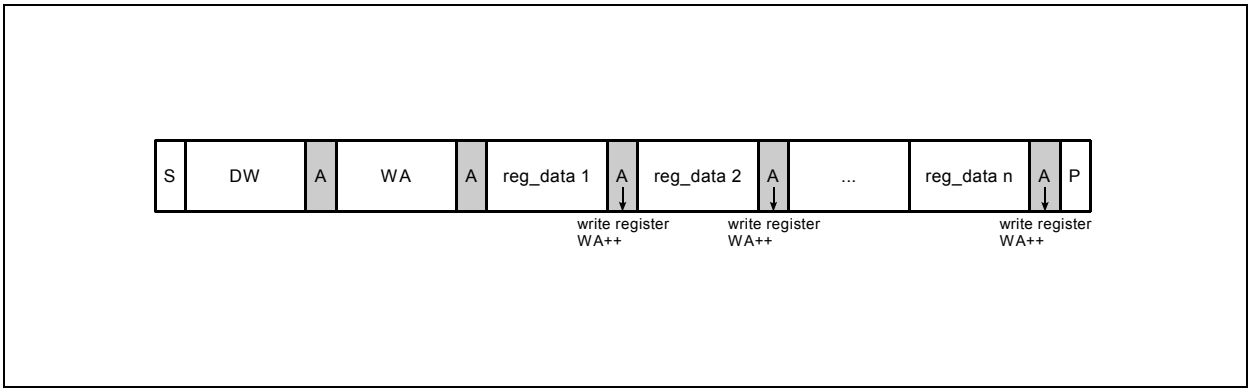
Byte Write and Page Write formats are used to write data to the slave.

Figure 92:
I²C Byte Write



I²C Byte Write: Shows the format of an I²C byte write access.

Figure 93:
I²C Page Write



I²C Page Write: Shows the format of an I²C page write access.

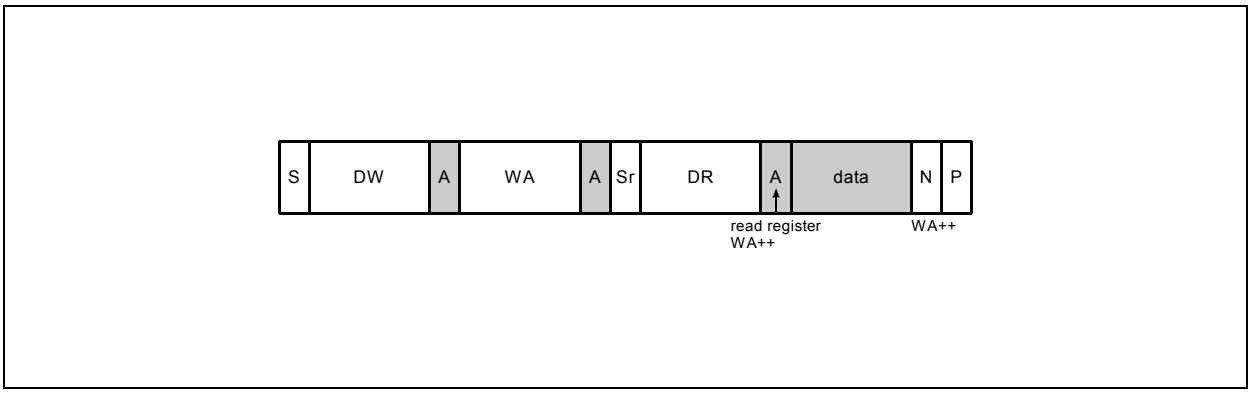
The transmission begins with the START condition, which is generated by the master when the bus is in IDLE state (the bus is free). The device-write address is followed by the word address. After the word address any number of data bytes can be sent to the slave. The word address is incremented internally, in order to write subsequent data bytes on subsequent address locations.

For reading data from the slave device, the master has to change the transfer direction. This can be done either with a repeated START condition followed by the device-read address, or simply with a new transmission START followed by the device-read address, when the bus is in IDLE state. The device-read address is always followed by the 1st register byte transmitted from the slave. In Read Mode any number of subsequent register bytes can be read from the slave. The word address is incremented internally.

I²C Read Access

Random, Sequential and Current Address Read are used to read data from the slave.

Figure 94:
I²C Random Read



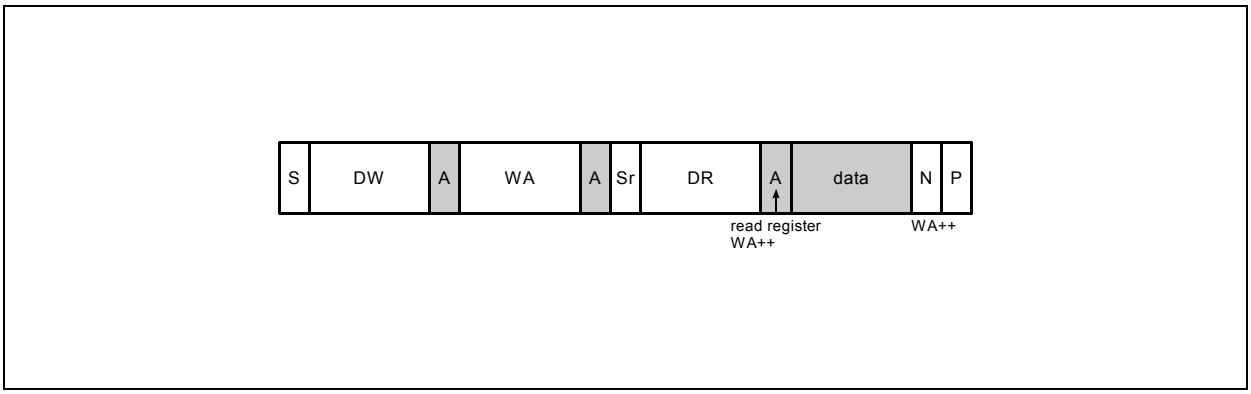
I²C Random Read: Shows the format of an I²C random read access.

Random Read and Sequential Read are combined formats. The repeated START condition is used to change the direction after the data transfer from the master.

The word address transfer is initiated with a START condition issued by the master while the bus is idle. The START condition is followed by the device-write address and the word address.

In order to change the data direction a repeated START condition is issued on the 1st SCL pulse after the acknowledge bit of the word address transfer. After the reception of the device-read address, the slave becomes the transmitter. In this state the slave transmits register data located by the previous received word address vector. The master responds to the data byte with a not-acknowledge, and issues a STOP condition on the bus.

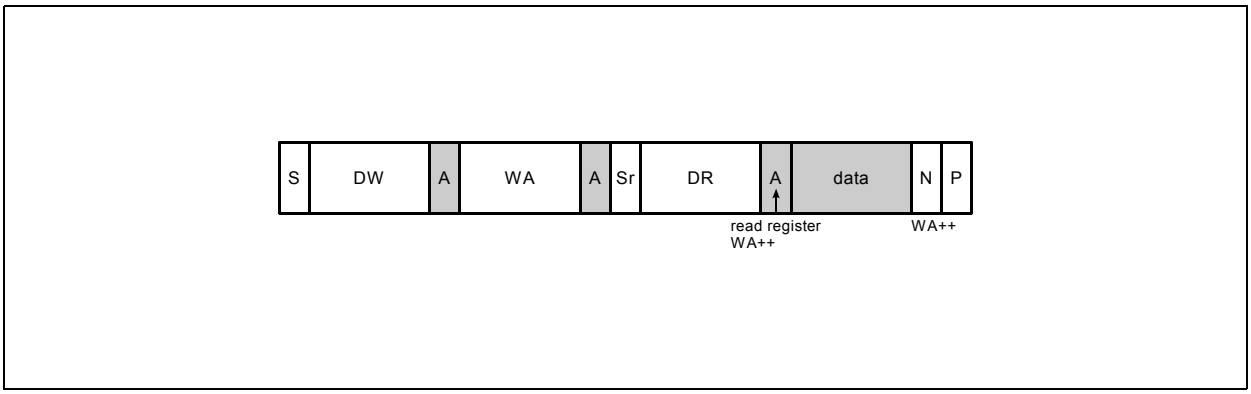
Figure 95:
I²C Sequential Read



I²C Sequential Read: Shows the format of an I²C sequential read access.

Sequential Read is the extended form of Random Read, as more than one register-data bytes are transferred subsequently. In difference to the Random Read, for a sequential read the transferred register-data bytes are responded by an acknowledge from the master. The number of data bytes transferred in one sequence is unlimited (consider the behavior of the word-address counter). To terminate the transmission the master has to send a not-acknowledge following the last data byte and generate the STOP condition subsequently.

Figure 96:
I²C Current Address Read



I²C Current Address Read: Shows the format of an I²C current address read access.

To keep the access time as small as possible, this format allows a read access without the word address transfer in advance to the data transfer. The bus is idle and the master issues a START condition followed by the Device-Read address. Analogous to Random Read, a single byte transfer is terminated with a not-acknowledge after the 1st register byte. Analogous to Sequential Read an unlimited number of data bytes can be transferred, where the data bytes has to be responded with an acknowledge from the master. For termination of the transmission the master sends a not-acknowledge following the last data byte and a subsequent STOP condition.

GPIO, SWD and Security Registers

Figure 97:
GPIO_DATA

0x00: GPIO_DATA				
Field	**Name**	**Rst**	**Type**	**Description**
12:0	gpio_d	0	R_PUSH	Read/write pin data directly. A read always returns the value at the pin. (1)

Note(s):

1. The upper 4 bits are routed to the LED pins. This way the software can output data conveniently and quickly. The AFE module has to be turned ON and the LED have to be enabled for this to work.

Figure 98:
GPIO_OE

0x04: GPIO_OE				
Field	**Name**	**Rst**	**Type**	**Description**
8:0	gpio_oe	0	R_PUSH	Output enable (1=output 0=input)

Figure 99:
GPIO_WMASK

0x08: GPIO_WMASK				
Field	**Name**	**Rst**	**Type**	**Description**
8:0	gpio_wmask	0x1ff	RW	All subsequent writes to GPIO_DATA and GPIO_OE will affect only those bits that are asserted in this mask register. This way a driver can set and clear bits with one access without affecting any other bits. This can be used for bit banging implementations of serial protocols.

Figure 100:
GPIO_INTTYPE

0x10: GPIO_INTTYPE				
Field	**Name**	**Rst**	**Type**	**Description**
8:0	gpio_inttype	0	RW	Interrupt type (0=level 1=edge sensitive). Level sensitive interrupts are asserted as long the interrupt condition is true. Edge level interrupt have to be cleared explicitly.

Figure 101:
GPIO_INTPOL

0x14: GPIO_INTPOL				
Field	**Name**	**Rst**	**Type**	**Description**
8:0	gpio_intpol	0	RW	Interrupt polarity (0=interrupt when '0' / nedgedge, 1=when '1' / posedge)

Figure 102:
GPIO_STATUS

0x20: GPIO_STATUS				
Field	**Name**	**Rst**	**Type**	**Description**
8:0	gpio_status	0	R_PUSH	Interrupt condition fulfilled (edge interrupt has to be cleared by writing a '1' here)

Figure 103:
GPIO_INTMASK

0x24: GPIO_INTMASK				
Field	**Name**	**Rst**	**Type**	**Description**
8:0	gpio_intmsk	0	RW	Interrupt mask: a '1' enables the interrupt

Figure 104:
GPIO_INTR

0x28: GPIO_INTR				
Field	**Name**	**Rst**	**Type**	**Description**
8:0	gpio_intr	0	RO	These bits are OR'ed together and generate the interrupt signal

Figure 105:
GPIO_D_SET

0x30: GPIO_D_SET				
Field	**Name**	**Rst**	**Type**	**Description**
12:0	gpio_o_set	0	PUSH	Setting one or more bit(s) of the GPIO_DATA register directly without affecting the others

Figure 106:
GPIO_OE_SET

0x34: GPIO_OE_SET				
Field	**Name**	**Rst**	**Type**	**Description**
12:0	gpio_oe_set	0	PUSH	Setting one or more bit(s) of the GPIO_OE registers directly without affecting the others

Figure 107:
GPIO_D_CLR

0x38: GPIO_D_CLR				
Field	**Name**	**Rst**	**Type**	**Description**
12:0	gpio_o_clr	0	PUSH	Clearing one or more bit(s) of the GPIO_DATA register directly without affecting the others

Figure 108:
GPIO_OE_CLR

0x3c: GPIO_OE_CLR				
Field	**Name**	**Rst**	**Type**	**Description**
12:0	gpio_oe_clr	0	PUSH	Clearing one or more bit(s) of the GPIO_OE registers directly without affecting the others

Figure 109:
CCU_IOFUNC0

0x50: CCU_IOFUNC0				
Field	**Name**	**Rst**	**Type**	**Description**
2:0	gpio0_func	0	RW	Please refer to Figure 110
4:3	gpio0_pd	0	RW	Please refer to Figure 111
5	gpio0_sr	0	RW	Slew rate: 0=fast 1=slow
10:8	gpio1_func	0	RW	Please refer to Figure 110
12:11	gpio1_pd	0	RW	Please refer to Figure 111
13	gpio1_sr	0	RW	Slew rate: 0=fast 1=slow
18:16	gpio2_func	0	RW	Please refer to Figure 110
20:19	gpio2_pd	0	RW	Please refer to Figure 111
21	gpio2_sr	0	RW	Slew rate: 0=fast 1=slow
26:24	gpio3_func	0	RW	Please refer to Figure 110
28:27	gpio3_pd	0	RW	Please refer to Figure 111
29	gpio3_sr	0	RW	Slew rate: 0=fast 1=slow

The CCU_IOFUNC0/1/2 gpioX_func register defines the multiplexing mode of each pin.

Figure 110:
gpioX_func Codings (X=0…8)

gpioX_func	Description
0	GPIO
3	I^2C Master
4	I^2C Slave
5	UART
7	Analog

The CCU_IOFUNC0/1/2 gpioX_pd fields define the pullup/pulldown configuration

Figure 111:
gpioX_pd Codings (X=0…8)

gpioX_pd	Description
0	None
1	Weak Pull Up
2	Weak Pull Down
3	Keeper

Figure 112:
CCU_IOFUNC1

0x54: CCU_IOFUNC1				
Field	**Name**	**Rst**	**Type**	**Description**
2:0	gpio4_func	0	RW	Please refer to Figure 110
4:3	gpio4_pd	0	RW	Please refer to Figure 111
5	gpio4_sr	0	RW	Slew rate: 0=fast 1=slow
10:8	gpio5_func	0	RW	Please refer to Figure 110
12:11	gpio5_pd	0	RW	Please refer to Figure 111
13	gpio5_sr	0	RW	Slew rate: 0=fast 1=slow
18:16	gpio6_func	0	RW	Please refer to Figure 110
20:19	gpio6_pd	0	RW	Please refer to Figure 111
21	gpio6_sr	0	RW	Slew rate: 0=fast 1=slow
26:24	gpio7_func	0	RW	Please refer to Figure 110
28:27	gpio7_pd	0	RW	Please refer to Figure 111
29	gpio7_sr	0	RW	Slew rate: 0=fast 1=slow

Figure 113:
CCU_IOFUNC2

0x58: CCU_IOFUNC2				
Field	**Name**	**Rst**	**Type**	**Description**
2:0	gpio8_func	0	RW	Please refer to Figure 110
4:3	gpio8_pd	0	RW	Please refer to Figure 111
5	gpio8_sr	0	RW	Slew rate: 0=fast 1=slow

Figure 114:
CCU_RETENTION

0xfc: CCU_RETENTION				
Field	Name	Rst	Type	Description
30	enable_swd	1	RW	Enable SWD interface on GPIO7/8 (overrides any gpio7_ func/gpio8_func setting).
31	securitybit	0	WS_SC	securitybit, to disable access through the SWD interface in the final product. The bit can only be written to 1, not reset. If enabled by the factory or in EEPROM, the bootloader sets this bit before booting the user software. Therefore the image inside the EEPROM is protected against external access.

The CCU_RETENTION register is the only register that is not affected by powerdown, Only a power cycle will reset these bits.

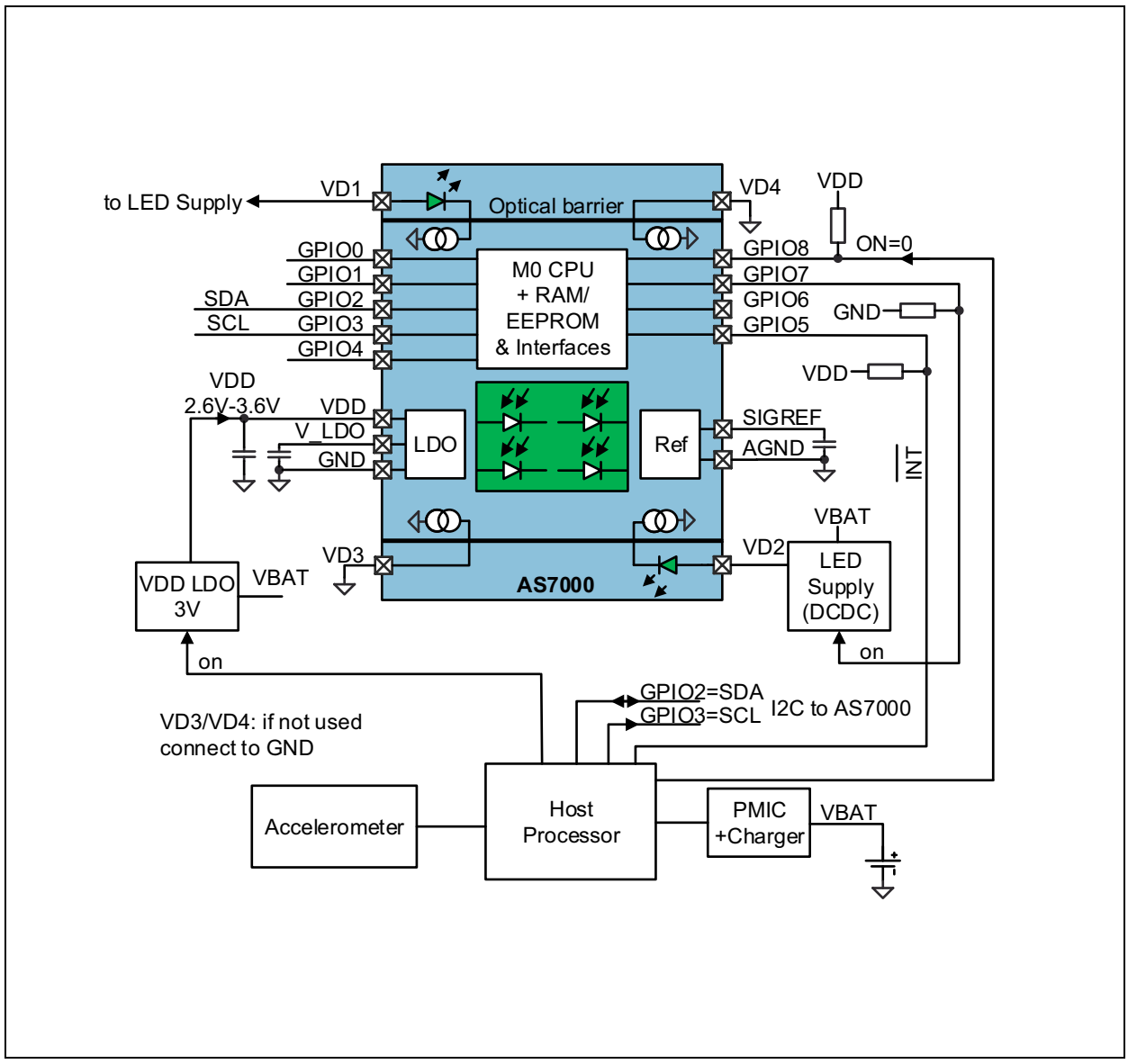
Application Information

The AS7000 has a built-in I²C master and host device. Therefore it allows to connect an accelerometer used for motion artefact compensation in two ways:

1. Connected through the host and data provided by the host to the AS7000 via the AS7000 I²C slave
2. Connected directly to the AS7000 and the AS7000 I²C master retrieves the data from the accelerometer.

Following two figures show the different configurations.

Figure 115:
Measurement System With Motion Artefact Compensation

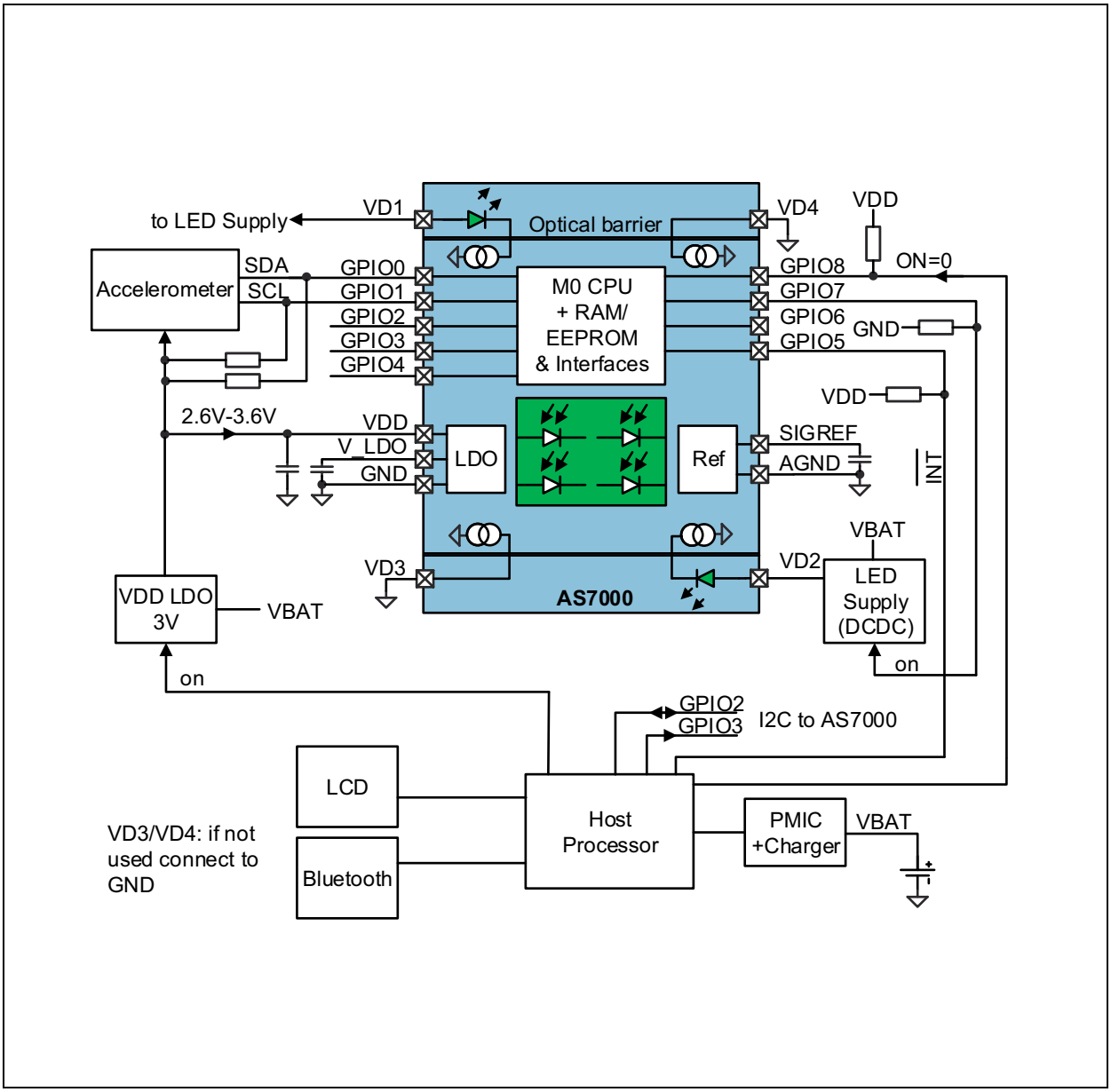


Note(s):

1. Accelerometer data provided by host.

In above configuration the host needs to send the accelerometer data to the AS7000 via the I²C interface.

Figure 116:
Measurement System With Motion Artefact Compensation Using AS7000 Dedicated Accelerometer



Note(s):

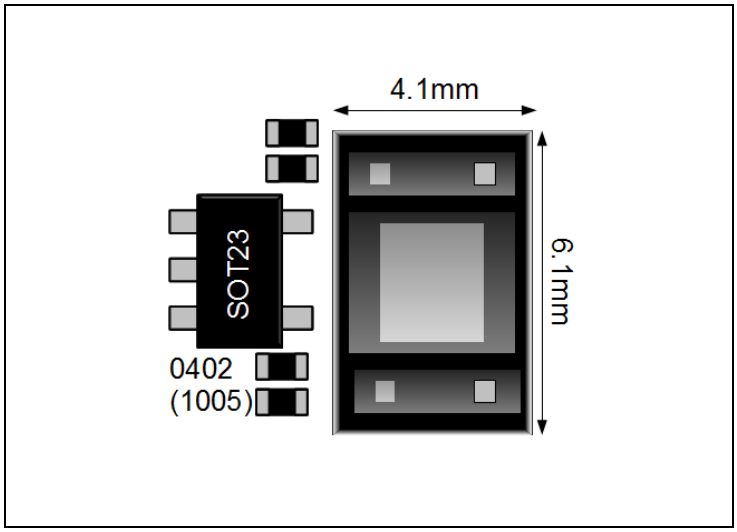
1. Accelerometer connected directly

In above configuration, the AS7000 I^2C master is used to poll the data from the accelerometer.

The AS7000 has internal protection diodes on all GPIO pins connected to VDD. If VDD is switched off, all GPIO pins are clamped to this VDD supply plus one diode voltage (typically 0.6V). Therefore connect the periphery supply of these pins (example: I^2C pins from host in above example connected to GPIO2/3), which are connected to the AS7000 GPIO pins to the same VDD supply as the AS7000. If this is not possible, ensure that these pins are at logic 0 if the VDD supply of AS7000 is switched off.

Due to the integration of the optical diode / optical frontend / analog processing / ADC and microprocessor a heart-rate measurement application can be built with very small PCB area as shown in following figure:

Figure 117:
Typical Form Factor Including VDD LDO



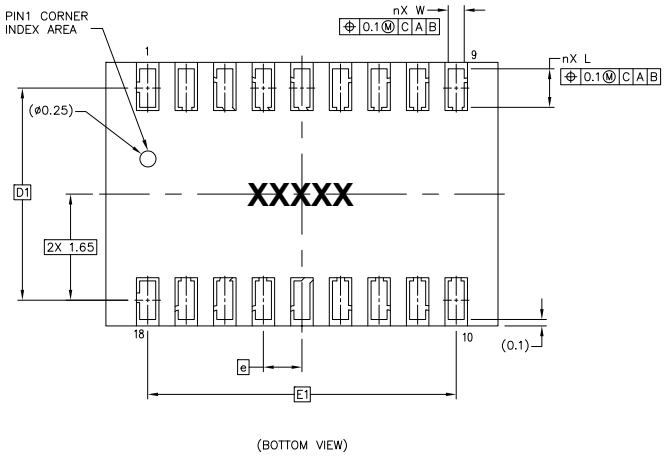
External Components

Figure 118:
External Components

Part Number	Parameter or Type	Voltage Rating	Size	Comment	Manufacturer
AS1383	DC-DC converter 200mA, 3.5MHz	n/a	1.17x0.77x0.6mm	DC-DC converter for VLED supply on pin VD1/VD2	**ams** www.ams.com
AS1369-BWLT-30	200mA LDO	VOUT=3.0V	0.97x0.97x0.6mm	Ultra Small LDO for VDD supply	
GRM153R60J225ME95	C=2.2µF, min. 1µF at 1.0V bias	6.3V	0402 (1.0x0.5x0.5mm)	On pin VDD, V_LDO and SIGREF	Murata www.murata.com
LIS2DH12	Accelerometer	n/a	2x2x1mm		ST www.st.com

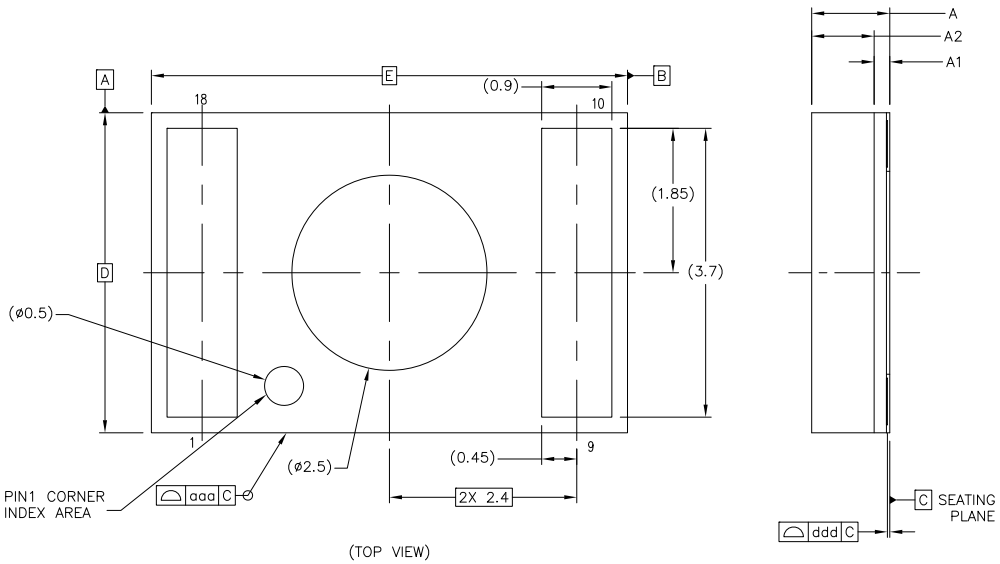
Package Drawings & Markings

Figure 119:
Package Drawings



(BOTTOM VIEW)

	SYMBOL	COMMON DIMENSIONS		
		MIN.	NOR.	MAX.
TOTAL THICKNESS	A	0.9	1	1.1
SUBSTRATE THICKNESS	A1	0.16	0.2	0.24
LID THICKNESS	A2	0.73	0.76	0.79
BODY SIZE	D	4	4.1	4.2
	E	6	6.1	6.2
LEAD WIDTH	W	0.2	0.25	0.3
LEAD LENGTH	L	0.55	0.6	0.65
LEAD PITCH	e		0.6	BSC
LEAD COUNT	n		18	
EDGE BALL CENTER TO CENTER	D1		3.3	BSC
	E1		4.8	BSC
BODY CENTER TO CONTACT BALL	SD		---	BSC
	SE		---	BSC
BALL WIDTH	b	---	---	---
BALL DIAMETER			---	
BALL OPENING			---	
BALL PICTH	e1		---	
BALL COUNT	n1		---	
PRE-SOLDER		---	---	---
PACKAGE EDGE TOLERANCE	aaa		0.1	
MOLD FLATNESS	bbb		---	
COPLANARITY	ddd		0.08	
BALL OFFSET (PACKAGE)	eee		---	
BALL OFFSET (BALL)	fff		---	



(TOP VIEW)

Note(s):

1. **XXXXX** - Tracecode backside marking (upside down)

Ordering & Contact Information

Figure 120:
Ordering Information

Ordering Code	Type	LED Configuration	Marking	Delivery Form	Delivery Quantity
AS7000-AA	AS7000	Green/Green	XXXXX(1)	Tape & Reel	5000 pcs/reel
AS7000-AAM	AS7000	Green/Green	XXXXX(1)	Tape & Reel	500 pcs/reel

Note(s):

1. **XXXXX** - Tracecode backside marking

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Document Status

Document Status	Product Status	Definition
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Preliminary Datasheet	Pre-Production	Information in this datasheet is based on products in the design, validation or qualification phase of development. The performance and parameters shown in this document are preliminary without any warranty and are subject to change without notice
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Datasheet (discontinued)	Discontinued	Information in this datasheet is based on products which conform to specifications in accordance with the terms of ams AG standard warranty as given in the General Terms of Trade, but these products have been superseded and should not be used for new designs

Revision Information

Changes from 1-10 (2017-Feb-28) to current revision 1-12 (2018-Feb-26)	Page
1-10 (2017-Feb-28) to 1-11 (2017-Sep-28)	
Added note under Absolute Maximum Ratings figure	5
1-11 (2017-Sep-28) to 1-12 (2018-Feb-26)	
Removed AS7000AB related content	

Note(s):

1. Page and figure numbers for the previous version may differ from page and figure numbers in the current revision.
2. Correction of typographical errors is not explicitly mentioned.

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