Octal D-type transparent latch (3-State) 74LV373

FEATURES

- Wide operating voltage: 1.0 to 5.5V
- Optimized for Low Voltage applications: 1.0V to 3.6V
- Accepts TTL input levels between V_{CC} = 2.7V and V_{CC} = 3.6V
- Typical V_{OLP} (output ground bounce) < 0.8V at V_{CC} = 3.3V, T_{amb} = 25°C
- Typical V_{OHV} (output V_{OH} undershoot) > 2V at V_{CC} = 3.3V, T_{amb} = 25°C
- Common 3-State output enable input
- Output capability: bus driver
- I_{CC} category: MSI

DESCRIPTION

The 74LV373 is a low-voltage Si-gate CMOS device that is pin and function compatible with 74HC/HCT373.

The 74LV373 is an octal D-type transparent latch featuring separate D-type inputs for each latch and 3-State outputs for bus oriented applications. A latch enable (LE) input and an output enable ($\overline{OE}$) input are common to all internal latches.

The '373' consists of eight D-type transparent latches with 3-State true outputs. When LE is HIGH, data at the Dn inputs enters the latches. In this condition the latches are transparent, i.e., a latch output will change each time its corresponding D-input changes.

When LE is LOW the latches store the information that was present at the D-inputs a set-up time preceding the HIGH-to-LOW transition of LE. When $\overline{OE}$ is LOW, the contents of the eight latches are available at the outputs. When $\overline{OE}$ is HIGH, the outputs go to the high impedance OFF-state. Operation of the $\overline{OE}$ input does not affect the state of the latches.

The '373' is functionally identical to the '573', but the '573' has a different pin arrangement.

QUICK REFERENCE DATA

GND = 0V; T_{amb} = 25°C; $t_r = t_f \leq 2.5$ ns

SYMBOL	PARAMETER	CONDITIONS	TYPICAL	UNIT
t_{PHL}/t_{PLH}	Propagation delay D_n to Q_n LE to Q_n	C_L = 15pF V_{CC} = 3.3V	 10 12	ns
C_I	Input capacitance		3.5	pF
C_{PD}	Power dissipation capacitance per latch	Notes 1, 2	22	pF

NOTES:

1. C_{PD} is used to determine the dynamic power dissipation (P_D in μW)
   $P_D = C_{PD} \times V_{CC}^2 \times f_i + \sum (C_L \times V_{CC}^2 \times f_o)$ where:
   f_i = input frequency in MHz; C_L = output load capacity in pF;
   f_o = output frequency in MHz; V_{CC} = supply voltage in V;
   $\sum (C_L \times V_{CC}^2 \times f_o)$ = sum of the outputs.
2. The condition is V_I = GND to V_{CC}.

ORDERING AND PACKAGE INFORMATION

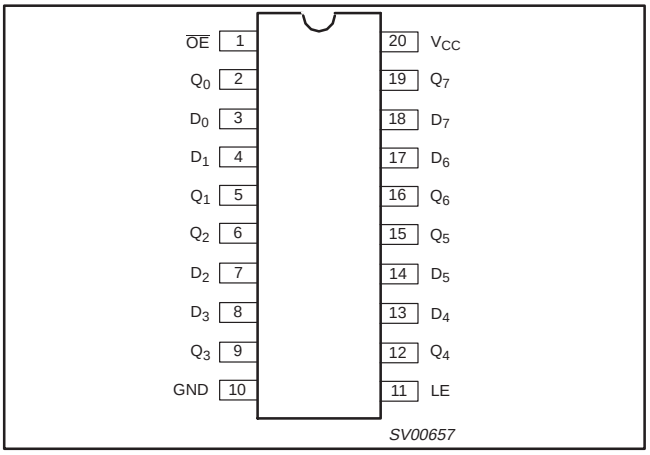
PACKAGES	TEMPERATURE RANGE	OUTSIDE NORTH AMERICA	NORTH AMERICA	PKG. DWG. #
20-Pin Plastic DIL	–40°C to +125°C	74LV373 N	74LV373 N	SOT146-1
20-Pin Plastic SO	–40°C to +125°C	74LV373 D	74LV373 D	SOT163-1
20-Pin Plastic SSOP Type II	–40°C to +125°C	74LV373 DB	74LV373 DB	SOT339-1
20-Pin Plastic TSSOP Type I	–40°C to +125°C	74LV373 PW	74LV373PW DH	SOT360-1

PIN DESCRIPTION

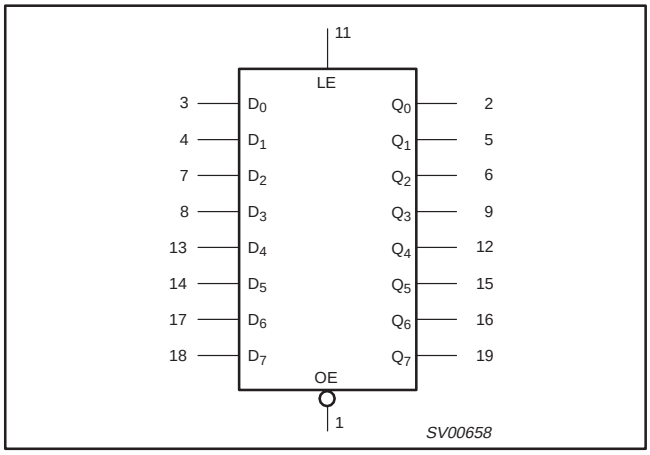
PIN NUMBER	SYMBOL	FUNCTION
1	$\overline{OE}$	Output enabled input (active LOW)
2, 5, 6, 9, 12, 15, 16, 19	Q_0–Q_7	3-State latch outputs
3, 4, 7, 8, 13, 14, 17, 18	D_0–D_7	Data inputs
10	GND	Ground (0V)
11	LE	Latch enable input (active HIGH)
20	V_{CC}	Positive supply voltage

Octal D-type transparent latch (3-State) 74LV373

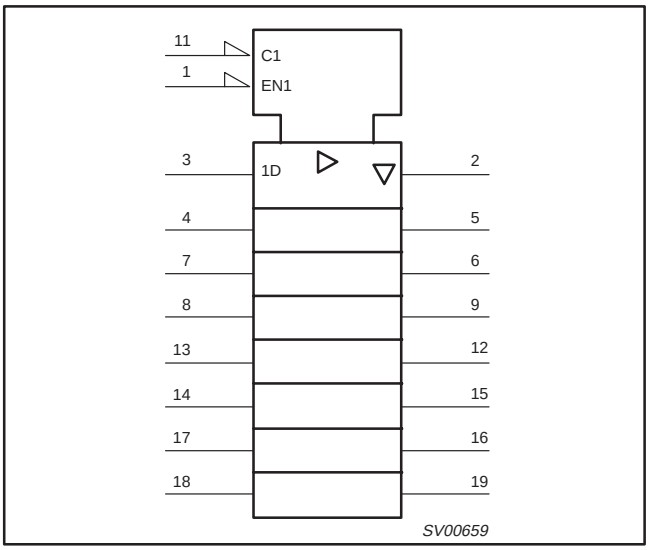
PIN CONFIGURATION



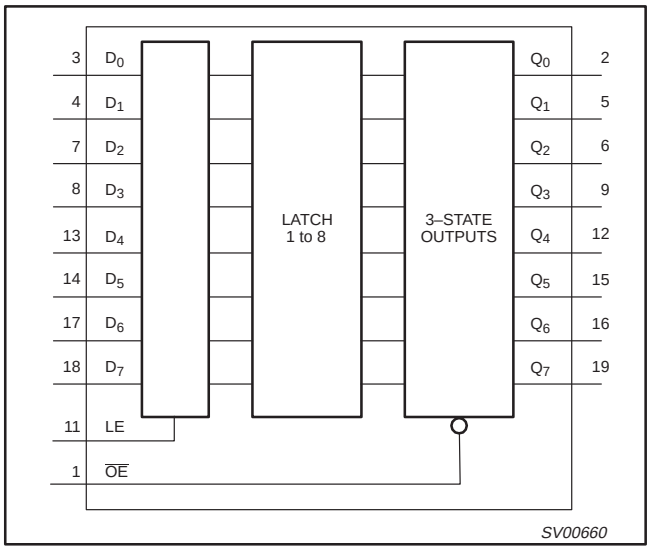
LOGIC SYMBOL



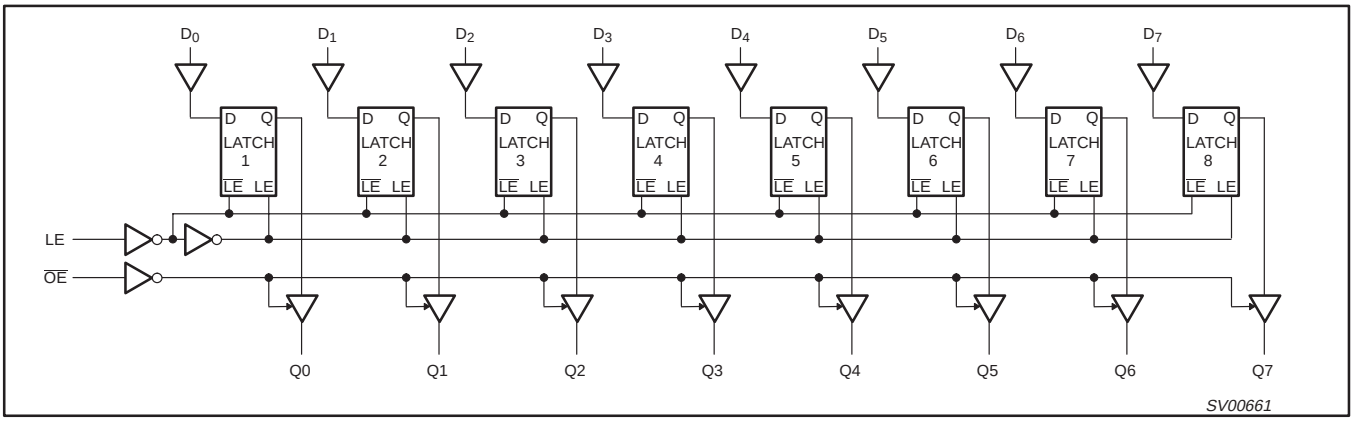
LOGIC SYMBOL (IEEE/IEC)



FUNCTIONAL DIAGRAM



LOGIC DIAGRAM



FUNCTION TABLE

OPERATING MODES	INPUTS			INTERNAL LATCHES	OUTPUTS
	$\overline{OE}$	LE	Dn		Q_0 to Q_7
Enable and read register (transparent mode)	L L	H H	L H	L H	L H
Latch and read register	L L	L L	l h	L H	L H
Latch register and disable outputs	H H	L L	l h	L H	Z Z

H = HIGH voltage level
h = HIGH voltage level one set-up time prior to the HIGH-to-LOW LE transition
L = LOW voltage level
l = LOW voltage level one set-up time prior to the HIGH-to-LOW LE transition
X = Don't care
Z = High impedance OFF-state

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP.	MAX	UNIT
V_{CC}	DC supply voltage	See Note1	1.0	3.3	5.5	V
V_I	Input voltage		0	–	V_{CC}	V
V_O	Output voltage		0	–	V_{CC}	V
T_{amb}	Operating ambient temperature range in free air	See DC and AC characteristics	–40 –40		+85 +125	°C
t_r, t_f	Input rise and fall times	V_{CC} = 1.0V to 2.0V V_{CC} = 2.0V to 2.7V V_{CC} = 2.7V to 3.6V V_{CC} = 3.6V to 5.5V	– – – –	– – – –	500 200 100 50	ns/V

NOTE:
1. The LV is guaranteed to function down to V_{CC} = 1.0V (input levels GND or V_{CC}); DC characteristics are guaranteed from V_{CC} = 1.2V to V_{CC} = 5.5V.

ABSOLUTE MAXIMUM RATINGS[1, 2]

In accordance with the Absolute Maximum Rating System (IEC 134).
Voltages are referenced to GND (ground = 0V).

SYMBOL	PARAMETER	CONDITIONS	RATING	UNIT
V_{CC}	DC supply voltage		–0.5 to +7.0	V
$\pm I_{IK}$	DC input diode current	$V_I < –0.5$ or $V_I > V_{CC} + 0.5V$	20	mA
$\pm I_{OK}$	DC output diode current	$V_O < –0.5$ or $V_O > V_{CC} + 0.5V$	50	mA
$\pm I_O$	DC output source or sink current – bus driver outputs	$–0.5V < V_O < V_{CC} + 0.5V$	35	mA
$\pm I_{GND}$, $\pm I_{CC}$	DC V_{CC} or GND current for types with –bus driver outputs		70	mA
T_{stg}	Storage temperature range		–65 to +150	°C
P_{tot}	Power dissipation per package –plastic DIL –plastic mini-pack (SO) –plastic shrink mini-pack (SSOP and TSSOP)	for temperature range: –40 to +125°C above +70°C derate linearly with 12mW/K above +70°C derate linearly with 8 mW/K above +60°C derate linearly with 5.5 mW/K	 750 500 400	mW

NOTES:
1. Stresses beyond those listed may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
2. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

DC CHARACTERISTICS

Over recommended operating conditions. Voltages are referenced to GND (ground = 0V).

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS					UNIT
			-40°C to +85°C			-40°C to +125°C		
			MIN	TYP[1]	MAX	MIN	MAX	
V_{IH}	HIGH level Input voltage	V_{CC} = 1.2V	0.9			0.9		V
		V_{CC} = 2.0V	1.4			1.4		
		V_{CC} = 2.7 to 3.6V	2.0			2.0		
		V_{CC} = 4.5 to 5.5V	0.7*V_{CC}			0.7*V_{CC}		
V_{IL}	LOW level Input voltage	V_{CC} = 1.2V			0.3		0.3	V
		V_{CC} = 2.0V			0.6		0.6	
		V_{CC} = 2.7 to 3.6V			0.8		0.8	
		V_{CC} = 4.5 to 5.5			0.3*V_{CC}		0.3*V_{CC}	
V_{OH}	HIGH level output voltage; all outputs	V_{CC} = 1.2V; V_I = V_{IH} or V_{IL}; $-I_O$ = 100µA		1.2				V
		V_{CC} = 2.0V; V_I = V_{IH} or V_{IL}; $-I_O$ = 100µA	1.8	2.0		1.8		
		V_{CC} = 2.7V; V_I = V_{IH} or V_{IL}; $-I_O$ = 100µA	2.5	2.7		2.5		
		V_{CC} = 3.0V; V_I = V_{IH} or V_{IL}; $-I_O$ = 100µA	2.8	3.0		2.8		
		V_{CC} = 4.5V; V_I = V_{IH} or V_{IL}; $-I_O$ = 100µA	4.3	4.5		4.3		
	HIGH level output voltage; BUS driver outputs	V_{CC} = 3.0V; V_I = V_{IH} or V_{IL}; $-I_O$ = 8mA	2.40	2.82		2.20		
		V_{CC} = 4.5V; V_I = V_{IH} or V_{IL}; $-I_O$ = 16mA	3.60	4.20		3.50		
V_{OL}	LOW level output voltage; all outputs	V_{CC} = 1.2V; V_I = V_{IH} or V_{IL}; I_O = 100µA		0				V
		V_{CC} = 2.0V; V_I = V_{IH} or V_{IL}; I_O = 100µA		0	0.2		0.2	
		V_{CC} = 2.7V; V_I = V_{IH} or V_{IL}; I_O = 100µA		0	0.2		0.2	
		V_{CC} = 3.0V; V_I = V_{IH} or V_{IL}; I_O = 100µA		0	0.2		0.2	
		V_{CC} = 4.5V; V_I = V_{IH} or V_{IL}; I_O = 100µA		0	0.2		0.2	
	LOW level output voltage; BUS driver outputs	V_{CC} = 3.0V; V_I = V_{IH} or V_{IL}; I_O = 8mA		0.20	0.40		0.50	
		V_{CC} = 4.5V; V_I = V_{IH} or V_{IL}; I_O = 16mA		0.35	0.55		0.65	
I_I	Input leakage current	V_{CC} = 5.5V; V_I = V_{CC} or GND			1.0		1.0	µA
I_{OZ}	3-State output OFF-state current	V_{CC} = 5.5V; V_I = V_{IH} or V_{IL}; V_O = V_{CC} or GND			5		10	µA
I_{CC}	Quiescent supply current; MSI	V_{CC} = 5.5V; V_I = V_{CC} or GND; I_O = 0			20.0		160	µA
ΔI_{CC}	Additional quiescent supply current per input	V_{CC} = 2.7V to 3.6V; V_I = V_{CC} – 0.6V			500		850	µA

NOTE:

1. All typical values are measured at T_{amb} = 25°C.

AC CHARACTERISTICS

GND = 0V; $t_r = t_f \leq 2.5$ns; $C_L = 50$pF; $R_L = 1$KΩ

SYMBOL	PARAMETER	WAVEFORM	CONDITION	LIMITS					UNIT
				–40 to +85 °C			–40 to +125 °C		
			V_{CC}(V)	MIN	TYP[1]	MAX	MIN	MAX	
t_{PHL}/t_{PLH}	Propagation delay D_n to Q_n	Figure 1, 5	1.2	–	65	–	–	–	ns
			2.0	–	22	37	–	48	
			2.7	–	16	28	–	35	
			3.0 to 3.6	–	13[2]	22	–	28	
			4.5 to 5.5	–	–	16	–	20	
t_{PHL}/t_{PLH}	Propagation delay LE to Q_n	Figure 2, 5	1.2	–	80	–	–	–	ns
			2.0	–	27	43	–	54	
			2.7	–	20	26	–	33	
			3.0 to 3.6	–	15[2]	25	–	31	
			4.5 to 5.5	–	9.5[3]	19	–	24	
t_{PZH}/t_{PZL}	3-State output enable time $\overline{OE}$ to Q_n	Figure 3	1.2	–	80	–	–	–	ns
			2.0	–	27	46	–	58	
			2.7	–	20	28	–	35	
			3.0 to 3.6	–	15[2]	27	–	34	
			4.5 to 5.5	–	–	23	–	29	
t_{PHZ}/t_{PLZ}	3-State output disable time $\overline{OE}$ to Q_n	Figure 3	1.2	–	75	–	–	–	ns
			2.0	–	27	46	–	58	
			2.7	–	21	28	–	35	
			3.0 to 3.6	–	16[2]	27	–	34	
			4.5 to 5.5	–	–	23	–	29	
t_W	LE pulse width HIGH	Figure 2	2.0	34	10	–	41	–	ns
			2.7	25	8	–	30	–	
			3.0 to 3.6	20	6[2]	–	24	–	
t_{su}	Setup time D_n to LE	Figure 4	1.2	–	25	–	–	–	ns
			2.0	17	9	–	20	–	
			2.7	13	6	–	15	–	
			3.0 to 3.6	10	5[2]	–	12	–	
t_h	Hold time D_n to LE	Figure 4	1.2	–	–15	–	–	–	ns
			2.0	5	–5	–	5	–	
			2.7	5	–3	–	5	–	
			3.0 to 3.6	5	–3[2]	–	5	–	

NOTES:
1. All typical values are measured at $T_{amb} = 25°C$
2. Typical values are measured at $V_{CC} = 3.3$V
3. Typical values are measured at $V_{CC} = 5.0$V

AC WAVEFORMS

V_M = 1.5V at $V_{CC} \geq$ 2.7V and $\leq$ 3.6V
V_M = 0.5 * V_{CC} at V_{CC} < 2.7V and $\geq$ 4.5V
V_{OL} and V_{OH} are the typical output voltage drop that occur with the output load.
$V_X = V_{OL} + 0.3V$ at $V_{CC} \geq$ 2.7V and $\leq$ 3.6V
$V_X = V_{OL} + 0.1V_{CC}$ at V_{CC} < 2.7V and $\geq$ 4.5V
$V_Y = V_{OH} - 0.3V$ at $V_{CC} \geq$ 2.7V and $\leq$ 3.6V
$V_Y = V_{OH} - 0.1V_{CC}$ at V_{CC} < 2.7V and $\geq$ 4.5V

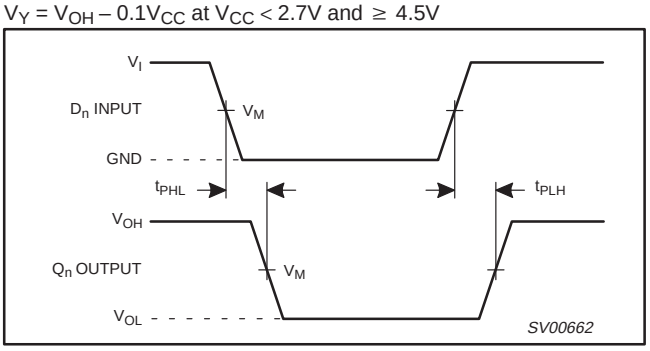


Figure 1. Data input (D_n) to output (Q_n) propagation delays and the output transition times.

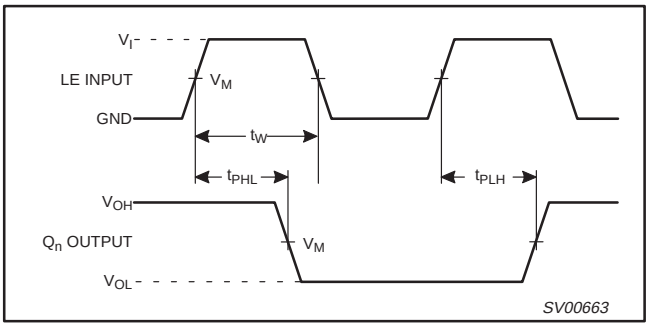


Figure 2. Latch enable input (LE) pulse width, the latch enable input to output (Q_n) propagation delays and the output transition times.

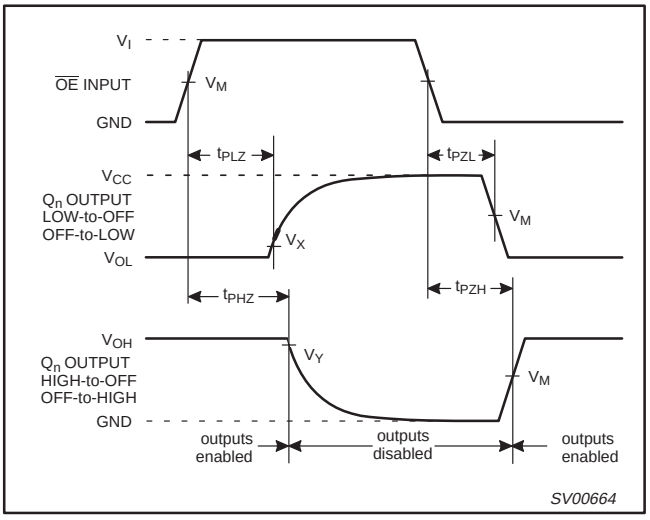


Figure 3. 3-State enable and disable times.

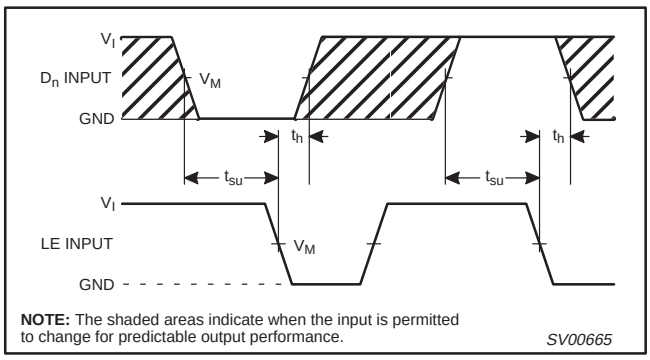
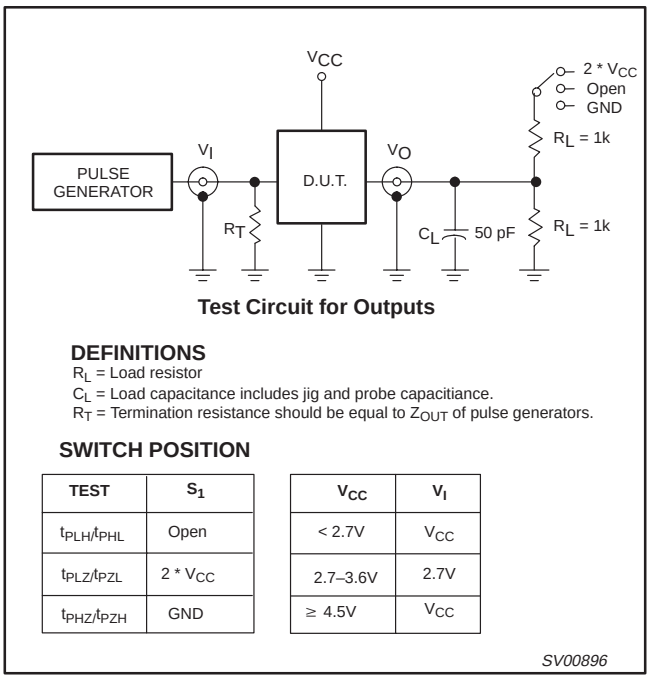


Figure 4. Data set-up and hold times for the D_n input to the LE input.

TEST CIRCUIT



Test Circuit for Outputs

DEFINITIONS
R_L = Load resistor
C_L = Load capacitance includes jig and probe capacitance.
R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.

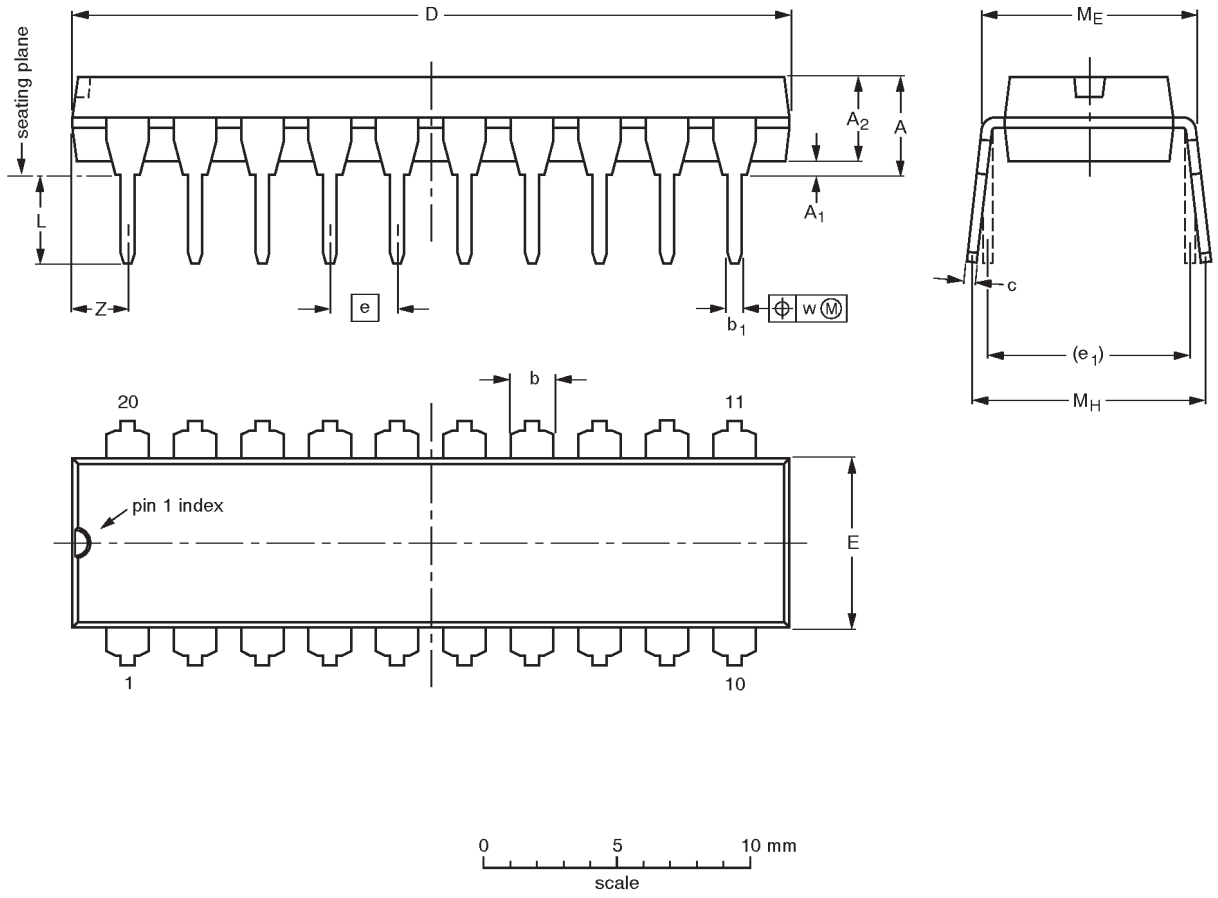
SWITCH POSITION

TEST	S_1
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	2 * V_{CC}
t_{PHZ}/t_{PZH}	GND

V_{CC}	V_I
< 2.7V	V_{CC}
2.7–3.6V	2.7V
$\geq$ 4.5V	V_{CC}

Figure 5. Load circuitry for switching times

DIP20: plastic dual in-line package; 20 leads (300 mil) **SOT146-1**



DIMENSIONS (inch dimensions are derived from the original mm dimensions)

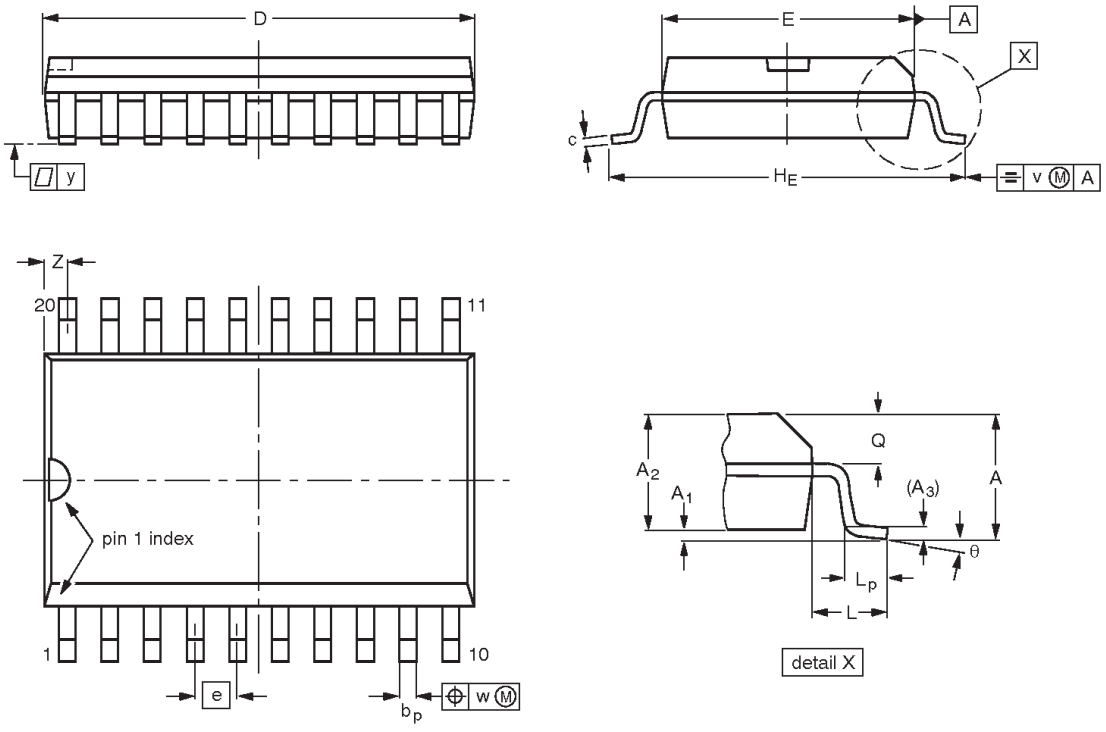
UNIT	A max.	A_1 min.	A_2 max.	b	b_1	c	D (1)	E (1)	e	e_1	L	M_E	M_H	w	Z (1) max.
mm	4.2	0.51	3.2	1.73 1.30	0.53 0.38	0.36 0.23	26.92 26.54	6.40 6.22	2.54	7.62	3.60 3.05	8.25 7.80	10.0 8.3	0.254	2.0
inches	0.17	0.020	0.13	0.068 0.051	0.021 0.015	0.014 0.009	1.060 1.045	0.25 0.24	0.10	0.30	0.14 0.12	0.32 0.31	0.39 0.33	0.01	0.078

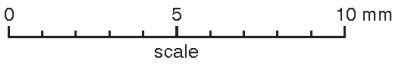
Note

1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT146-1			SC603			~~92-11-17~~ 95-05-24

SO20: plastic small outline package; 20 leads; body width 7.5 mm **SOT163-1**





DIMENSIONS (inch dimensions are derived from the original mm dimensions)

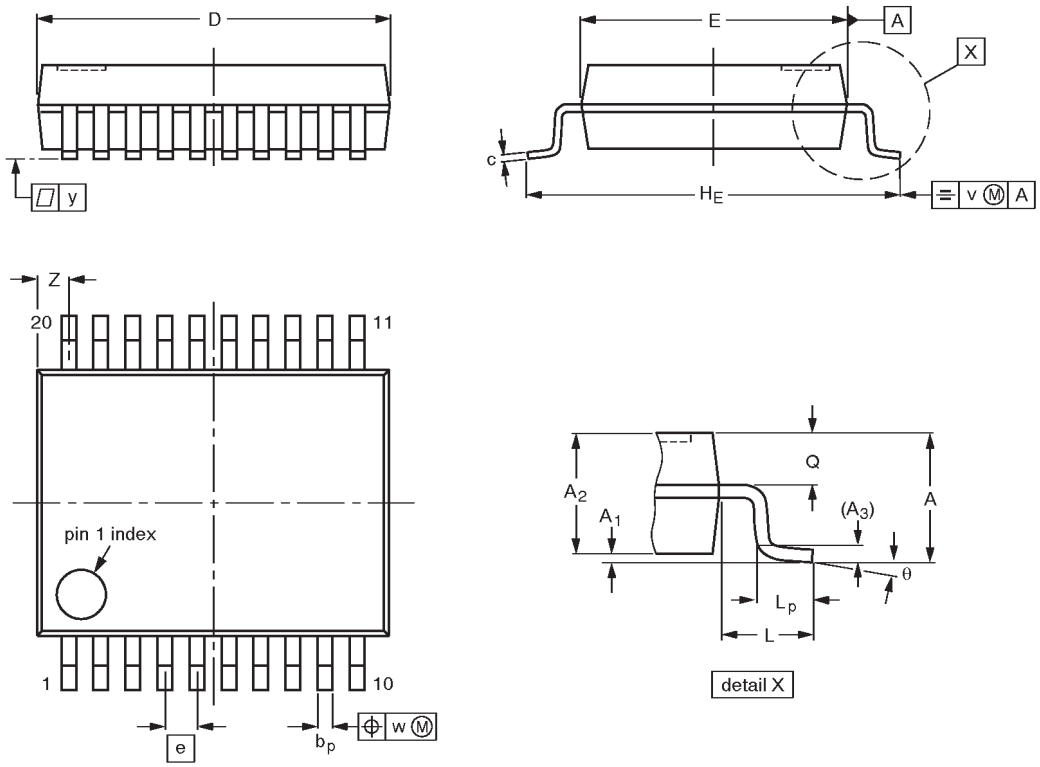
UNIT	A max.	A_1	A_2	A_3	b_p	c	D (1)	E (1)	e	H_E	L	L_p	Q	v	w	y	Z (1)	θ
mm	2.65	0.30 0.10	2.45 2.25	0.25	0.49 0.36	0.32 0.23	13.0 12.6	7.6 7.4	1.27	10.65 10.00	1.4	1.1 0.4	1.1 1.0	0.25	0.25	0.1	0.9 0.4	8^o 0^o
inches	0.10	0.012 0.004	0.096 0.089	0.01	0.019 0.014	0.013 0.009	0.51 0.49	0.30 0.29	0.050	0.42 0.39	0.055	0.043 0.016	0.043 0.039	0.01	0.01	0.004	0.035 0.016	

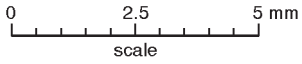
Note

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT163-1	075E04	MS-013AC				~~92-11-17~~ 95-01-24

SSOP20: plastic shrink small outline package; 20 leads; body width 5.3 mm **SOT339-1**





DIMENSIONS (mm are the original dimensions)

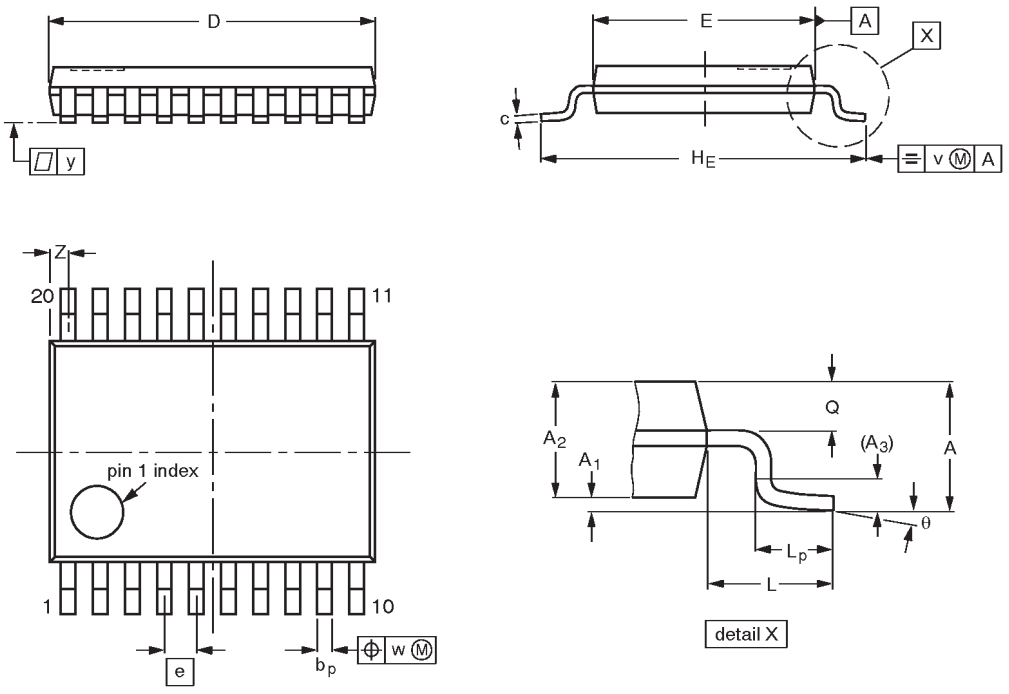
UNIT	A max.	A_1	A_2	A_3	b_p	c	$D^{(1)}$	$E^{(1)}$	e	H_E	L	L_p	Q	v	w	y	$Z^{(1)}$	θ
mm	2.0	0.21 0.05	1.80 1.65	0.25	0.38 0.25	0.20 0.09	7.4 7.0	5.4 5.2	0.65	7.9 7.6	1.25	1.03 0.63	0.9 0.7	0.2	0.13	0.1	0.9 0.5	8° 0°

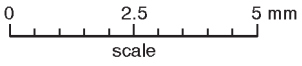
Note

1. Plastic or metal protrusions of 0.20 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT339-1		MO-150AE				~~93-09-08~~ 95-02-04

TSSOP20: plastic thin shrink small outline package; 20 leads; body width 4.4 mm **SOT360-1**





DIMENSIONS (mm are the original dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	D (1)	E (2)	e	H_E	L	L_p	Q	v	w	y	Z (1)	θ
mm	1.10	0.15 0.05	0.95 0.80	0.25	0.30 0.19	0.2 0.1	6.6 6.4	4.5 4.3	0.65	6.6 6.2	1.0	0.75 0.50	0.4 0.3	0.2	0.13	0.1	0.5 0.2	8° 0°

Notes

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.
2. Plastic interlead protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT360-1		MO-153AC				~~93-06-16~~ 95-02-04

DEFINITIONS

Data Sheet Identification	Product Status	Definition
Objective Specification	Formative or in Design	This data sheet contains the design target or goal specifications for product development. Specifications may change in any manner without notice.
Preliminary Specification	Preproduction Product	This data sheet contains preliminary data, and supplementary data will be published at a later date. Philips Semiconductors reserves the right to make changes at any time without notice in order to improve design and supply the best possible product.
Product Specification	Full Production	This data sheet contains Final Specifications. Philips Semiconductors reserves the right to make changes at any time without notice, in order to improve design and supply the best possible product.

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