Absolute Maximum Ratings

OUT1, OUT2, FB1, FB2, FB3, $\overline{POR}$, PG2, PG3, PGA, $\overline{OT}$ to GND ..... -0.3V to +6V
$\overline{UVO}$, EN2, EN3, ENA, OUTA, SYNC, V_L to GND ..... -0.3V to +6V
UVI, UVS to GND ..... -0.3V to +20V
UVI, UVS Input Current ..... ±10mA
OUT3 to GND ..... -0.3V to +10V
V_{INA}, V_{INB}, ODRV, LX1, LX2, LX3 to GND (500ms) ..... -0.3V to +45V
V_{INA} to V_{INB} ..... -2V to +18V
BST1, BST2, BST3 to PGND_ (500ms) ..... -0.3V to +50V
Continuous Power Dissipation (T_A = +70°C)
TQFN (derate 37mW/°C above +70°C) 2963mW
Operating Temperature Range ..... -40°C to +125°C
Junction Temperature ..... +150°C
Storage Temperature Range ..... -65°C to +150°C
Lead Temperature (soldering, 10s) ..... +300°C
Soldering Temperature (reflow) ..... +260°C

Package Thermal Characteristics (Note 1)

TQFN
Junction-to-Ambient Thermal Resistance (θ_{JA}) ..... 27°C/W
Junction-to-Case Thermal Resistance (θ_{JC}) ..... 1°C/W

Note 1: Package thermal resistances were obtained using the method described in JEDEC specification JESD51-7, using a four-layer board. For detailed information on package thermal considerations, refer to **www.maximintegrated.com/thermal-tutorial**.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Electrical Characteristics

(V_{INA} = V_{INB} = 14V, T_A = -40°C to +125°C, unless otherwise noted. Typical values are at T_A = +25°C.) (Note 2)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
V_{INA}/V_{INB} Operating Supply Range	V_{IN}	Full performance	5.5		18	V
		DC-DC1 maintains regulation, I_{OUT1} = 100mA (Note 2)	4		28	
V_{INA}/V_{INB} Supply Current in Operation	I_{IN}	EN2 = EN3 = ENA = high, no switching		2	3	mA
V_{INA}/V_{INB} Supply Current, Standby Mode	I_{ST}	Only DC-DC1 operating, EN2 = EN3 = ENA = low, I_{OUT1} = no load		25	50	µA
V_L Undervoltage Lockout	V_{UVL}	V_L rising	2.9	3.15	3.4	V
V_L Undervoltage Lockout Hysteresis	V_{UVH}			0.4		V
V_L Output Voltage	V_L			5		V
UVI Threshold	UVL	V_{INA}/V_{INB} falling	1.181 (-2%)	1.205	1.229 (+2%)	V
UVI Input Current	I_{UVI}	V_{UVI} = 1.2V			1	µA
UVI Hysteresis	UVH		10	20	30	mV
UVS Switch Resistance	R_{UVS}		1100	1540	2100	Ω
Thermal Shutdown Temperature	T_S	Temperature rising, $\overline{OT}$ output asserted (Note 3)	155	170		°C
Thermal Shutdown Hysteresis	T_H	(Note 3)		10	20	°C
OVERVOLTAGE GATE DRIVER						
Overvoltage Shutdown Level	V_{OV}	Input voltage rising, ODRV output turns off external pMOSFET	18.7	19.2	19.7	V
Overvoltage Shutdown Level	$V_{OV,F}$	Input voltage falling	18.1			V

Electrical Characteristics (continued)

(V_{INA} = V_{INB} = 14V, T_A = -40°C to +125°C, unless otherwise noted. Typical values are at T_A = +25°C.) (Note 2)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
ODRV Positive Output Drive Resistance	R_{DRV+}	Turning off		2000		Ω
ODRV Negative Output Drive Resistance	R_{DRV-}	Turning on		2000		Ω
DC-DC CONVERTERS						
Free-Running Switching Frequency Range	$f_{SWITCHI}$	SYNC = GND, MAX16920A	360	400	440	kHz
		SYNC = GND, MAX16920B	1980	2200	2420	
SYNC Input Frequency Range	f_{SYNC}	MAX16920A: switching frequency is half of f_{SYNC} (Note 3)	600		1000	kHz
		MAX16920B: switching frequency is equal to f_{SYNC} (Notes 3, 4)	1800		2400	
FB_ Voltage	$V_{FB\_}$	Output in regulation, 5.5V < $V_{IN\_}$ < 18V	1.196 (-2%)	1.22	1.244 (+2%)	V
Power-Good Threshold	PGT	Output rising for OUT2 and OUT3	88.5	91.5	94.5	% of V_{OUT} (NOM)
Power-Good Threshold Hysteresis	PGTH			3		%
$\overline{POR}$ Threshold	$\overline{POR}$	OUT1 rising	88.5	91.5	94.5	% of V_{OUT} (NOM)
$\overline{POR}$ Threshold Hysteresis	$\overline{PORH}$			3		%
$\overline{POR}$ Output Delay	$t_{\overline{POR}}$	MAX16920A	4.6	5.1	5.6	ms
		MAX16920B, Spread-spectrum disabled	6.75	7.5	8.25	
		MAX16920B, Spread-spectrum enabled	7	8	9	
DC-DC1 High-Side Switch R_{DSON}	R_{1H}				3	Ω
DC-DC1 Low-Side Switch R_{DSON}	R_{1L}				1.55	Ω
DC-DC1 V_{OUT1} Accuracy	V1	I_{OUT1} < 150mA, FB1 connected to GND, 6V < V_{INA} < 18V	-3%	3.3	+3%	V
DC-DC2 High-Side Switch R_{DSON}	R_{2H}				1.7	Ω
DC-DC2 Low-Side Switch R_{DSON}	R_{2L}				0.64	Ω
DC-DC2 V_{OUT2} Accuracy	V2	6V < V_{INB} < 18V, I_{OUT2} < 600mA, FB2 connected to GND	-3%	5	+3%	V
		5.5V < V_{INB} < 18V, I_{OUT2} = 400mA				
DC-DC3 High-Side Switch R_{DSON}	R_{3H}				0.7	Ω
DC-DC3 Low-Side Switch R_{DSON}	R_{3L}				0.3	Ω
DC-DC3 V_{OUT3} Accuracy	V3	4.5V < V_{INB} < 18V; I_{OUT3} = 500mA	-3%	3.3	+3%	V
		6V < V_{INB} < 18V; I_{OUT3} ≤ 1.5A				
DC-DC1 Output Current Limit	I_{LIM1}	Peak current limit	240	300	360	mA
DC-DC2 Output Current Limit	I_{LIM2}	Peak current limit	960	1200	1440	mA
DC-DC3 Output Current Limit	I_{LIM3}	Peak current limit	1920	2400	2880	mA

Electrical Characteristics (continued)

(V_{INA} = V_{INB} = 14V, T_A = -40°C to +125°C, unless otherwise noted. Typical values are at T_A = +25°C.) (Note 2)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
DC-DC Load Regulation	LoREG	DC-DC1 (0 to 150mA)			1		%
		DC-DC2 (0 to 600mA)			1.5		
		DC-DC3 (0 to 1.5A)			2.5		
DC-DC Line Regulation	LiREG	DC-DC1, V_{INA}, V_{INB} = 6V to 18V, I_{OUT1} = 15mA			3		mV/V
		DC-DC2, V_{INA}, V_{INB} = 6V to 18V, I_{OUT2} = 60mA			5		
		DC-DC3, V_{INA}, V_{INB} = 6V to 18V, I_{OUT3} = 150mA			3		
Soft-Start Time	t_{SS}	MAX16920A		8.5	10	11.5	ms
		MAX16920B	Spread-spectrum disabled	6.5	7.5	8.5	
			Spread-spectrum enabled	6.75	8	9.25	
Duty-Cycle Range (Note 3)	DCR	MAX16920A		3		97	%
		MAX16920B		11		96	
Input Voltage to Maintain Constant Switching with $V_{OUT\_}$ = 1.22V (Note 3)	V_{INDCL}	MAX16920A, limited by minimum duty cycle, DC-DC2 and DC-DC3 only				18	V
		MAX16920B, limited by minimum duty cycle, DC-DC2 and DC-DC3 only				8	
Spread-Spectrum Range	SS	Spread-spectrum option only			10		%
LINEAR REGULATOR (LDO)							
Output Voltage	V_{OUTA}	Output in regulation, I_{OUTA} < 100mA, V_{INA} = 6V to 18V		4.85	5	5.15	V
Operating Current	I_{CCA}	No load (excludes DC-DC_ operating current)			100		µA
Power-Good Threshold	PGTA	Output rising		88.5	91.5	94.5	% of V_{OUTA} (nom)
Power-Good Threshold Hysteresis	PGTAH				2		%
Output Current Limit	I_{LIMA}			200		300	mA
Dropout Voltage	V_{DA}	V_{INA} = 5V, I_{LDOA} = 100mA (Note 3)				0.5	V
Load Regulation	DI	I_{OUTA} = 5mA to 100mA			30		mV
Line Regulation	DV	V_{INA} = 6V to 18V, I_{OUTA} = 50mA			0.05		mV/V
LOGIC LEVELS							
$\overline{POR}$, PG_, $\overline{OT}$, and $\overline{UVO}$ Output Voltage Low	V_{OL}	Sink current = 1mA				0.4	V

Electrical Characteristics (continued)

(V_{INA} = V_{INB} = 14V, T_A = -40°C to +125°C, unless otherwise noted. Typical values are at T_A = +25°C.) (Note 2)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
EN2, EN3, ENA, SYNC Input Low Voltage	V_{IL}				0.4	V
EN2, EN3, ENA, SYNC Input High Voltage	V_{IH}		1.7			V
EN2, EN3, ENA, SYNC Input Hysteresis	V_H			200		mV
SYNC Input Pulldown Resistor	RSYNC		100	200	360	kΩ

Note 2: Operation at voltages outside the 5.5V to 18V range is guaranteed, but some parameters may be out of specification.

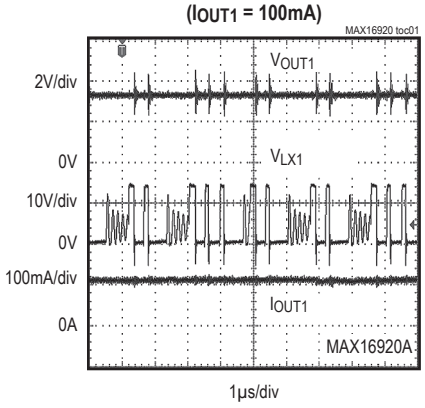
Note 3: Not production tested.

Note 4: The MAX16920BATJ/V+ with spread-spectrum disabled has a typical switching frequency of 2.2MHz, while the MAX16920BATJS/V+ is centered at 2.025MHz typically.

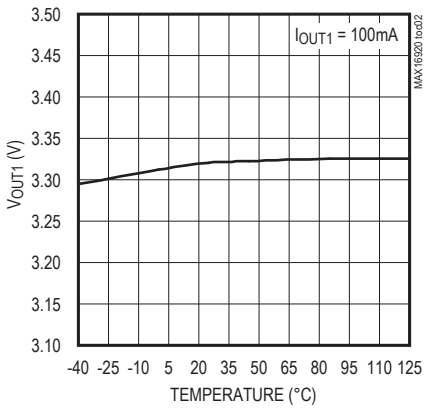
Typical Operating Characteristics

(V_{INA} = V_{INB} = 14V, T_A = +25°C, unless otherwise noted. Data measured on MAX16920B, see Figure 5 for application circuit.)

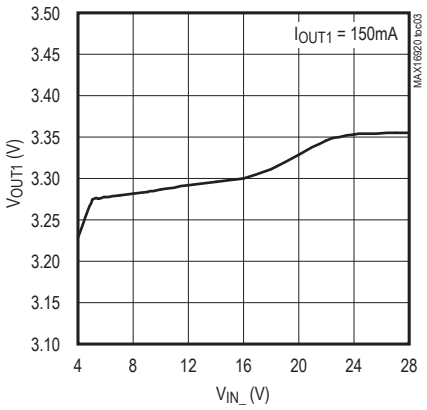
DC-DC1 SKIP MODE OPERATION (I_{OUT1} = 100mA)



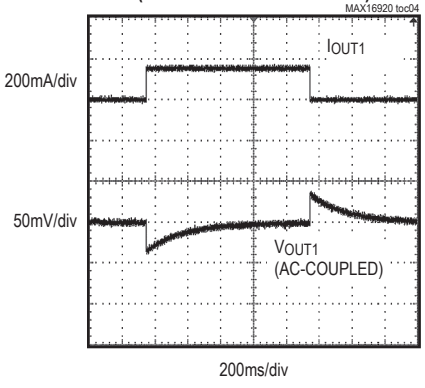
DC-DC1 OUTPUT VOLTAGE vs. TEMPERATURE



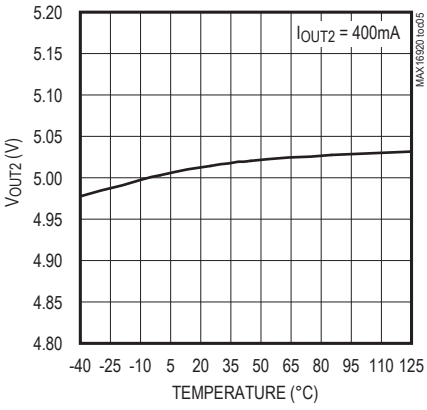
DC-DC1 LINE REGULATION



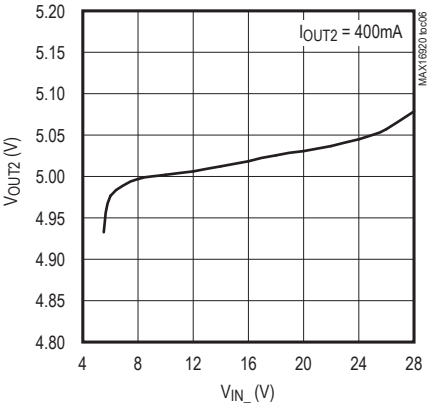
DC-DC1 LOAD REGULATION (15mA TO 150mA TO 15mA)



DC-DC2 OUTPUT VOLTAGE vs. TEMPERATURE



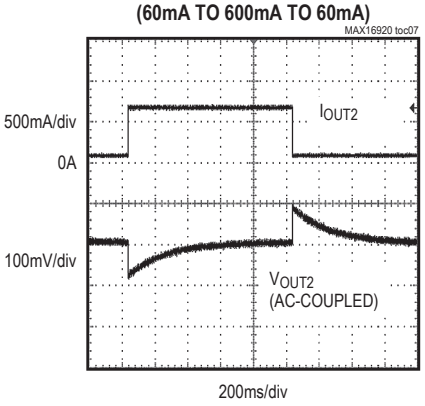
DC-DC2 LINE REGULATION



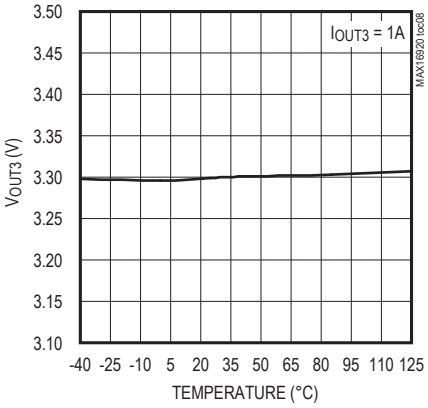
Typical Operating Characteristics (continued)

(V_{INA} = V_{INB} = 14V, T_A = +25°C, unless otherwise noted. Data measured on MAX16920B, see Figure 5 for application circuit.)

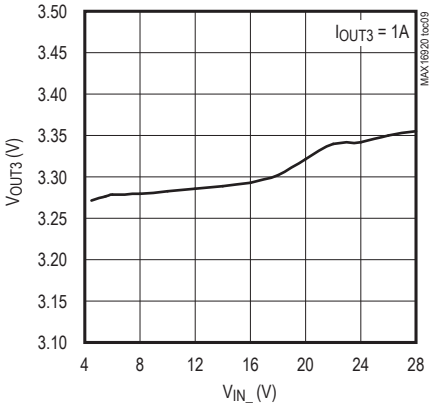
DC-DC2 LOAD REGULATION (60mA TO 600mA TO 60mA)



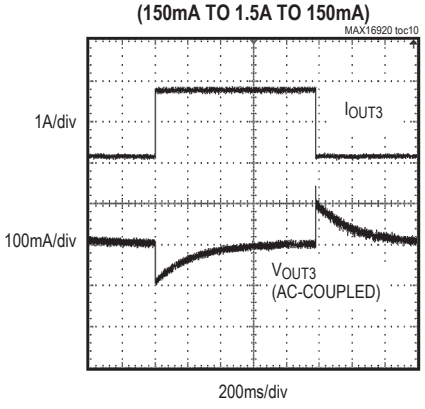
DC-DC3 OUTPUT VOLTAGE vs. TEMPERATURE



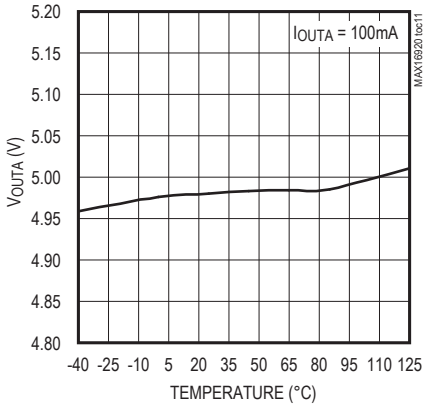
DC-DC3 LINE REGULATION



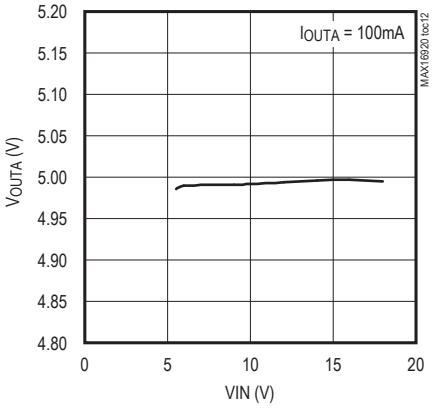
DC-DC3 LOAD REGULATION (150mA TO 1.5A TO 150mA)



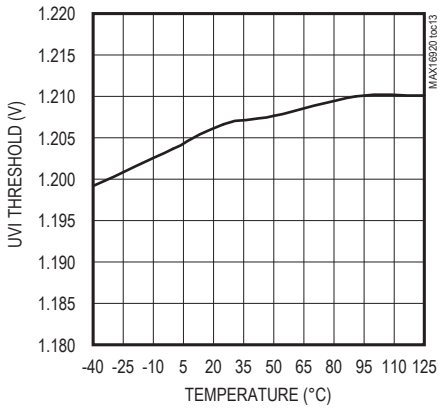
LDOA OUTPUT VOLTAGE vs. TEMPERATURE



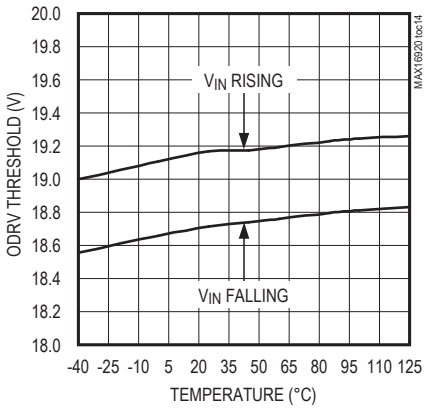
LDOA LINE REGULATION



UVI THRESHOLD vs. TEMPERATURE



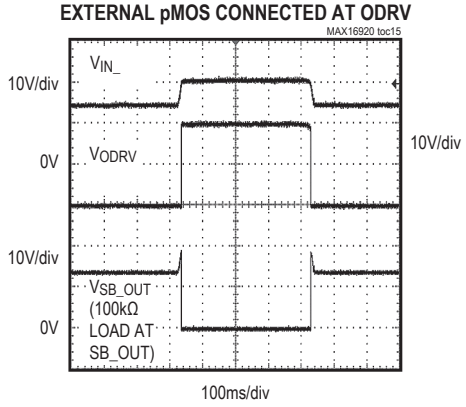
ODRV THRESHOLD vs. TEMPERATURE



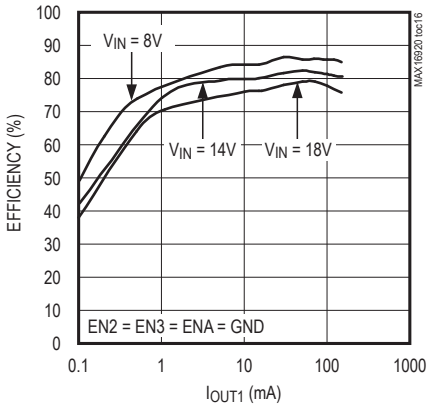
Typical Operating Characteristics (continued)

(V_{INA} = V_{INB} = 14V, T_A = +25°C, unless otherwise noted. Data measured on MAX16920B, see Figure 5 for application circuit.)

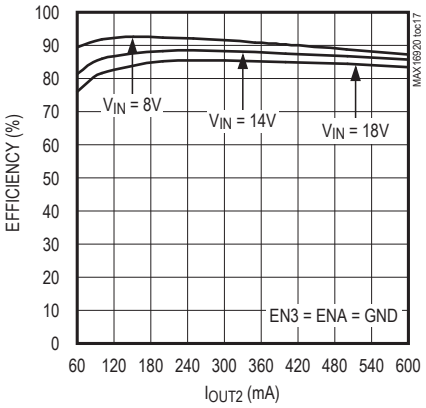
**ODRV SWITCH ON/OFF
SB_OUT IS THE "DRAIN" SIDE OF THE
EXTERNAL pMOS CONNECTED AT ODRV**



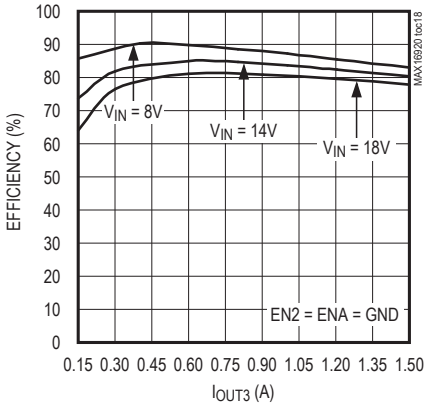
DC-DC1 EFFICIENCY vs. LOAD CURRENT



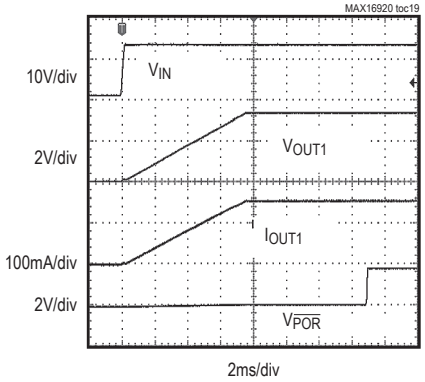
DC-DC2 EFFICIENCY vs. LOAD CURRENT



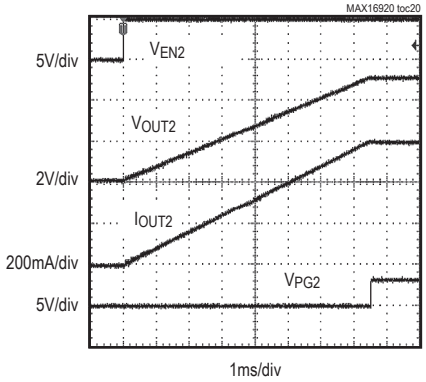
DC-DC3 EFFICIENCY vs. LOAD CURRENT



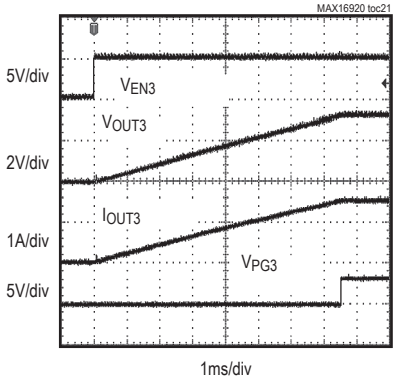
DC-DC1 STARTUP INTO FULL LOAD



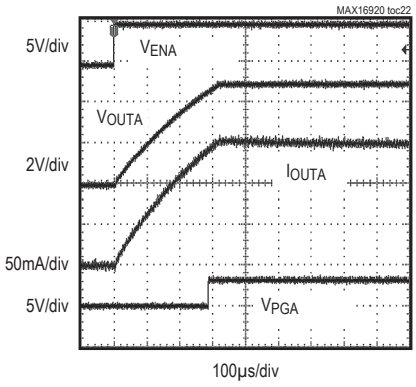
DC-DC2 STARTUP INTO FULL LOAD



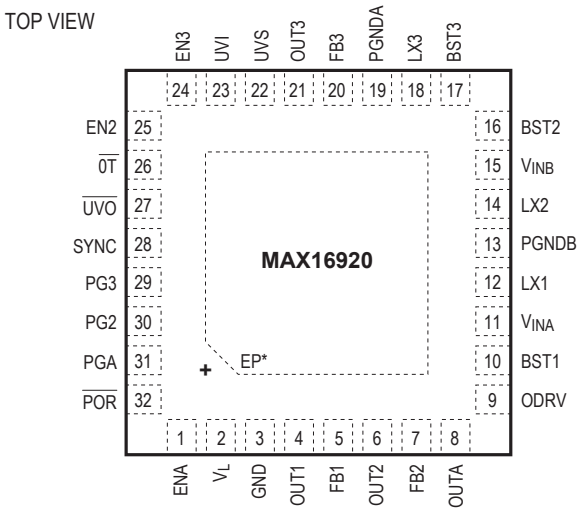
DC-DC3 STARTUP INTO FULL LOAD



LDOA STARTUP INTO FULL LOAD



Pin Configuration



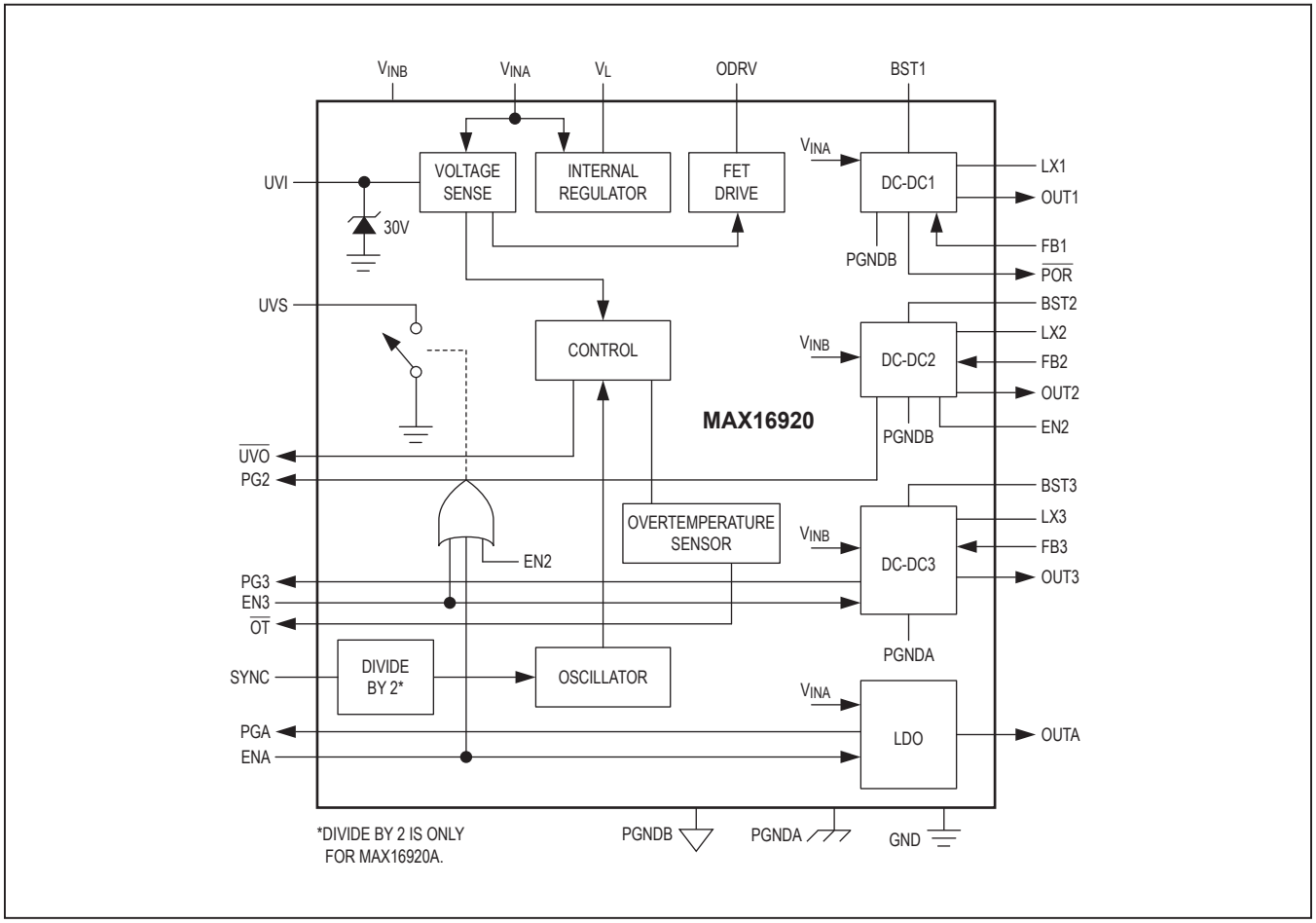
Pin Description

PIN	NAME	FUNCTION
1	ENA	LDO Enable Input. Drive ENA high to enable the LDO (OUTA). Drive low to disable the LDO.
2	V_L	Internal Regulator Output. Bypass V_L to GND with a 4.7µF capacitor.
3	GND	Ground
4	OUT1	DC-DC1 Converter Output. OUT1 supplies internal circuitry in standby mode reducing overall current consumption. Connect a 0.1µF capacitor from OUT1 to GND as close as possible to the IC. If the DC-DC1 output is pulled below its power-on-reset threshold ($\overline{POR}$), DC-DC2 and DC-DC3 are automatically disabled.
5	FB1	DC-DC1 Converter Feedback Input. Connect FB1 to GND for a fixed 3.3V output. Connect to a resistive divider to adjust the output voltage between 1.22V and 5.5V.
6	OUT2	DC-DC2 Converter Output
7	FB2	DC-DC2 Converter Feedback Input. Connect FB2 to GND for a fixed 5V output. Connect to a resistive divider to adjust the output voltage between 1.22V and 5V.
8	OUTA	5V Linear Regulator Output. Connect an external capacitor of at least 4.7µF from OUTA to GND.
9	ODRV	External pMOS Output Drive Signal. ODRV turns off the pMOS during overvoltage events. If only DC-DC1 is running, the overvoltage circuit is disabled and the external pMOS is turned off.
10	BST1	Bootstrap Capacitor Connection for DC-DC1. Connect a 0.47µF capacitor from BST1 to LX1.
11	V_{INA}	Battery Supply-Voltage Input. V_{INA} supplies power to the V_L regulator, the LDO, and DC-DC1.
12	LX1	DC-DC1 Converter Switching Node. Connect an LC filter to LX1. Use a capacitor with a maximum ESR of 0.3Ω. Unless there is an undervoltage lockout, DC-DC1 is always on when power is applied.

Pin Description (continued)

PIN	NAME	FUNCTION
13	PGNDB	Power Ground for DC-DC1 and DC-DC2
14	LX2	DC-DC2 Converter Switching Node. Connect an LC filter to LX2. Use a capacitor with a maximum ESR of 0.3Ω.
15	V_{INB}	Battery Supply-Voltage Input. V_{INB} supplies power to DC-DC2 and DC-DC3.
16	BST2	Bootstrap Capacitor Connection for DC-DC2. Connect a 0.1µF capacitor from BST2 to LX2.
17	BST3	Bootstrap Capacitor Connection for DC-DC3. Connect a 0.1µF capacitor from BST3 to LX3.
18	LX3	DC-DC3 Converter Switching Node. Connect an LC filter to LX3. Use a capacitor with a maximum ESR of 0.3Ω.
19	PGNDA	Power Ground for DC-DC3
20	FB3	DC-DC3 Feedback Input. Connect FB3 to GND for a fixed 3.3V output. Connect to a resistive divider to adjust the output voltage between 1.22V and 8V.
21	OUT3	DC-DC3 Converter Output
22	UVS	Undervoltage Switch. This switch connects the undervoltage resistor-divider to ground during normal operation. When only DC-DC1 is running, this switch is open to reduce current consumption, and the undervoltage circuit is not active.
23	UVI	Undervoltage Lockout Sense Input. Connect a resistor-divider between the battery, UVI, and UVS to set the undervoltage lockout level. The nominal threshold for UVI is 1.205V.
24	EN3	DC-DC3 Converter Enable Input. Drive EN3 high to enable the DC-DC3 converter. Drive low to disable the DC-DC3 converter.
25	EN2	DC-DC2 Converter Enable Input. Drive EN2 high to enable the DC-DC2 converter. Drive low to disable the DC-DC2 converter.
26	$\overline{OT}$	Active-Low Open-Drain Overtemperature Output. $\overline{OT}$ output low indicates that all converters except DC-DC1 are in shutdown due to an overtemperature condition.
27	$\overline{UVO}$	Active-Low Open-Drain Undervoltage Output. $\overline{UVO}$ asserts low when the voltage at UVI falls below 1.205V ±2%. The $\overline{UVO}$ output is high impedance when only DC-DC1 is operating (standby mode).
28	SYNC	DC-DC Converters Synchronization Input. For MAX16920A, the SYNC frequency is divided by 2, whereas for the MAX16920B the switching frequency is same as the SYNC frequency. Connect SYNC to GND if SYNC is not used. The SYNC input is a Schmitt trigger type to accommodate a lowpass-filtered square-wave input. The duty-cycle range of the signal is 30% to 70%. The SYNC input has an internal 200kΩ pulldown resistor.
29	PG3	DC-DC3 Open-Drain Power-Good Output. PG3 goes low when OUT3 is out of regulation. In standby mode, PG3 is high-impedance.
30	PG2	DC-DC2 Open-Drain Power-Good Output. PG2 goes low when OUT2 is out of regulation. In standby mode, PG2 is high-impedance.
31	PGA	Linear Regulator Open-Drain Power-Good Output. PGA goes low when LDO is out of regulation. In standby mode, PGA is high-impedance.
32	$\overline{POR}$	Active-Low Open-Drain Reset Output from DC-DC1. $\overline{POR}$ is low when DC-DC1 is out of regulation and has a delay time of 7.5ms to 8ms in the MAX16920B (2MHz) and 5.1ms in the MAX16920A (400kHz).
—	EP	Exposed Pad. Connect the exposed pad to ground.

Functional Diagram



Detailed Description

The MAX16920 power-management IC integrates three high-voltage step-down DC-DC converters, one high-voltage linear regulator, and an overvoltage protection block. The three step-down converters deliver up to 150mA, 600mA, and 1.5A, while the linear regulator is capable of up to 150mA. The MAX16920 is designed to operate with input voltages between 5.5V to 28V and survive voltage transients to 45V, making it ideal for automotive applications.

The MAX16920 is optimized for high efficiency and low standby current. The MAX16920A features 400kHz switching frequency, while the MAX16920B features 2MHz switching frequency. The DC-DC converters can also be synchronized to an external frequency reference to ensure low EMI. The MAX16920 includes power-good outputs (PG_) for DC-DC2, DC-DC3, LDOA, and a power-on-reset ($\overline{POR}$) output for DC-DC1. All regulators other than DC-DC1 have an enable input (EN_).

DC-DC1

DC-DC1 is an always-on, high-efficiency, step-down converter that outputs up to 150mA. The DC-DC1 has a 5.5V to 28V wide input voltage range and provides a fixed 3.3V output, or provides an adjustable output between 1.22V to 5.5V. DC-DC1 operates in PWM mode or in skip mode.

Soft-Start

DC-DC1 features an internal soft-start timer. The output voltage soft-start ramp time is 10ms (typ) for the MAX16920A, and 7.5ms to 8ms (typ) for the MAX16920B. If a short circuit is encountered, after the soft-start timer has expired, the device is disabled for 40ms (typ) (for MAX16920A) or 28ms (typ) (for MAX16920B) and then reattempts soft-start. This pattern repeats until the short circuit has been removed.

Adjusting Output Voltage

DC-DC1 provides a fixed 3.3V output or an adjustable output between 1.22V to 5.5V. Connect FB1 to GND to set the OUT1 voltage to a fixed 3.3V voltage. Connect a resistive divider between OUT1, FB1, and GND to adjust the output voltage. When OUT1 is set to a voltage greater than 3.3V, additional resistors are needed between the converter output, OUT1 and GND. See the *Setting the Output Voltage (DC-DC1, DC-DC2, DC-DC3)* section for more information.

Overcurrent Protection

DC-DC1 limits the peak output current to 300mA (typ). The accuracy of the current limit is ±20%, which makes selection of external components very easy. To protect against short-circuit events, the MAX16920 shuts off if the current limit is exceeded and OUT1 is below 1.5V. DC-DC1 attempts a soft-start restart every 40ms (typ) (for MAX16920A) or 28ms (typ) (for MAX16920B) and stays off if the short circuit has not been removed. When the short circuit is no longer present, normal operation resumes with the output voltage following the normal soft-start sequence. If the MAX16920 die reaches the thermal limit of +170°C (typ), all outputs except OUT1 are immediately shut off.

Power-On Reset

DC-DC1 features an open-drain reset output ($\overline{POR}$). If OUT1 exceeds 91.5% of its nominal output voltage, the $\overline{POR}$ output goes high after a delay time of 5.1ms (typ) for the MAX16920A, or 7.5ms to 8ms (typ) for the MAX16920B. Contact the factory for other $\overline{POR}$ delay options.

Standby and Skip Mode

When EN2, EN3, and ENA are all logic-low, the MAX16920 consumes a standby current of 25µA (typ) with no load on OUT1. If I_{OUT1} < 170mA (typ), DC-DC1 operates in skip mode. Also, the power-good outputs (PG_) are high impedance and the undervoltage circuit is inactive in standby mode. When any other channel (DC-DC2, DC-DC3, or LDOA) is enabled, DC-DC1 operates in constant PWM mode to improve EMI performance.

Holding Up the OUT1 During Input Undervoltage Events

It is possible to make DC-DC1 more immune to input voltage dropouts by adding extra capacitance buffered by means of a diode on the V_{INA} pin as shown in Figure 1. This is useful if OUT1 powers the main system processor, which needs to remain powered for as long as possible. Estimate the size of the hold-up capacitor needed on V_{INA} using the following formula:

$$C_{VINA} = (I_{IN1} \times t_H)/\Delta V$$

where I_{IN1} is the estimated input current to DC-DC1, t_H is the hold-up time, and ΔV is the drop-in voltage on C_{VINA} that can be tolerated. To prolong the hold-up time, the LDO should be disabled during undervoltage events. If this is not possible, the supply and load current of the LDO should be taken into account in the calculation.

DC-DC2

DC-DC2 is a high-efficiency step-down converter that outputs up to 600mA. DC-DC2 has a 5.5V to 28V input voltage range and provides a fixed 5V output or

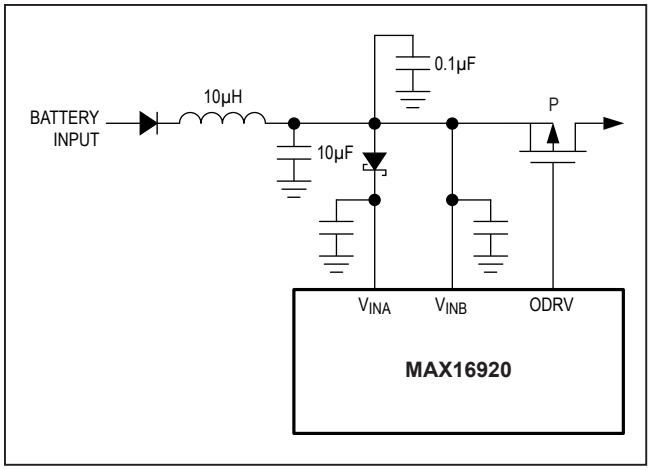


Figure 1. Holding Up OUT1 During Input Undervoltage Events

an adjustable output between 1.22V to 5.5V. DC-DC2 operates in PWM mode only.

DC-DC2 is activated by driving EN2 high.

Soft-Start

DC-DC2 features an internal soft-start timer with a ramp time of 10ms (typ) for the MAX16920A, and 7.5ms to 8ms (typ) for the MAX16920B. The soft-start at OUT2 is initiated when OUT1 reaches a power-good condition and EN2 is high. If a short circuit is encountered, after the soft-start timer has expired, DC-DC2 is disabled for 40ms (typ) (for MAX16920A) or 28ms (typ) (for MAX16920B) and it reattempts soft-start. This pattern repeats until the short circuit has been removed.

Adjusting Output Voltage

DC-DC2 provides a fixed 5V output or an adjustable output between 1.22V to 5.5V. Connect FB2 to GND to set the OUT2 voltage to a fixed 5V. Connect a resistive divider between OUT2, FB2, and GND to adjust the output voltage. See the *Setting the Output Voltage (DC-DC1, DC-DC2, DC-DC3)* section for more information.

Overcurrent Protection

DC-DC2 limits the peak output current to 1.2A (typ). The accuracy of the current limit is ±20%, which makes selection of external components very easy. To protect against short-circuit events, the MAX16920 shuts off DC-DC2 if OUT2 is below 1.5V and one overcurrent event is detected. DC-DC2 attempts a soft-start restart every 40ms (typ) (for MAX16920A) or 28ms (typ) (for MAX16920B)) and stays off if the short circuit has not been removed. When the short-circuit is no longer present, normal operation resumes with the output voltage following the normal soft-start sequence. If the MAX16920 die reaches the thermal limit of +170°C (typ) (temperature rising) OUT2 is immediately shut off.

Power-Good Output (PG2)

DC-DC2 provides an open-drain power-good output (PG2). PG2 is an active-high output that pulls high when the output voltage (OUT2) is above 91.5% of its nominal value. In standby mode PG2 is high impedance.

DC-DC3

DC-DC3 is a high-efficiency step-down converter that outputs up to 1.5A. DC-DC3 has a 5.5V to 28V input voltage range and provides a fixed 3.3V output or provides an adjustable output between 1.22V to 8V. DC-DC3 operates in PWM mode only.

DC-DC3 is activated by driving EN3 high.

Soft-Start

DC-D3 features an internal soft-start timer. The OUT3 soft-start ramp time is 10ms (typ) for the MAX16920A, and 7.5ms to 8ms (typ) for the MAX16920B. A soft-start at OUT3 is initiated when OUT1 reaches the power-good condition and EN3 is taken high. If a short circuit is encountered, after the soft-start timer has expired, DC-DC3 is disabled for 40ms (typ) (for MAX16920A) or 28ms (typ) (for MAX16920B) and it reattempts soft-start. This pattern repeats until the short circuit has been removed.

Adjusting Output Voltage

DC-DC3 provides a fixed 3.3V output or provides an adjustable output between 1.22V to 8V. Connect FB3 to GND to set the OUT3 voltage to 3.3V. Connect a resistive divider between OUT3, FB3, and GND to adjust the output voltage. When OUT3 is set to a voltage greater than 3.3V, additional resistors are needed between the converter output, OUT3 and GND. See the *Setting the Output Voltage (DC-DC1, DC-DC2, DC-DC3)* section for more information.

Overcurrent Protection

The DC-DC3 limits the peak output current to 2.4A (typ). The accuracy of the current limit is ±20%, which makes the selection of external components very easy. To protect against short-circuit events, the MAX16920 shuts off if OUT3 is below 1.5V and one overcurrent event is detected. The DC-DC3 attempts a soft-start restart every 40ms (typ) (for MAX16920A) or 28ms (typ) (for MAX16920B) and stays off if the short circuit has not been removed. When the short circuit is no longer present, normal operation resumes with the output voltage following the

normal soft-start sequence. If the MAX16920 die reaches the thermal limit of +170°C (typ) (temperature rising), OUT3 is immediately shut off.

Power-Good Output (PG3)

DC-DC3 provides an open-drain power-good output (PG3). PG3 is an active-high output that pulls high when the output voltage (OUT3) is above 91.5% of its nominal value. In standby mode, PG3 is high impedance.

Linear Regulator (OUTA)

The MAX16920 features a fixed 5V output linear regulator (OUTA). OUTA provides up to 150mA load current. Connect an external capacitor of at least 4.7µF from OUTA to GND. OUTA is activated by driving ENA high.

Power-Good Output (PGA)

OUTA provides an open-drain power-good output (PGA). PGA is an active-high output that pulls high when the output voltage (OUTA) is above 91.5% of its nominal value. In standby mode, PGA is high impedance.

Overcurrent Protection

The OUTA output current is limited to 200mA (min). If the output current exceeds the current limit, OUTA drops out of regulation. Excess power dissipation in the device can cause the device to turn off due to thermal shutdown.

Dropout

The dropout voltage for the linear regulator (OUTA) is 500mV (max) at 100mA load. To avoid dropout, make sure the input supply voltage is greater than the output voltage plus the dropout voltage based on the application output current requirements.

Switching Frequency

The MAX16920AATJ/V+ provides a fixed 400kHz switching frequency, whereas the MAX16920BATJ/V+ provides a fixed 2.2MHz switching frequency. Connect SYNC to GND when using the internal switching frequency. For external synchronization, see the *DC-DC Synchronization (SYNC)* section.

Spread-Spectrum Option

The MAX16920AATJS/V+ and MAX16920BATJS/V+ have a built-in spread-spectrum oscillator. The internal operating frequency varies by +10% relative to the internally generated operating frequency of 400kHz (typ) for MAX16920AATJS/V+ and 2.025MHz (typ) for MAX16920BATJS/V+. Spread spectrum improves the EMI performance of the MAX16920 in some applications. By varying the frequency 10% only in the positive direction, the switching frequency of MAX16920BATJS/V+ never drops below the AM radio band upper limit of 1.8MHz. The internal spread spectrum does not interfere with the external clock applied on the SYNC pin. It is active only when generating the switching frequency internally.

DC-DC Synchronization (SYNC)

The SYNC input provides for synchronization of the DC-DC converters. The MAX16920 defaults to the internal switching frequency during startup or when a SYNC input signal is not provided. For external synchronization, provide a signal between 600kHz and 1000kHz for the MAX16920A and between 1800kHz and 2400kHz for the MAX16920B. The MAX16920A divides the SYNC frequency by a factor of 2 before feeding to the DC-DC converters, whereas the MAX16920B feeds the SYNC frequency as it is to the DC-DC converters. The duty cycle of the SYNC signal should be in the 30% to 70% range. The SYNC input has an internal 200kΩ pulldown resistor.

Controlled EMI with Forced-Fixed Frequency

Under normal operating conditions, the MAX16920 attempts to operate at a constant switching frequency for all load currents (DC-DC1 enters skip mode below its skip-mode threshold). For tightest frequency control, apply the operating frequency to SYNC. The advantage of this is a more accurate switching frequency and more predictable EMI characteristics.

Extremes of Input Voltage

In some cases, especially at high switching frequencies, the MAX16920 is forced to deviate from its operating frequency independent of the state of SYNC. For input voltages above 18V, the required duty cycle to regulate the output can be lower than the minimum on-time of the high-side switch (90ns typ). In this event, the MAX16920 is forced to lower its switching frequency by skipping pulses. In an analogous fashion when the input voltage is reduced and the MAX16920 approaches dropout, the device attempts to turn on the high-side FET continuously. However, to maintain gate charge on the high-side FET, the BST capacitor must be periodically recharged. To ensure proper charge on the BST capacitor when in dropout, the high-side FET is turned off every 5.5µs for the MAX16920B and the low-side FET is turned on for about 150ns. This gives an effective duty cycle of > 97% and a switching frequency of 180kHz when in dropout. (The MAX16920A refreshes the BST capacitor every 7.5µs for 150ns and switches at 133kHz when in dropout.)

Undervoltage Output *($\overline{UVO}$)*

The MAX16920 features an active-low undervoltage output ($\overline{UVO}$) to monitor the input voltage. $\overline{UVO}$ is pulled low when the voltage at UVI falls below 1.205V. To monitor battery voltage, connect a resistive divider between the battery, UVI, and UVS. An undervoltage condition asserts the $\overline{UVO}$ flag only and does not effect the regulator outputs.

In case only DC-DC1 is running, $\overline{UVO}$ is high impedance.

For more details, see the *Setting the Undervoltage Output ($\overline{UVO}$) Level* section.

Overvoltage Output (ODRV)

The MAX16920 features an overvoltage output (ODRV) that can be used to create an overvoltage-protected battery output with the addition of an external pMOS transistor. If V_{INA} exceeds 19.2V (typ), the ODRV output is driven high, which turns off the external pMOS. An overvoltage condition does not affect any of the other MAX16920 converters.

Choose an external pMOS transistor with a low-enough R_{DSON} so that voltage loss and power dissipation at the nominal output current are acceptable. Very low R_{DSON} pMOS transistors have larger effective input capacitance and thus are switched more slowly by the ODRV output. When only DC-DC1 is running, ODRV is high and the external pMOS is off.

Overtemperature Protection *($\overline{OT}$)*

The MAX16920 features an active-low overtemperature output ($\overline{OT}$). The MAX16920 pulls the $\overline{OT}$ output low and disables all the regulators except DC-DC1, if the die temperature exceeds the thermal shutdown temperature (T_S).

Applications Information

Inductor Selection

Three key inductor parameters must be specified for operation with the MAX16920: inductance value (L), peak inductor current (I_{PEAK}), and inductor saturation current (I_{SAT}). The minimum required inductance is a function of operating frequency, input-to-output voltage differential, and the peak-to-peak inductor current (ΔI_{P-P}). Higher ΔI_{P-P} allows for a lower inductor value, while a lower ΔI_{P-P} requires a higher inductor value. A lower inductor value minimizes size and cost, improves large-signal and transient response, but reduces efficiency due to higher peak currents and higher peak-to-peak output-voltage ripple for the same output capacitor. On the other hand, higher inductance increases efficiency by reducing the ripple current. Resistive losses due to extra wire turns can exceed the benefit gained from lower ripple current levels, especially when the inductance is increased without also allowing for larger inductor dimensions. A good compromise is to choose ΔI_{P-P} equal to 30% of the full load current.

Use the following equation to calculate the inductance:

$$L = V_{OUT} (V_{IN} - V_{OUT})/(V_{IN} \times f_{SW} \times \Delta I_{P-P})$$

V_{IN} and V_{OUT} are typical values so that efficiency is optimum for typical conditions. The peak-to-peak inductor current, which reflects the peak-to-peak output ripple, is larger at the maximum input voltage. See the *Output Capacitor Selection* section to verify that the worst-case output ripple is acceptable. The inductor saturation current is also important to avoid runaway current during continuous output short circuit. Choose an inductor with a saturation current of greater than the maximum current limit to ensure proper operation and avoid runaway.

Input Capacitor Selection

The discontinuous input current of the buck converter causes large input ripple current. The switching frequency, peak inductor current, and the allowable peak-to-peak input-voltage ripple dictate the input capacitance requirement. Increasing the switching frequency or the inductor value lowers the peak-to-average current ratio, yielding a lower input capacitance requirement.

The input ripple consists mainly of ΔV_Q (caused by the capacitor discharge) and ΔV_{ESR} (caused by the ESR of the input capacitor). The total voltage ripple is the sum of ΔV_Q and ΔV_{ESR}. Assume the input voltage ripple from the ESR and the capacitor discharge is equal to 50% each. The following equations show the ESR and capacitor requirement for a target voltage ripple at the input:

$$ESR = \frac{\Delta V_{ESR}}{\left(I_{OUT} + \frac{\Delta I_{P-P}}{2}\right)}$$

$$C_{IN} = \frac{I_{OUT} \times D(1-D)}{\Delta V_Q \times f_{SW}}$$

where:

$$\Delta I_{P-P} = \frac{(V_{IN} - V_{OUT}) \times V_{OUT}}{(V_{IN} \times f_{SW} \times L)}$$

and:

$$D = \frac{V_{OUT}}{V_{IN}}$$

where I_{OUT} is the output current, D is the duty cycle, and f_{SW} is the switching frequency. Use additional input capacitance at lower input voltages to avoid possible undershoot below the UVLO threshold during transient loading.

Output Capacitor Selection

The allowable output voltage ripple and the maximum deviation of the output voltage during step load currents determine the output capacitance and its ESR. The output ripple is composed of ΔV_Q (caused by the capacitor discharge) and ΔV_{ESR} (caused by the ESR of the output capacitor). Use low-ESR ceramic or aluminum electrolytic capacitors at the output. For aluminum electrolytic capacitors, the entire output ripple is contributed by ΔV_{ESR}. Use the ESR_{OUT} equation to calculate the ESR requirement and choose the capacitor accordingly. If using ceramic capacitors, assume the contribution to the output ripple voltage from the ESR and the capacitor discharge to be equal. The following equations show the output capacitance and ESR requirement for a specified output voltage ripple.

$$ESR = \Delta V_{ESR}/\Delta I_{P-P}$$

$$C_{OUT} = \Delta I_{P-P}/(8 \times \Delta V_Q \times f_{SW})$$

where:

$$\Delta I_{P-P} = (V_{IN} - V_{OUT}) \times V_{OUT}/(V_{IN} \times f_{SW} \times L)$$

$$V_{OUT\_RIPPLE} \sim \Delta V_{ESR} + \Delta V_Q$$

ΔI_{P-P} is the peak-to-peak inductor current as calculated above, and f_{SW} is the converter's switching frequency. The allowable deviation of the output voltage during fast transient loads also determines the output capacitance and its ESR. The output capacitor supplies the load-step current until the converter responds with a greater duty cycle. The response time ($t_{RESPONSE}$) depends on the closed-loop bandwidth of the converter. The high switching frequency of the MAX16920 allows for a higher closed-loop bandwidth, thus reducing $t_{RESPONSE}$ and the output capacitance requirement. The resistive drop across the output capacitor's ESR and the capacitor discharge causes a voltage droop during a load step. Use low-ESR ceramic capacitors for better transient load and ripple/noise performance. Keep the maximum output voltage deviations below the tolerable limits of the electronics being powered. When using a ceramic capacitor, assume an 80% and 20% contribution from the output capacitance discharge and the ESR drop, respectively. Use the following equations to calculate the required ESR and capacitance value:

$$ESR_{OUT} = \Delta V_{ESR}/I_{STEP}$$

$$C_{OUT} = (I_{STEP} \times t_{RESPONSE})/\Delta V_Q$$

where I_{STEP} is the load step, and $t_{RESPONSE}$ is the response time of the converter. The converter response time depends on the control-loop bandwidth.

Electrolytic output capacitors can be used if a 2.2µF ceramic capacitor is connected in parallel. At output currents lower than the maximum, smaller capacitors can be used. Use a 4.7µF or larger ceramic capacitor on the output of the linear regulator, OUTA.

Setting the Output Voltage (DC-DC1, DC-DC2, DC-DC3)

The output voltage for any of the DC-DC converters is set by selecting resistor R1 according to the formula:

$$R1 = R2 \times ((V_{OUT\_}/1.22) - 1)$$

where $V_{OUT\_}$ is the desired output voltage, and R2 is the value of the ground connected resistor (a good starting value is 30kΩ). See Figure 2. When setting DC-DC1 or DC-DC3 to output voltages higher than 3.3V. It is necessary to add an additional resistive divider between the converter output and the OUT1 or OUT3 pins. Resistor values of 100kΩ and 50kΩ work well in all applications. See Figure 3 for the exact configuration.

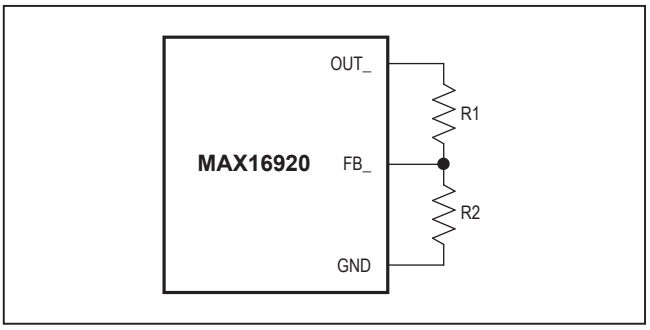


Figure 2. Setting the Output Voltage

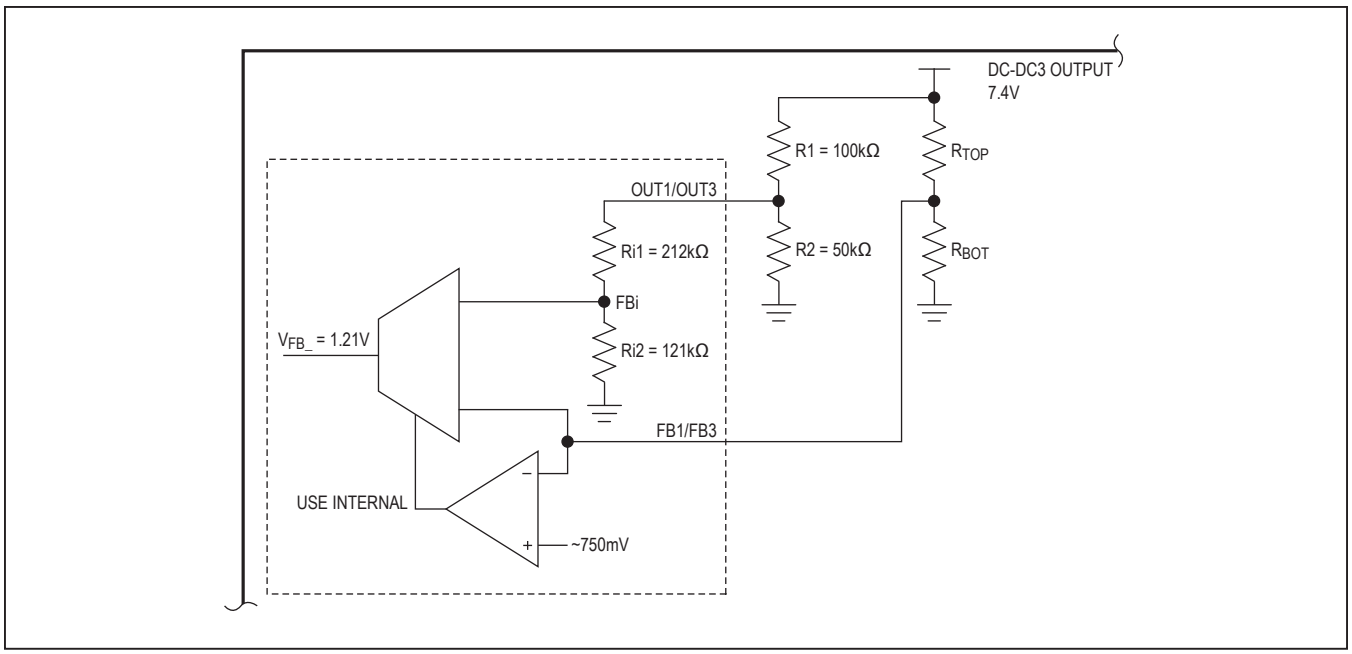


Figure 3. Typical Application Circuit for Setting OUT1 or OUT3 Above 3.3V

Setting the Undervoltage Output ($\overline{UVO}$) Level

The $\overline{UVO}$ level is set by using two resistors connected between the input (before the reverse-polarity protection diode if used) and the UVI and between UVI and UVS. The UVS switch has a 1540Ω typical resistance that must be taken into account when calculating the external resistor values to maintain accuracy. Use the following equation to calculate the value of the upper resistor, R1:

$$R1 = (V_{BT} – 1.205)/(1.205/(R2 + R_{UVS}))$$

where V_{BT} is the desired undervoltage level at the battery, and R2 is the value of the lower resistor (a good starting value is 100kΩ). R_{UVS} is 1540Ω. See the *typical operating circuits* in Figures 4 and 5.

PCB Layout Guidelines

Grounding

Establish a “quiet” ground for all analog ground (GND) connections. Sources of switching current and other noisy signals should be connected to their respective power grounds (PGNDA and PGNDB). GND, PGNDA, and PGNDB should be connected together at the GND pin of the MAX16920. If needed, use multiple vias to connect ground planes between different board layers to keep the ground impedance low.

The following should be connected to analog GND:

1) The GND pin of the MAX16920.
2) The ground connection of the V_L capacitor.
3) The grounds for any feedback resistor-dividers used.
4) The ground side of the OUTA output capacitor.

All other ground connections should be to their respective PGNDA and PGNDB grounds.

General Guidelines

1) Minimize the area of high-current loops by placing each DC-DC converter’s inductor and output capacitors near its input capacitors and its LX_ and PGND_ pins. OUT1 and OUT2 converters share PGNDB for ground return, while OUT3 has PGNDA for ground return.
2) Keep the power traces and load connections as short and wide as possible, especially at the ground terminals. This practice is essential for high efficiency and jitter-free operation.
3) Use thick copper PCBs (2oz. vs. 1oz.) if possible to enhance efficiency.
4) Keep the LX_ connections short and wide and place the inductors as close as possible to the associated LX pin.

5) Route high-speed switching nodes (BST_ and LX_) away from sensitive analog areas (SYNC and FB_) and keep their area as small as possible.
6) Place the V_{INA}, V_{INB}, and V_L bypass capacitors as close as possible to the device. If using multiple bypass capacitors, place the lowest value capacitor closest to the pin. The ground connection of the V_L bypass capacitor should be connected directly to the GND pin with a wide trace.
7) Keep any feedback traces as short and small as possible to prevent noise pickup. Make feedback connections directly to the positive terminal of the output capacitor to ensure good regulation.

Thermal Considerations

The power dissipation of the MAX16920 is made up of three components: power dissipation due to the DC-DC converters, power dissipation due to the linear regulator, and internal power dissipation. The DC-DC converter power dissipation can be estimated as follows:

$$P_{DCDC} = P_{RESISTIVE} + P_{SWITCHING}$$

$$P_{RESISTIVE} = D \times I_{OUT}^2 \times R_H + (1 - D) \times I_{OUT}^2 \times R_L$$

where D is the duty cycle (approximately V_{OUT}/V_{IN}), I_{OUT} is the output current, R_H is the resistance of the high-side switch, and R_L is the resistance of the low-side switch.

$$P_{SWITCHING} = f_{SW} \times (0.25 \times V_{IN} \times I_{OUT} \times t_{RISE} + 0.25 \times V_{IN} \times I_{OUT} \times t_{FALL})$$

where V_{IN} is the input voltage, t_{RISE} is the rise time of the LX node (approximately 5ms (MAX16920B) and 10ms (MAX16920A)), and t_{FALL} is the fall time of the LX node (approximately 5ms (MAX16920B) and 10ms (MAX16920A)).

The linear regulator power dissipation is:

$$P_{LIN} = (V_{IN} - 5V) \times I_{LIN}$$

The internal power dissipation can be approximately calculated as $V_{IN\_} \times 35mA$ during normal operation. In many applications, the power dissipation of the linear regulator (LDOA) is a large contributor to the overall power dissipation. Note that although the linear regulator can provide up to 150mA of output current, in most cases the permitted output current is lower due to power dissipation limitations.

The total power dissipation leads to an increase in the chip temperature, which is dependent on the thermal resistance of the board upon which the MAX16920 is mounted. The maximum permitted junction temperature is +150°C and a junction temperature above this eventually leads to overtemperature shutdown of the chip.

Typical Operating Circuits

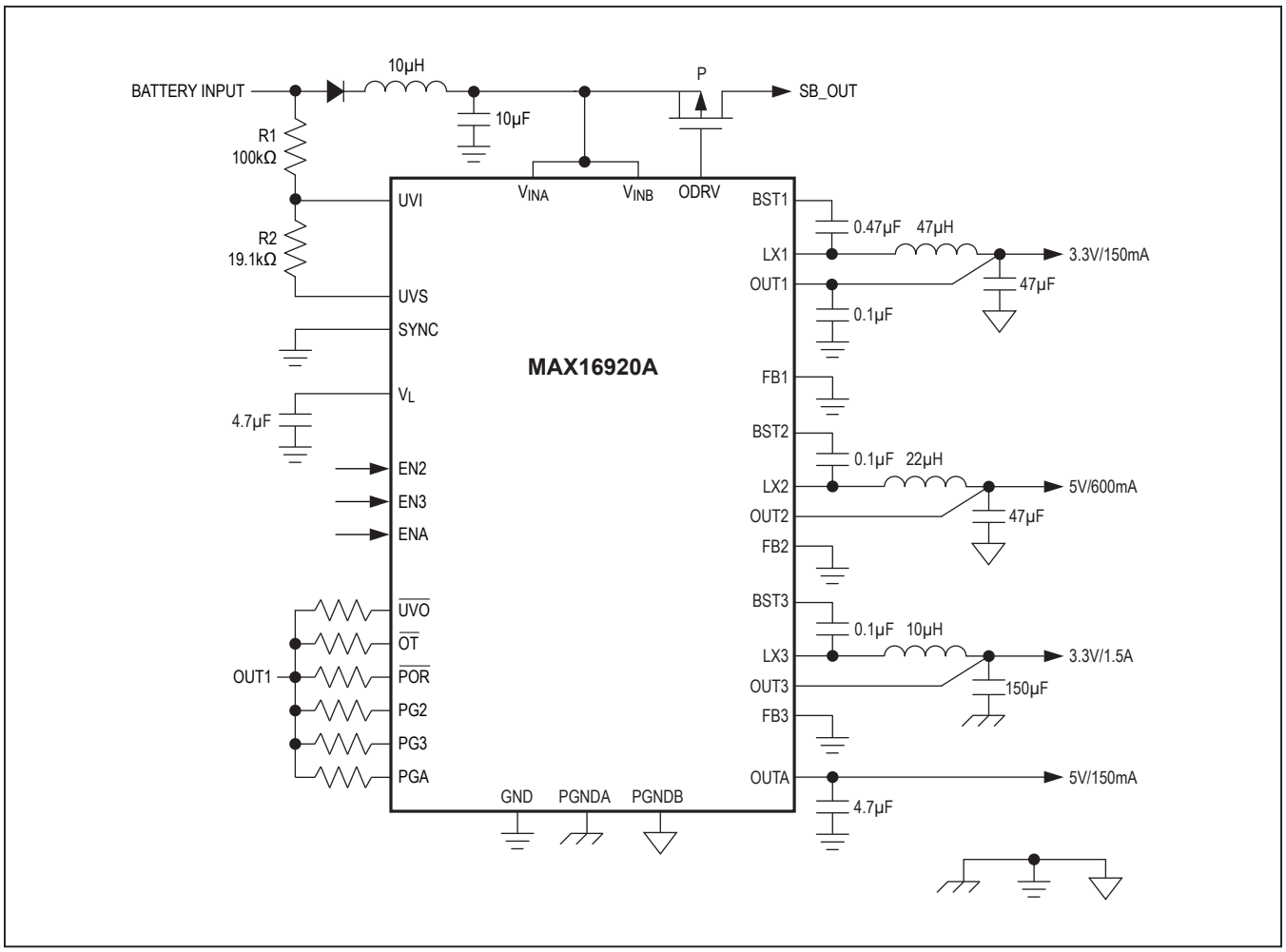


Figure 4. Typical Operating Circuit for MAX16920A Operating at 400kHz

Typical Operating Circuits (continued)

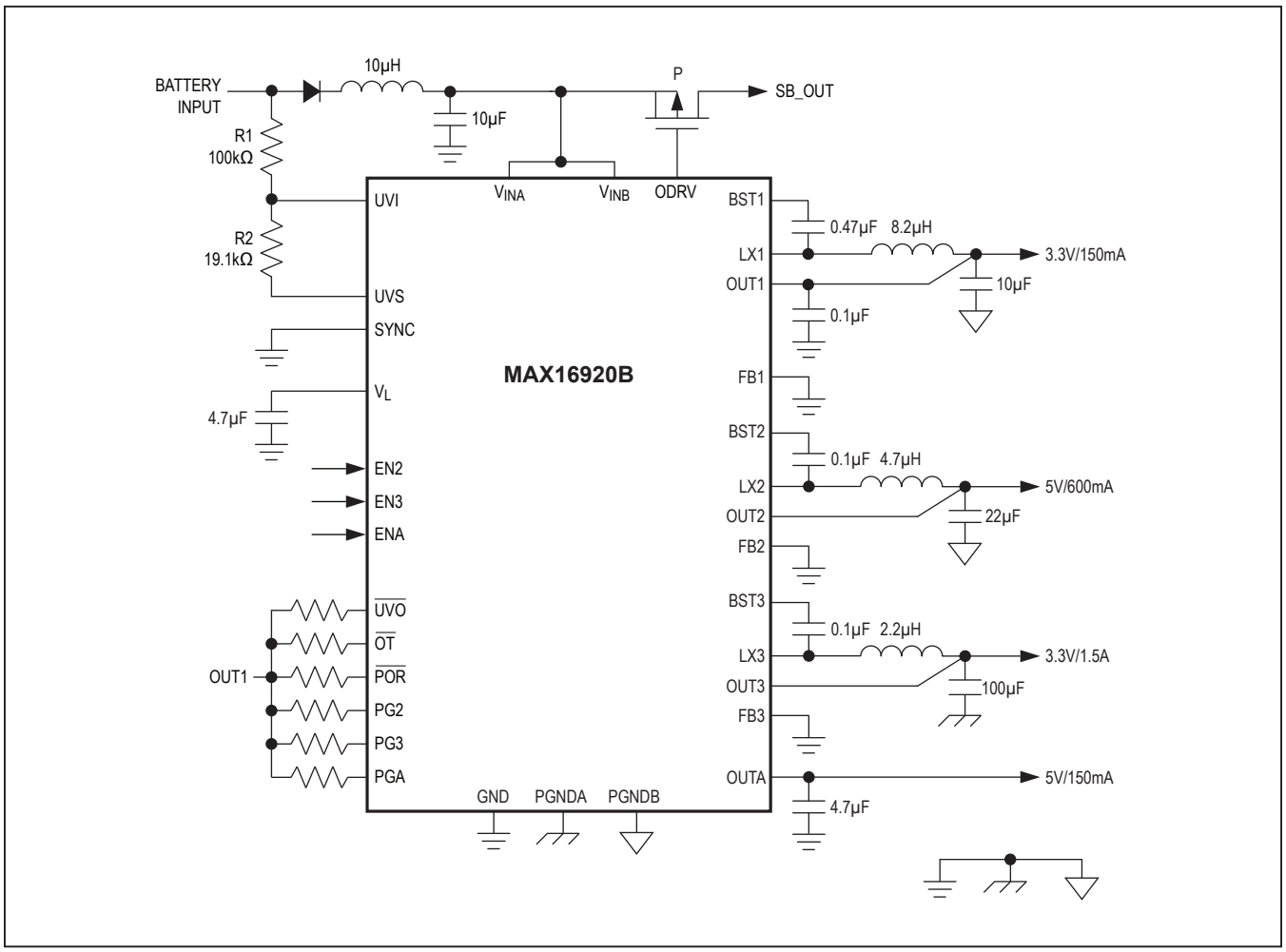


Figure 5. Typical Operating Circuit for MAX16920A Operating at 400kHz

Chip Information

PROCESS: BiCMOS

Package Information

For the latest package outline information and land patterns (footprints), go to **www.maximintegrated.com/packages**. Note that a "+", "#", or "-" in the package code indicates RoHS status only. Package drawings may show a different suffix character, but the drawing pertains to the package regardless of RoHS status.

PACKAGE TYPE	PACKAGE CODE	OUTLINE NO.	LAND PATTERN NO.
32 TQFN-EP	T3277+3	21-0144	90-0126

Revision History

REVISION NUMBER	REVISION DATE	DESCRIPTION	PAGES CHANGED
0	12/10	Initial release	—
1	8/11	Added the spread-spectrum option; updated the *Electrical Characteristics* table and added Note 4; included output voltage setting application instructions; added the *Spread-Spectrum Option* section; added new Figure 3 (*typical application circuit* for setting OUT1 or OUT3 above 3.3V)	1, 3, 4, 5, 8, 9, 11, 12, 13, 15, 16
2	2/19	Updated *Package Information*	19

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