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ABSOLUTE MAXIMUM RATINGS

Terminal Voltage (with respect GND)
- V_{CC} ..... -0.3V to +6.0V
- All Other Pins (Note 1)..... -0.3V to (V_{CC} + 0.3V)

Terminal Current (PFI, RESET IN, $\overline{MR}$)..... 10mA
Terminal Current (all other pins) 20mA
Continuous Power Dissipation (T_A = +25°C)
- Plastic DIP (derate 9.09mW/°C above +70°C) 727mW
- SO (derate 5.88mW/°C above +70°C)..... 471mW

Operating Temperature Ranges
- Commercial..... 0°C to +70°C
- Extended..... -40°C to +85C

Storage Temperature Range ..... -65°C to +125°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS, +5V Parts (MAX814/MAX815K, L, N)

(V_{CC} = 4.85V to 5.5V for MAX814K/MAX815K, V_{CC} = 4.75V to 5.5V for MAX814L/MAX815L, V_{CC} = 4.60V to 5.5V for MAX814N/MAX815N, T_A = T_{MIN} to T_{MAX}, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
Operating Voltage Range	V_{CC}	MAX814_C, MAX815_C		1.0		5.5	V
		MAX814_E, MAX815_E		1.2		5.5	
Supply Current	I_{SUPPLY}	MAX814_C, MAX815_C				75	µA
		MAX814_E, MAX815_E				85	
Reset Threshold	V_{RT}	MAX814K, MAX815K		4.75		4.85	V
		MAX814L, MAX815L		4.65		4.75	
		MAX814N, MAX815N		4.50		4.60	
Reset Threshold Hysteresis					0		mV
Reset Pulse Width	t_{RS}			140	200	250	ms
RESET Output Voltage	V_{OH}	MAX814	I_{SOURCE} = 800µA	V_{CC} -1.5			V
	V_{OL}		I_{SINK} = 3.2mA			0.4	
$\overline{RESET}$, $\overline{WDO}$, $\overline{PFO}$, $\overline{LOW\ LINE}$ Output Voltage	V_{OH}	I_{SOURCE} = 800µA		V_{CC} -1.5			V
	V_{OL}	I_{SINK} = 3.2mA				0.4	
		MAX814_C/MAX815_C, V_{CC} = 1.0V, I_{SINK} = 50µA				0.3	
		MAX814_E/MAX815_E, V_{CC} = 1.2V, I_{SINK} = 100µA				0.3	
Watchdog Timeout Period	t_{WD}	MAX815		1.12		2.00	s
WDI Pulse Width	t_{WP}	MAX815		50			ns
WDI Input Threshold	V_{WDI}	MAX815, V_{CC} = 5.0V	Low			0.8	V
			High	2.4			
WDI Input Current	I_{WDI}	WDI = V_{CC} or WDI = 0V		-1.0		1.0	µA
$\overline{MR}$ to $\overline{WDO}$ High Delay	t_{WDO}	MAX815 (Note 1)			1		µs
$\overline{LOW\ LINE}$ to $\overline{RESET}$ Differential Threshold	ΔV_{LL}	MAX814_C, V_{CC} falling		50		70	mV
		MAX814_E, V_{CC} falling		48		73	
$\overline{LOW\ LINE}$ Threshold	V_{LLT}	MAX814K, V_{CC} rising				4.93	V
		MAX814L, V_{CC} rising				4.83	
		MAX814N, V_{CC} rising				4.68	

ELECTRICAL CHARACTERISTICS, +5V Parts (MAX814/MAX815K, L, N) (continued)

(V_{CC} = 4.85V to 5.5V for MAX814K/MAX815K, V_{CC} = 4.75V to 5.5V for MAX814L/MAX815L, V_{CC} = 4.60V to 5.5V for MAX814N/MAX815N, T_A = T_{MIN} to T_{MAX}, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
$\overline{MR}$ Pull-Up Current	I_{MR}	$\overline{MR}$ = 0V	70		240	µA
$\overline{MR}$ Pulse Width	t_{MR}		150			ns
$\overline{MR}$ Input Threshold	$V_{\overline{MR}LO}$	Low			1.1	V
	$V_{\overline{MR}HI}$	High	0.7 x V_{CC}			
$\overline{MR}$ to $\overline{RESET}$ Out Delay	t_{MD}	(Note 3)			250	ns
PFI Input Threshold	V_{PFI}	V_{CC} = 5.0V	2.45	2.50	2.55	V
PFI Input Current	I_{PFI}		-15.00	+6.0	+35.00	nA
$\overline{LOW\ LINE}$, $\overline{PFO}$, $\overline{WDO}$ Assertion Delay		(Note 2)		200		µs

ELECTRICAL CHARACTERISTICS, +3V Parts (MAX814/MAX815T, MAX816)

(V_{CC} = 3.06V to 5.5V for MAX814T/MAX815T and MAX816, T_A = T_{MIN} to T_{MAX}, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
Operating Voltage Range	V_{CC}	0°C to +70°C		1.0		5.5	V
		-40°C to +85°C		1.2		5.5	
Supply Current	I_{SUPPLY}	0°C to +70°C				75	µA
		-40°C to +85°C				85	
Reset Threshold	V_{RT}	0°C to +70°C		3.00		3.06	V
		-40°C to +85°C		3.00		3.08	
RESET IN Threshold	V_{RIT}	MAX816C		1.683	1.700	1.717	V
		MAX816E		1.678	1.700	1.722	
RESET IN Input Current	I_{RT}	MAX816		-15	+6	+35	nA
Reset Threshold Hysteresis					0		mV
Reset Pulse Width	t_{RS}			140	200	250	ms
RESET Output Voltage	V_{OH}	V_{RT}(max) < V_{CC} < 3.6V; MAX814T, MAX816	I_{SOURCE} = 500µA	0.8 x V_{CC}			V
	V_{OL}		I_{SINK} = 1.2mA			0.3	
	V_{OH}	4.5V < V_{CC} < 5.5V; MAX814T, MAX816	I_{SOURCE} = 800µA	V_{CC} -1.5			
	V_{OL}		I_{SINK} = 3.2mA			0.4	
$\overline{RESET}$, $\overline{WDO}$, $\overline{PFO}$, $\overline{LOW\ LINE}$ Output Voltage	V_{OH}	V_{RT}(max) < V_{CC} < 3.6V	I_{SOURCE} = 500µA	0.8 x V_{CC}			V
	V_{OL}		I_{SINK} = 1.2mA			0.3	
	V_{OH}	4.5V < V_{CC} < 5.5V	I_{SOURCE} = 800µA	V_{CC} -1.5			
	V_{OL}		I_{SINK} = 3.2mA			0.4	
	V_{OL}	T_A = 0°C to +70°C, V_{CC} = 1.0V, I_{SINK} = 50µA				0.3	
		T_A = -40°C to +85°C, V_{CC} = 1.2V, I_{SINK} = 100µA				0.3	
Watchdog Timeout Period	t_{WD}	MAX815T		1.12		2.00	s

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ELECTRICAL CHARACTERISTICS, +3V Parts (MAX814/MAX815T, MAX816) (continued)

(V_{CC} = 3.06V to 5.5V for MAX814T/MAX815T and MAX816, T_A = T_{MIN} to T_{MAX}, unless otherwise noted.)

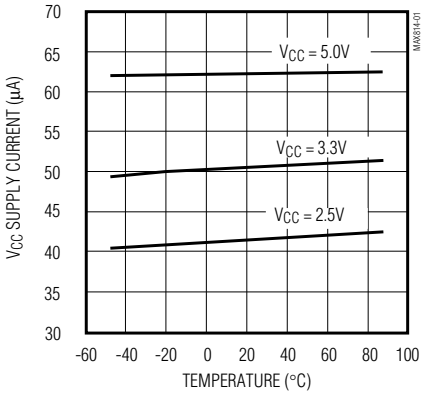
PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
$\overline{WDI}$ Pulse Width	t_{WP}	MAX815T	V_{RT}(max) < V_{CC} < 3.6V	100			ns
			4.5V < V_{CC} < 5.5V	50			
$\overline{WDI}$ Input Threshold	V_{WDI}	V_{RT}(max) < V_{CC} < 3.6V; MAX815T	Low			0.8	V
			High	0.7 x V_{CC}			
		V_{CC} = 5.0V; MAX815T	Low			0.8	
			High	2.4			
$\overline{WDI}$ Input Current	I_{WDI}	WDI = V_{CC} or 0V, MAX815T		-1.0		+1.0	µA
$\overline{MR}$ to $\overline{WDO}$ High Delay	t_{WDO}	MAX815T (Note 1)			1		µs
$\overline{LOW\ LINE}$ to $\overline{RESET}$ Differential Threshold	ΔV_{LL}	V_{CC} falling, MAX814TC		50		70	mV
		V_{CC} falling, MAX814TE		48		73	
$\overline{LOW\ LINE}$ Threshold	V_{LLT}	V_{CC} rising				3.163	V
$\overline{MR}$ Pullup Current	I_{MR}	$\overline{MR}$ = 0V	V_{RT}(max) < V_{CC}< 3.6V	70		240	µA
			4.5V < V_{CC} < 5.5V	110		370	
$\overline{MR}$ Pulse Width	t_{MR}	V_{RT}(max) < V_{CC} < 3.6V		500			ns
		4.5V < V_{CC} < 5.5V		150			
$\overline{MR}$ Input Threshold	$V_{\overline{MR}LO}$	Low				1.1	V
	$V_{\overline{MR}HI}$	High		0.7 x V_{CC}			
$\overline{MR}$ to $\overline{RESET}$ Out Delay (Note 3)	t_{MD}	V_{RT}(max) < V_{CC} < 3.6V				750	ns
		4.5V < V_{CC} < 5.5V				250	
PFI Input Threshold	V_{PFI}	V_{CC} = 3.3V, 5V		1.666	1.700	1.734	V
PFI Input Current	I_{PFI}			-15.00	+6.0	+35.00	nA

Note 1: Applies if $\overline{WDO}$ is externally connected to $\overline{MR}$ or if $\overline{MR}$ is externally driven.
Note 2: On power-up, delay from reset trip threshold crossing to valid outputs.
Note 3: Applies to both $\overline{RESET}$ and RESET.

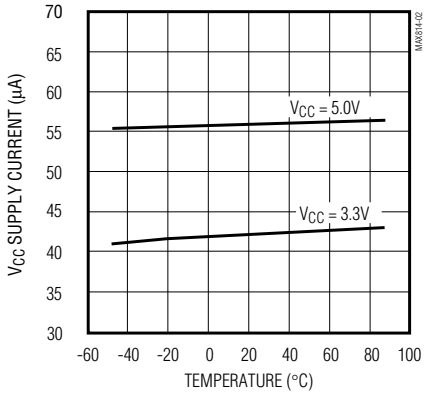
Typical Operating Characteristics

(T_A = +25°C, unless otherwise noted.)

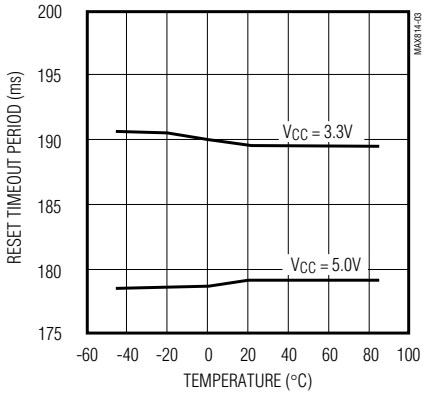
V_{CC} SUPPLY CURRENT vs. TEMPERATURE 3V PARTS (MAX814T/MAX815T, MAX816)



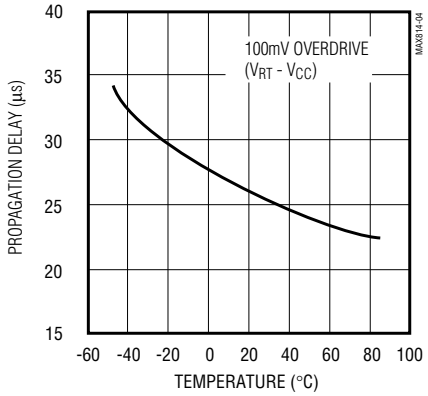
V_{CC} SUPPLY CURRENT vs. TEMPERATURE 5V PARTS (MAX814/MAX815K, L, N)



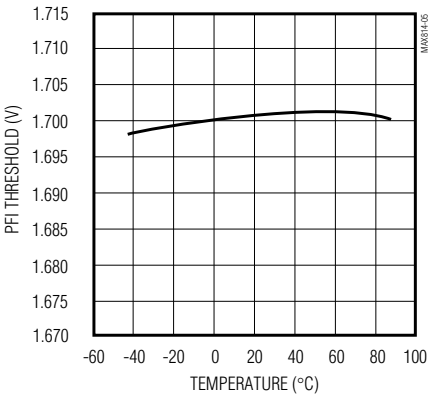
RESET TIMEOUT PERIOD vs. TEMPERATURE



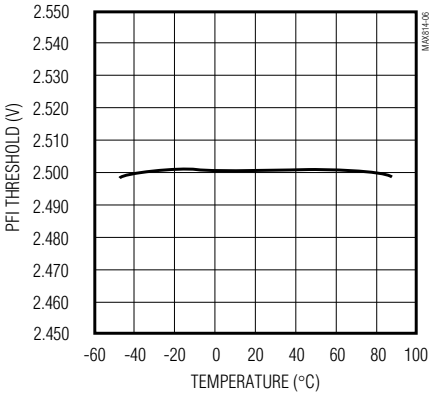
RESET-COMPARATOR PROPAGATION DELAY vs. TEMPERATURE



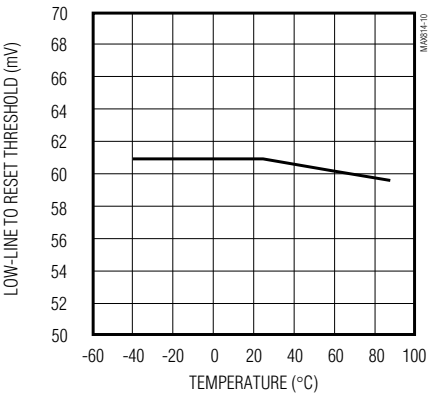
PFI THRESHOLD vs. TEMPERATURE 3V PARTS (MAX814T/MAX815T, MAX816)



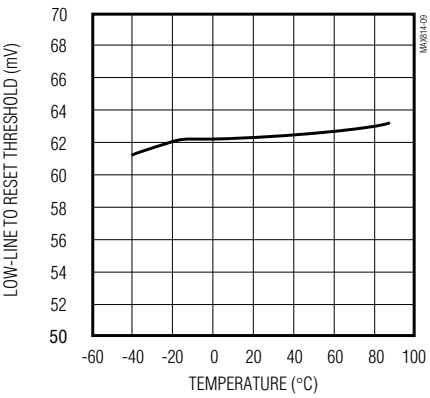
PFI THRESHOLD vs. TEMPERATURE 5V PARTS (MAX814/MAX815K, L, N)



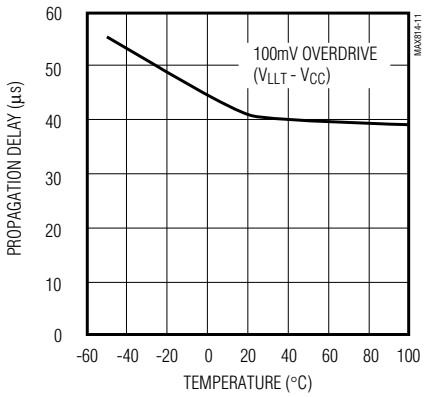
LOW-LINE TO RESET THRESHOLD vs. TEMPERATURE (V_{CC} RISING)



LOW-LINE TO RESET THRESHOLD vs. TEMPERATURE (V_{CC} FALLING)



LOW-LINE COMPARATOR PROPAGATION DELAY vs. TEMPERATURE



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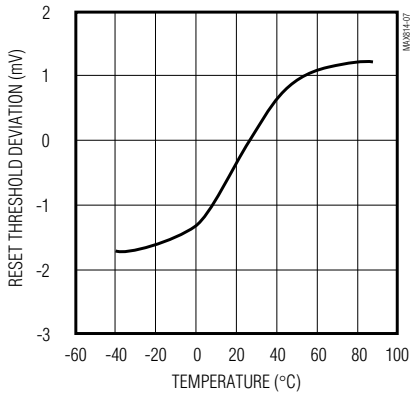
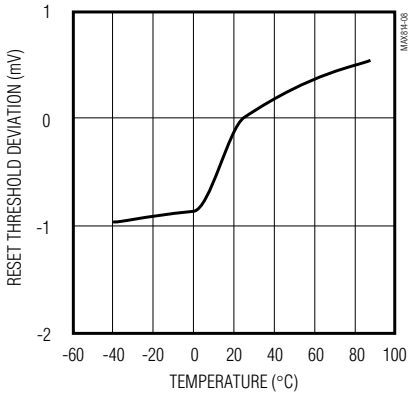
Typical Operating Characteristics (continued)

(T_A = +25°C, unless otherwise noted.)

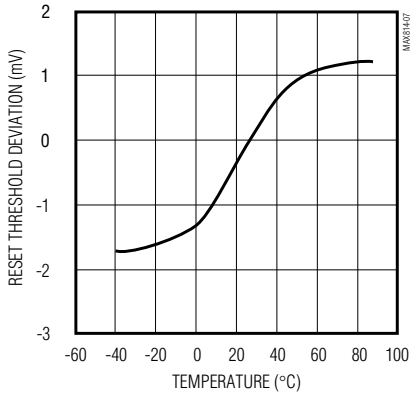
RESET THRESHOLD DEVIATION vs. TEMPERATURE 3V PARTS (MAX814T/MAX815T, MAX816)



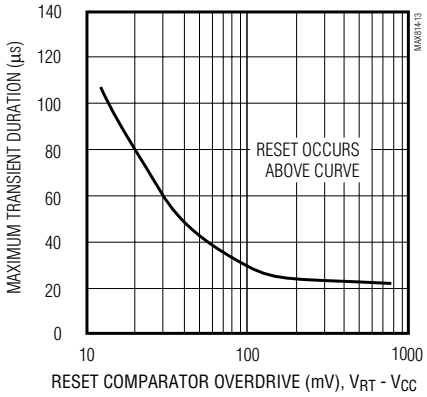
RESET THRESHOLD DEVIATION vs. TEMPERATURE 5V PARTS (MAX814/MAX815K, L, N)



RESET THRESHOLD DEVIATION vs. TEMPERATURE 3V PARTS (MAX814T/MAX815T, MAX816)



MAXIMUM TRANSIENT DURATION vs. RESET COMPARATOR OVERDRIVE 5V PARTS (MAX814/MAX815K, L, N)



Pin Description

PIN			NAME	FUNCTION
MAX814	MAX815	MAX816		
1	1	1	$\overline{MR}$	Manual-Reset Input. Triggers a reset when pulled below 1.10V. This active-low input has an internal 150µA pullup current to V_{CC}, and can be driven with CMOS logic or shorted to GND with a switch or transistor.
2	2	—	V_{CC}	Positive Power-Supply Input. When V_{CC} is below the reset threshold voltage*, $\overline{RESET}$ is low, and remains low for a minimum of 140ms after it rises above the threshold.
—	—	2		Positive Power-Supply Input. On the MAX816, $\overline{RESET}$ is controlled by RESET IN, not V_{CC}.
3	3	3	GND	Ground
4	4	4	PFI	Power-Fail Input. The PFI threshold voltage is 1.70V on the MAX816 and on MAX814/MAX815 parts with the T suffix. It is 2.50V on MAX814/MAX815 parts with K, L, and N suffixes. Connect PFI to GND or V_{CC} when not used.
5	5	5	$\overline{PFO}$	Power-Fail Output. When PFI is below its threshold, $\overline{PFO}$ is low; otherwise it is high.
—	6	—	WDI	Watchdog CMOS Input. If WDI remains high or low for more than 1.56s, the watchdog timer times out, and $\overline{WDO}$ goes low. The timer is reset to zero on each WDI transition.
6	—	—	$\overline{LOW\ LINE}$	Low-Line Output. Normally high, $\overline{LOW\ LINE}$ goes low when V_{CC} falls 60mV above the reset threshold. It returns high as soon as V_{CC} rises above the low-line threshold.
—	—	6	RESET IN	Reset Comparator Input. Reference is 1.70V. When RESET IN is below 1.70V, $\overline{RESET}$ is low, and remains low for a minimum of 140ms after it rises above the reference.
7	7	7	$\overline{RESET}$	Reset Output. Normally high, active low. Controlled by $\overline{MR}$ and reset comparator.
—	8	—	$\overline{WDO}$	Watchdog Output. Normally high, $\overline{WDO}$ goes low whenever the V_{CC} reset threshold comparator input voltage is low or when the watchdog timer times out. There is no appreciable delay going either direction when the V_{CC} threshold comparator toggles.
8	—	8	RESET	Reset Output. Active high. The inverse of $\overline{RESET}$.

*Reset Threshold Voltage is determined by part number suffix: K = 4.80V, L = 4.70V, N = 4.55V, T = 3.03V.

Detailed Description

The MAX814/MAX815/MAX816 are high-accuracy, low-power microprocessor (µP) supervisory circuits. They have µP-reset, watchdog-timer, and power-fail functions. Typical applications illustrating their similarities and differences are shown in Figures 1, 2, and 3. Figures 4, 5, and 6 show the block diagrams of these parts.

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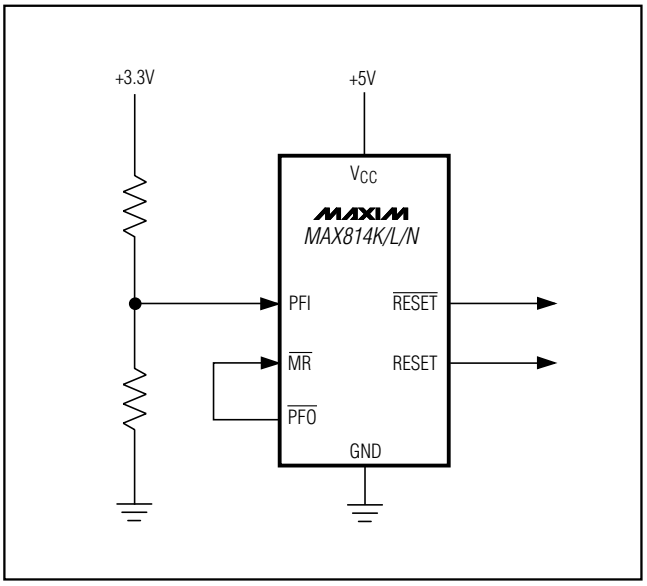

Figure 1a. Typical Application for Dual +3.3V and +5V Systems

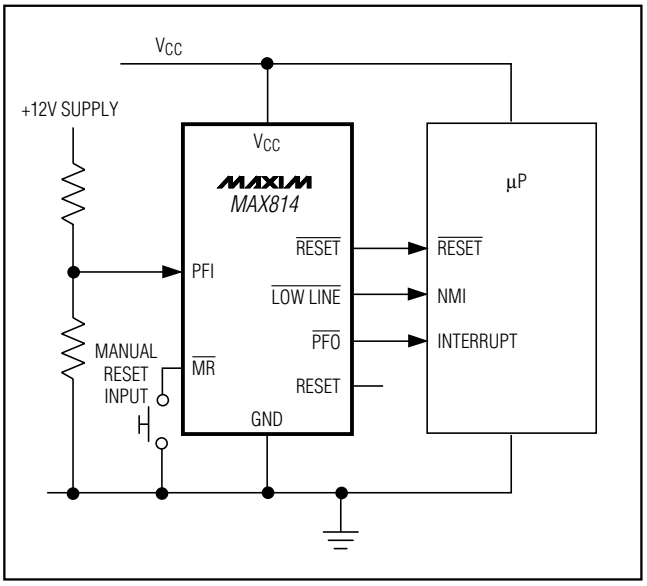

Figure 1b. MAX814 Typical Application

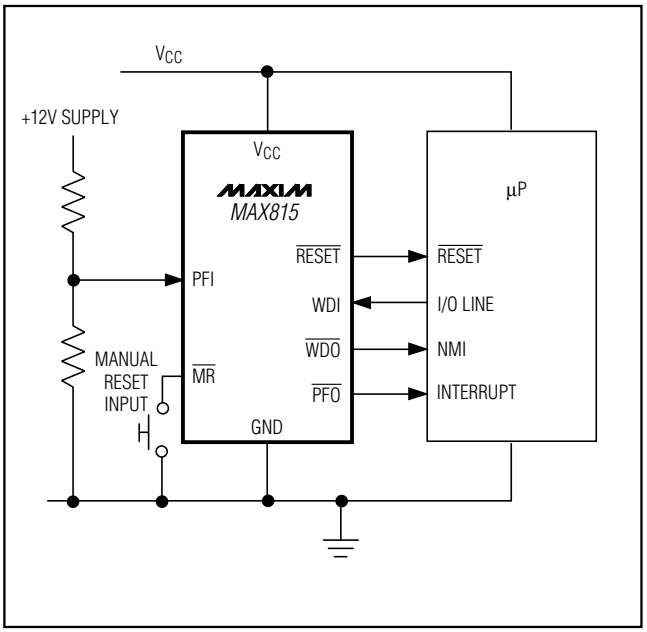

Figure 2. MAX815 Typical Application

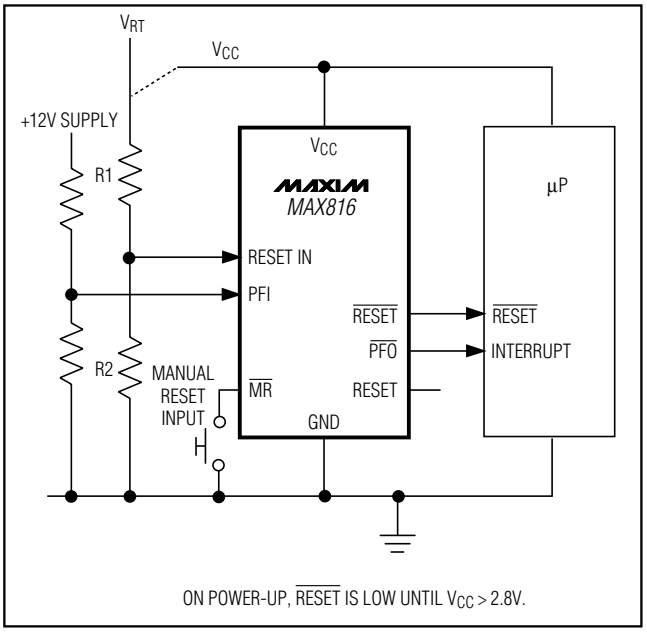

Figure 3. MAX816 Typical Application

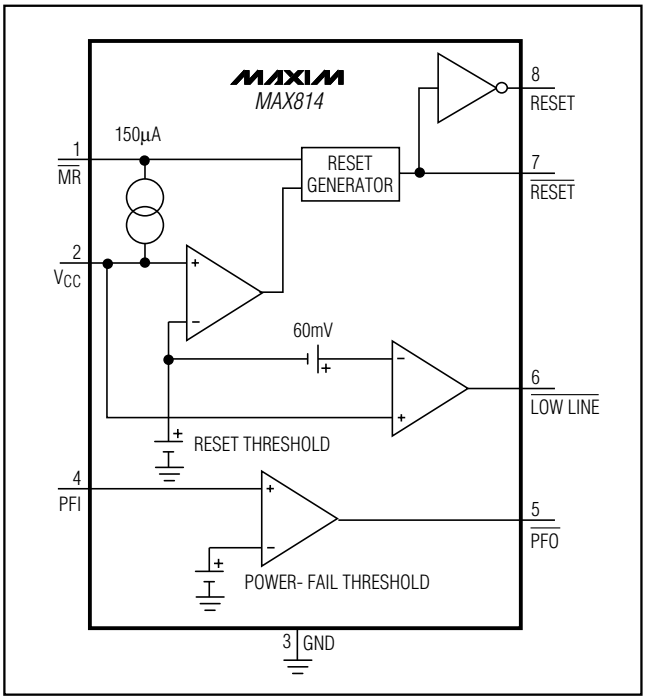

Figure 4. MAX814 Block Diagram

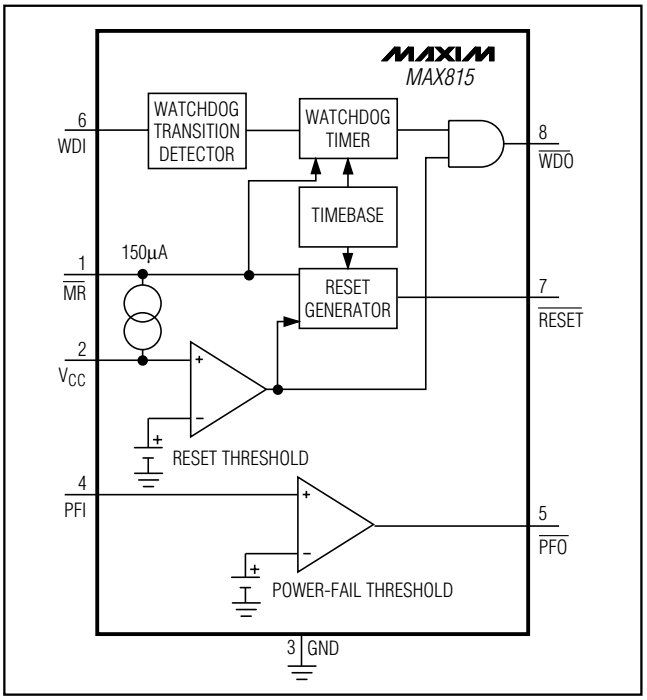

Figure 5. MAX815 Block Diagram

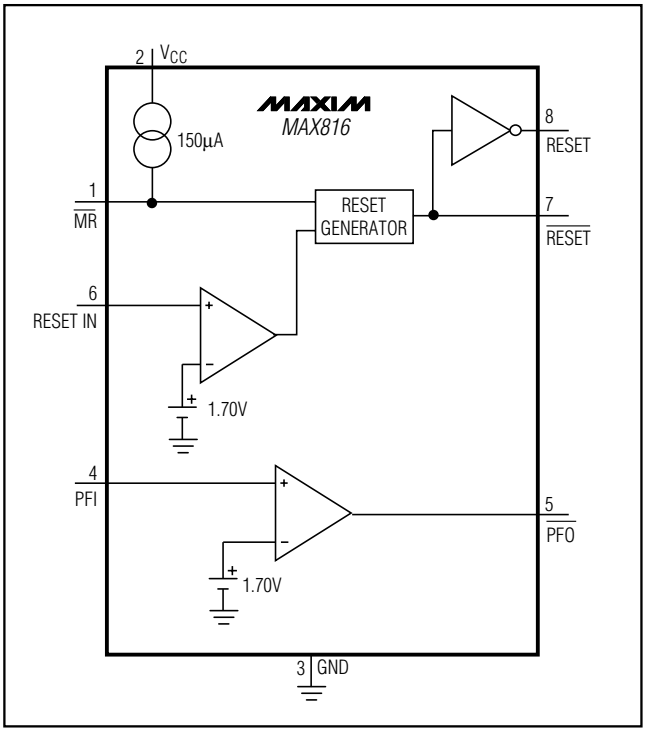

Figure 6. MAX816 Block Diagram

Reset Output

A µP's reset input starts the µP in a known state. Whenever the µP is in an unknown state, it should be held in reset. The MAX814/MAX815/MAX816 assert reset during power-up, power-down, or brownout conditions.

On power-up, once V_{CC} reaches 1V, $\overline{RESET}$ is a guaranteed logic low of 0.4V or less. As V_{CC} rises, $\overline{RESET}$ stays low. As V_{CC} rises above the reset threshold, an internal timer releases $\overline{RESET}$ after 200ms. $\overline{RESET}$ also pulses low whenever V_{CC} dips below the reset threshold (i.e., brownout condition). If brownout occurs in the middle of a previously initiated reset, the internal timer is reset and the output remains low for at least another 140ms after the brownout ends. On power-down, once V_{CC} falls below the reset threshold, $\overline{RESET}$ stays low and is guaranteed to be less than 0.3V until V_{CC} drops below 1V.

The MAX814 and MAX816 also offer active-high RESET outputs. They are the inverse of the $\overline{RESET}$ outputs.

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Reset Threshold

The MAX814/MAX815 have fixed, factory-set reset thresholds, signified by the first suffix letter in the part number (see Figure 7 for more information on reset ranges). The MAX816 has an adjustable reset threshold.

MAX814/MAX815 K-suffix parts have a minimum reset threshold set to 4.75V, worst case. They are intended for 5.0V systems with a ±4% or better power-supply tolerance design that must meet worst-case system parameters over time, temperature, line, and load variations. Typically, the reset threshold (V_{RT}) is greater than or equal to the minimum IC operating voltage (V_{ICMIN}). The "K" series 1%-tolerance reset threshold allows a larger range of power-supply tolerance. System ICs that have a tight operating supply range, like the 386/486 µPs, need a RESET initiated at a minimum threshold of 4.75V, worst case.

L-suffix parts have a minimum reset threshold set to 4.65V, worst case. They are intended for 5.0V systems with a ±5% power-supply tolerance. Typically, the reset threshold is less than or equal to the minimum power-supply voltage, allowing system operation over the complete power-supply range. A reset is initiated at 4.75V maximum. The 1% "L" version maximizes the System IC Guard-Band Range.

N-suffix parts have a minimum reset threshold set to 4.50V, worst case. They are intended for 5.0V systems with a ±10% IC system. Typically, the reset threshold

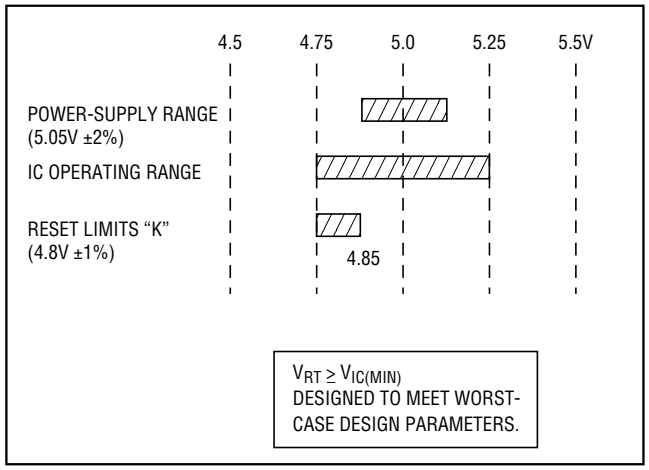

Figure 7a. K Suffix Design Range

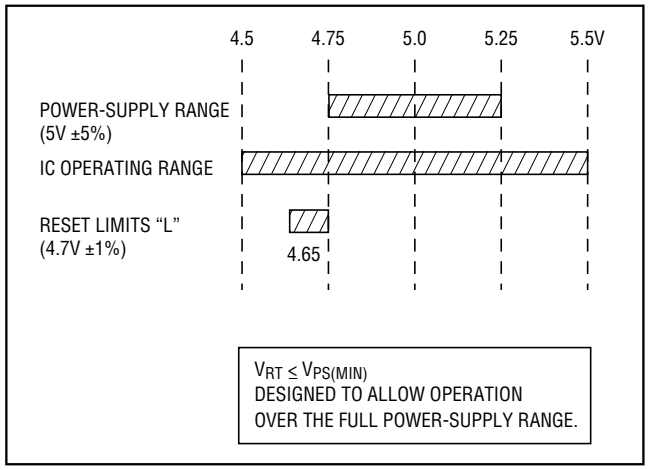

Figure 7b. L Suffix Design Range

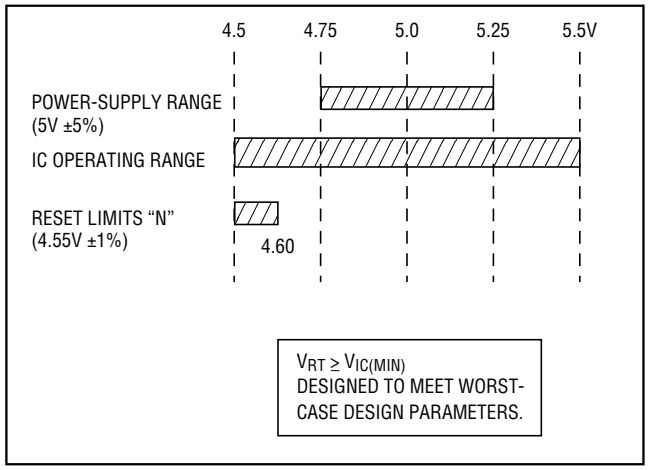

Figure 7c. N Suffix Design Range

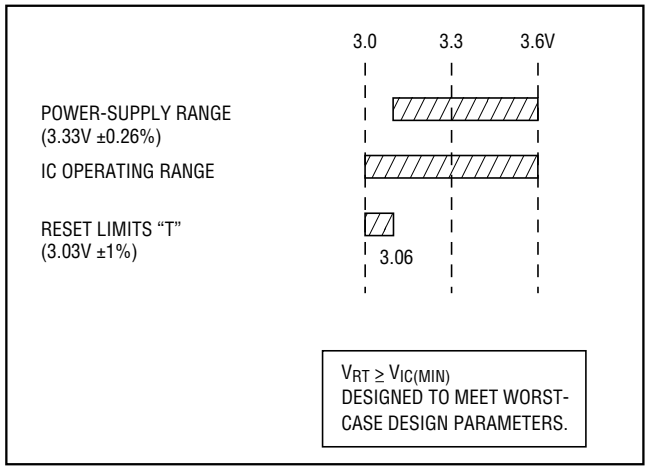

Figure 7d. T Suffix Design Range

(V_{RT}) is greater than or equal to the minimum IC operating voltages (V_{ICMIN}). The 1% "L" series allows the use of a 5V ±5% power supply, and guarantees system operation over worst-case conditions, maximizing the Power-Supply Guard-Band Range.

T-suffix parts have a minimum reset threshold set to 3.00V, worst case. They are intended for 3.3V systems (3.33V ±0.26V) with a 7.8% or better power-supply tolerance. Typically, the reset threshold (V_{RT}) is greater than or equal to the minimum IC operating voltages (V_{ICMIN}).

The MAX816 has an adjustable reset threshold, set with an external resistive divider (Figure 3). The voltage on the RESET IN pin is monitored, not the voltage on V_{CC}. The RESET IN threshold is 1.700V, and has very high impedance and 35nA maximum leakage. Calculate the trip point, V_{RT}, as follows:

$$V_{RT} = \frac{V_{RIT} \times (R1 + R2)}{R2}$$

where V_{RT} = the desired reset threshold, V_{RIT} is the RESET IN threshold (1.700V), R1 is the resistor connected between V_{RT} and RESET IN, and R2 is the resistor connected between RESET IN and GND.

Resistors R1 and R2 can have very high values. The usual procedure is to set R2 to some conveniently high value (100kΩ, for example) and calculate R1 based on the desired reset threshold, using the following formula:

$$R1 = R2 \times \left[\left(V_{RT} / V_{RIT} \right) - 1 \right]$$

The MAX816 can achieve ±1.2% accuracy with 0.1% resistors.

Watchdog Timer (MAX815)

The watchdog circuit monitors the µP's activity. If the µP does not toggle the watchdog input (WDI) within the watchdog timeout period (t_{WP}), $\overline{WDO}$ goes low (Figure 8). $\overline{WDO}$ also goes low during reset conditions. Whenever V_{CC} is below the reset threshold, $\overline{WDO}$ stays low; however, unlike $\overline{RESET}$, $\overline{WDO}$ does not have a minimum pulse width. As soon as V_{CC} rises above the reset threshold, $\overline{WDO}$ goes high with no delay (Figure 9).

Typically, $\overline{WDO}$ is connected to the non-maskable interrupt (NMI) of a µP. When V_{CC} drops below the reset threshold, $\overline{WDO}$ goes low whether or not the watchdog timer has timed out (Figure 9). This would normally trigger an NMI interrupt, but $\overline{RESET}$ goes low simultaneously and thus overrides the NMI interrupt.

Connecting $\overline{WDO}$ to $\overline{MR}$ enables the watchdog timeout to generate a reset in the MAX815.

Early Power-Fail Warning

Critical systems often require early warning to indicate when power is failing. This warning provides time for the µP to store vital data and take care of any additional "housekeeping" before the power supply gets too far out of tolerance for the µP to operate reliably.

Power-Fail Comparator

The power-fail comparator is intended as an undervoltage detector to signal a failing power supply. However, the comparator does not need to be dedicated to this function, because it is completely separate from the rest of the circuitry. To build an early-warning circuit for power failure, connect the PFI pin to a voltage divider (see Figures 1, 2, and 3). Choose the voltage divider ratio, so the voltage at PFI falls below V_{PFI} just before the monitored voltage drops out. Use $\overline{PFO}$ to interrupt the µP, so it can prepare for an orderly power-down.

The power-fail input (PFI) is compared to an internal reference. If the voltage on PFI is less than the power-fail reference, $\overline{PFO}$ sinks at least 1.2mA to GND; otherwise it sources at least 300µA from V_{CC}. The reference is 2.50V in the MAX814/MAX815 with K, L, N suffixes, or 1.70V with the T suffix. It is also 1.70V in the MAX816.

$\overline{LOW\ LINE}$ Output (MAX814)

The low-line detector is a separate comparator that monitors V_{CC} with a typical threshold voltage of 60mV above the normal reset threshold, with 2mV of hysteresis (Figure 9). If V_{CC} rises faster than 10µs/V, insert a 100pF capacitor from $\overline{LOW\ LINE}$ to GND to ensure proper start-up. For normal operation (V_{CC} above the reset threshold), $\overline{LOW\ LINE}$ is pulled to V_{CC}. Use $\overline{LOW\ LINE}$ to provide an NMI to the µP when power begins to fall. In most battery-operated portable systems, reserve energy in the battery provides ample time to complete the shutdown routine once the low-line warning is encountered, and before reset asserts. If the system must also contend with a more rapid V_{CC} fall time—such as when the main battery is disconnected or a high-side switch is opened during operation—use capacitance on the V_{CC} line to provide time to execute the shutdown routine. First, calculate the worst-case time required for the system to perform its shutdown routine. Then use the worst-case shutdown time (t_{SHDN}), worst-case load current (I_{LOAD}), and minimum low-line to reset threshold (V_{LR}) to calculate the amount of capacitance required to allow the shutdown routine to complete before reset is asserted.

$$C_{HOLD} = \frac{I_{LOAD} \times t_{SHDN}}{V_{LR}}$$

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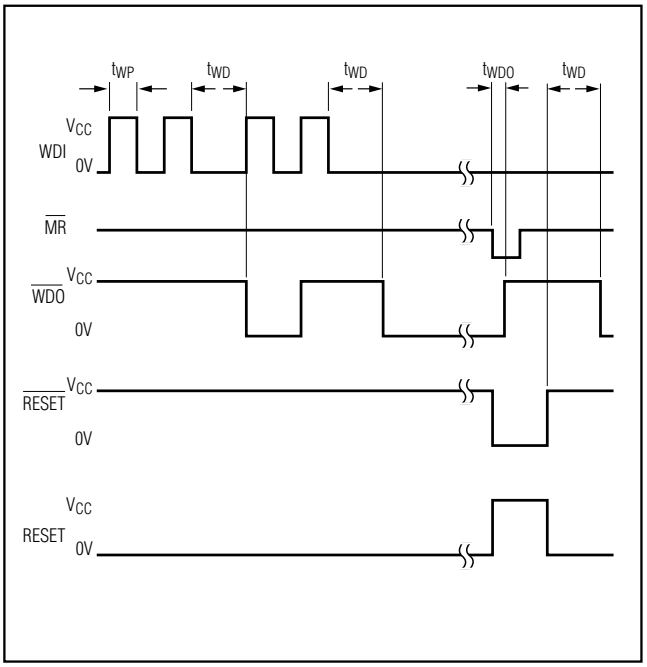


Figure 8. MAX815 Watchdog Timing

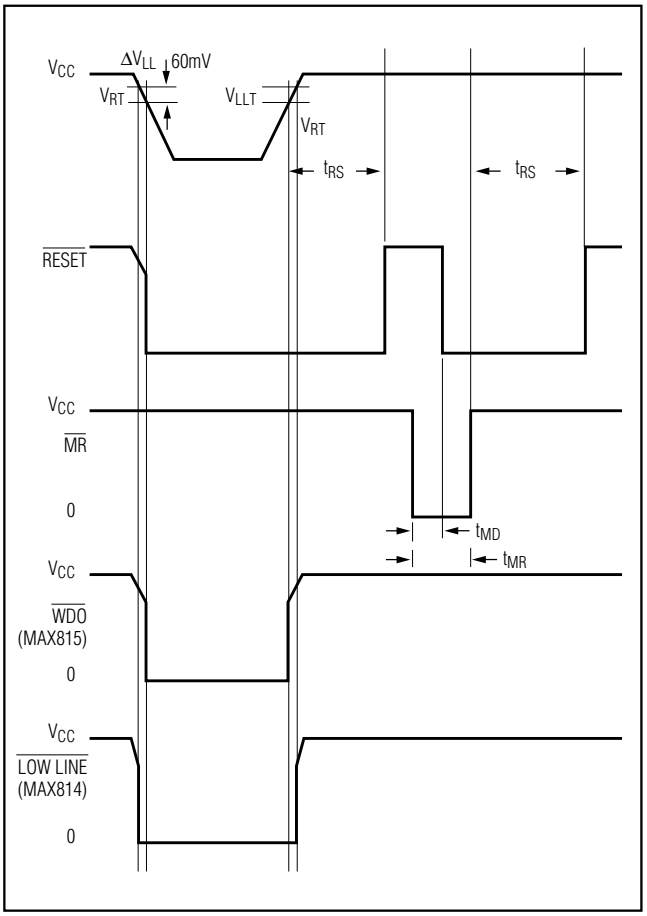


Figure 9. Timing Diagram

where C_{HOLD} is the capacitance (in Farads), I_{LOAD} is the current being drained from the capacitor (in Amperes), and V_{LR} is the low-line to reset threshold difference (in Volts).

Manual Reset

Many µP-based products require manual-reset capability, allowing the operator, a test technician, or external logic circuitry to initiate a reset. A logic low on $\overline{MR}$ asserts reset. Reset remains asserted while $\overline{MR}$ is low, and for t_{RS} (200ms) after $\overline{MR}$ returns high. This input has an internal pullup resistor, so it can be left open if not used. $\overline{MR}$ can be driven with TTL/CMOS-logic levels or with open-drain/collector outputs.

Connect a normally open momentary switch from $\overline{MR}$ to GND to create a manual-reset function; external debounce circuitry is not required.

The watchdog circuit can be used to force a reset in the MAX815 by connecting $\overline{WDO}$ to $\overline{MR}$. If $\overline{MR}$ is driven from long cables, or the device is used in a noisy environment, connect a 0.1µF capacitor to ground to provide additional noise immunity.

Applications Information

Low-Voltage Operation

The $\overline{LOW\ LINE}$, $\overline{PFO}$, and $\overline{WDO}$ outputs will be locked to logic low when the power supply drops below the lockout threshold (typically 1V below the reset threshold).

Ensuring a Valid $\overline{RESET}$ Output Down to V_{CC} = 0V

When V_{CC} falls below 1V, the $\overline{RESET}$ output no longer sinks current, but becomes an open circuit. High-impedance CMOS-logic inputs can drift to undetermined voltages if left undriven. If a pulldown resistor is added to the $\overline{RESET}$ pin as shown in Figure 10, any stray charge or leakage currents will be drained to ground, holding $\overline{RESET}$ low. Resistor value R1 is not critical. It should be about 100kΩ—large enough not to load $\overline{RESET}$, and small enough to pull $\overline{RESET}$ to ground.

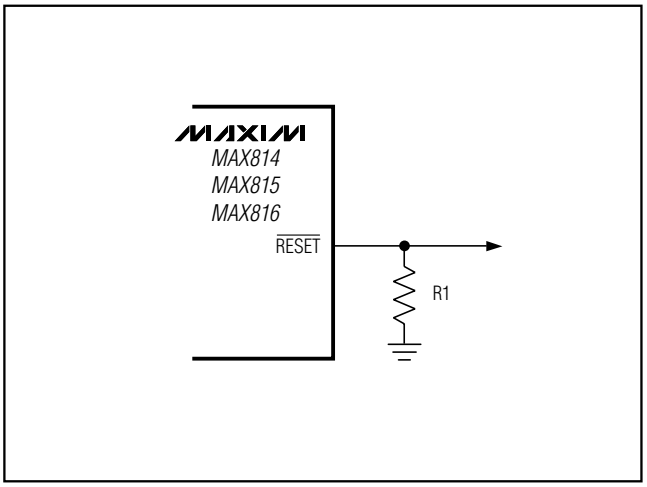
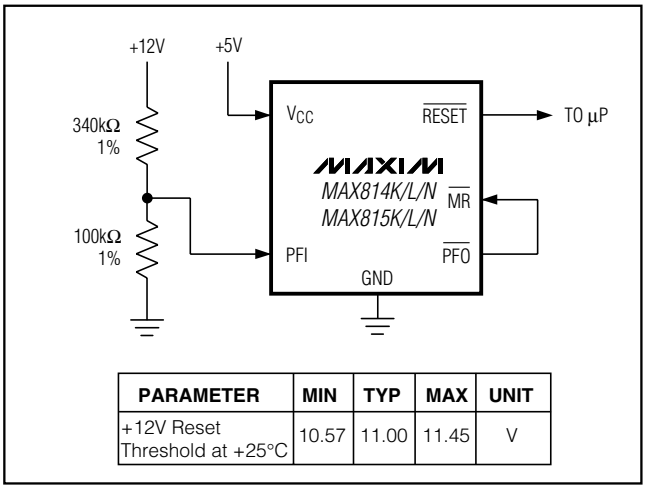


Figure 10. $\overline{RESET}$ Valid to Ground Circuit



PARAMETER	MIN	TYP	MAX	UNIT
+12V Reset Threshold at +25°C	10.57	11.00	11.45	V

Figure 11. Monitoring Both +5V and +12V

Monitoring Voltages Other than V_{CC}

Monitor voltages other than the V_{CC} by connecting a voltage divider to PFI and adjusting the ratio appropriately. If required, add hysteresis by connecting a resistor (with a value approximately 10-times the sum of the two resistors in the potential divider network) between PFI and $\overline{PFO}$. A capacitor between PFI and GND will reduce the power-fail circuit's sensitivity to high-frequency noise on the line being monitored. $\overline{RESET}$ can be asserted on other voltages in addition to the +5V V_{CC} line. Connect $\overline{PFO}$ to $\overline{MR}$ to initiate a reset when PFI drops below 2.50V (K, L, N suffix) or 1.70V (T suffix or MAX816). Figure 11 shows the MAX814K/L/N/MAX815K/L/N configured to assert $\overline{RESET}$ when the +5V supply falls below the reset threshold, or when the +12V supply falls below approximately 11V.

Monitoring a Negative Voltage

The power-fail comparator can also monitor a negative supply rail (Figure 12). When the negative rail is good (a negative voltage of large magnitude), $\overline{PFO}$ is low. When the negative rail is degraded (a negative voltage of lesser magnitude), $\overline{PFO}$ is high. By adding the resistors and transistor as shown, a high $\overline{PFO}$ triggers reset. As long as $\overline{PFO}$ remains high, the MAX814/MAX815/MAX816 will keep reset asserted ($\overline{RESET}$ = low, RESET = high). Note that this circuit's accuracy depends on the PFI threshold tolerance, the V_{CC} line, and the resistor.

Watchdog Software Considerations

A way to help the watchdog timer keep closer tabs on software execution involves setting and resetting the watchdog input at different points in the program, rather than pulsing the watchdog input high-low-high or low-high-low. This technique avoids a stuck loop where the watchdog timer continues to be reset within the loop, keeping the watchdog from timing out. Figure 13 shows an example flow diagram where the I/O driving the watchdog input is set low at the beginning of the program, set high at the beginning of every subroutine, then set low at the end of every subroutine. If the program should hang in any subroutine, the I/O is continually set high and the watchdog timer is allowed to time out, causing a reset to be issued.

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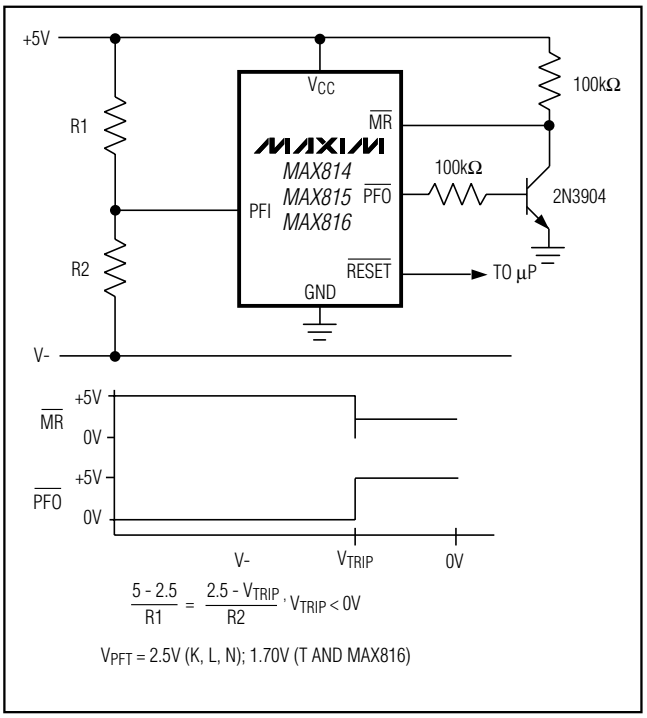


Figure 12. Monitoring a Negative Voltage

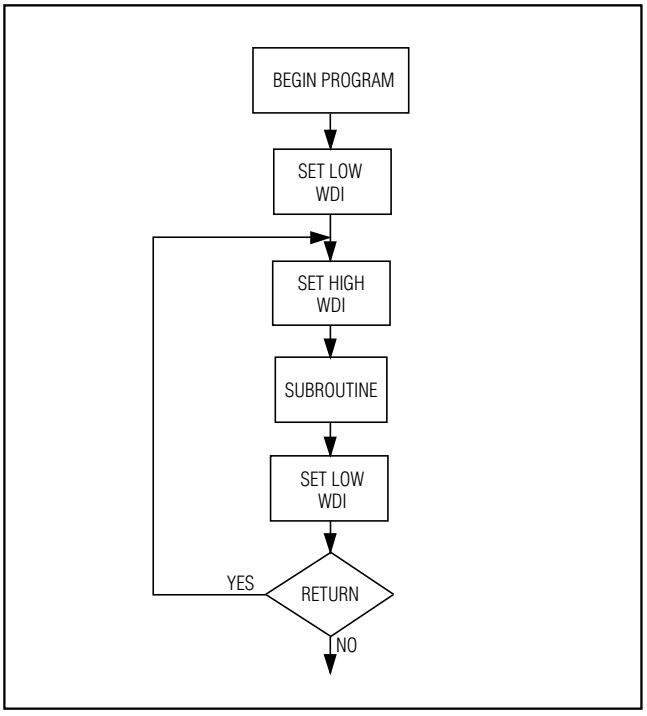


Figure 13. Flow Chart of WDI Implementation

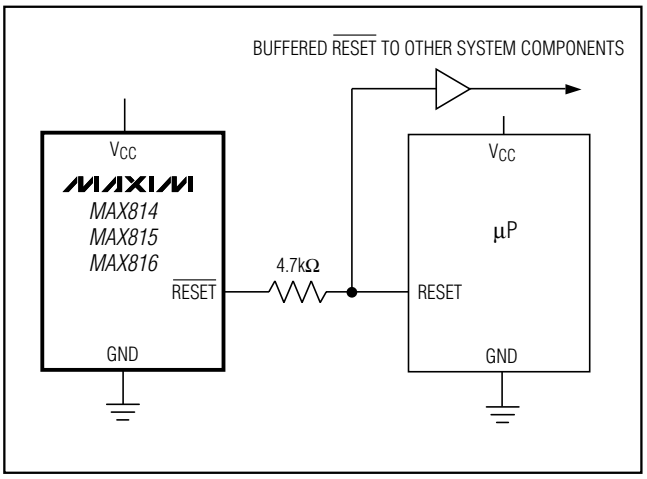


Figure 14. Interfacing to µPs with Bidirectional Reset I/O

Negative-Going V_{CC} Transients

In addition to issuing a reset to the µP during power-up, power-down, and brownout conditions, the MAX814/MAX815/MAX816 series is relatively immune to short duration negative-going V_{CC} transients (glitches). The *Typical Operating Characteristics* show a graph of Maximum Transient Duration vs. Reset Comparator Overdrive, for which a reset is not generated. The graph was made using a negative-going pulse applied to V_{CC}, starting 1.5V above the actual reset threshold and ending below it by the magnitude indicated (reset comparator overdrive). The graph indicates the typical maximum pulse width a negative-going V_{CC} transient may have without causing a reset pulse. As the magnitude of the transient increases (goes further below the reset threshold), the maximum allowable pulse width decreases. Typically, a V_{CC} that goes 100mV below the reset threshold and lasts 30µs or less will not cause a reset pulse to be issued.

A 0.1µF bypass capacitor mounted as close as possible to pin 2 (V_{CC}) provides additional transient immunity.

Interfacing to µPs with Bidirectional Reset Pins

µPs with bidirectional reset pins, such as the Motorola 68HC11 series, can cause a conflict with the $\overline{RESET}$ output. If, for example, the $\overline{RESET}$ output is driven high and the µP wants to pull it low, indeterminate logic levels may result. To correct this, connect a 4.7kΩ resistor between the $\overline{RESET}$ output and the µP reset I/O, as in Figure 14. Buffer the $\overline{RESET}$ output to other system components.

Ordering Information

PART*	TEMP. RANGE	PIN-PACKAGE
MAX814_CPA	0°C to +70°C	8 Plastic DIP
MAX814_CSA	0°C to +70°C	8 SO
MAX814_EPA	-40°C to +85°C	8 Plastic DIP
MAX814_ESA	-40°C to +85°C	8 SO
MAX815_CPA	0°C to +70°C	8 Plastic DIP
MAX815_CSA	0°C to +70°C	8 SO
MAX815_EPA	-40°C to +85°C	8 Plastic DIP
MAX815_ESA	-40°C to +85°C	8 SO
MAX816CPA	0°C to +70°C	8 Plastic DIP
MAX816CSA	0°C to +70°C	8 SO
MAX816EPA	-40°C to +85°C	8 Plastic DIP
MAX816ESA	-40°C to +85°C	8 SO

**The MAX814/MAX815 offer a choice of reset threshold voltage. From the Reset Trip Threshold table, select the suffix corresponding to the desired threshold and insert it into the blank to complete the part number.*

Devices are available in both leaded and lead-free packaging. Specify lead free by adding the + symbol at the end of the part number when ordering.

Reset Trip Thresholds

MAX814/MAX815		
SUFFIX	**RESET TRIP THRESHOLD**	
	MIN (V)	**MAX (V)**
K	4.75	4.85
L	4.65	4.75
N	4.50	4.60
T	3.00	3.06
MAX816		
—	Adjustable	

Chip Information

TRANSISTOR COUNT: 744

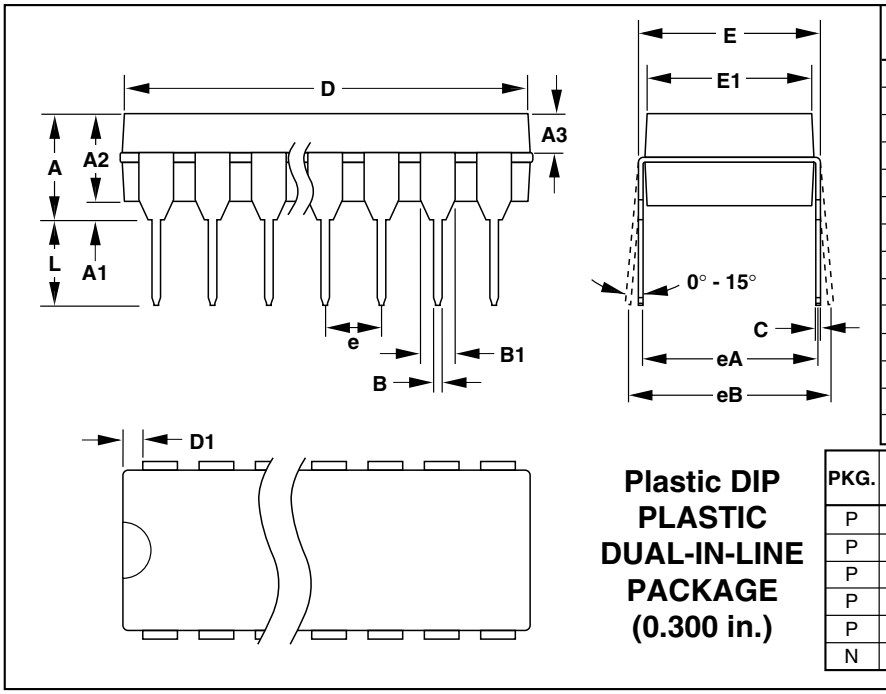
Revision History

Pages changed at Rev 1: 1–4, 12-16.

±1% Accuracy, Low-Power, +3V and +5V µP Supervisory Circuits

Package Information

(The package drawing(s) in this data sheet may not reflect the most current specifications. For the latest package outline information, go to **www.maxim-ic.com/packages**.)



Plastic DIP PLASTIC DUAL-IN-LINE PACKAGE (0.300 in.)

DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	–	0.200	–	5.08
A1	0.015	–	0.38	–
A2	0.125	0.175	3.18	4.45
A3	0.055	0.080	1.40	2.03
B	0.016	0.022	0.41	0.56
B1	0.045	0.065	1.14	1.65
C	0.008	0.012	0.20	0.30
D1	0.005	0.080	0.13	2.03
E	0.300	0.325	7.62	8.26
E1	0.240	0.310	6.10	7.87
e	0.100	–	2.54	–
eA	0.300	–	7.62	–
eB	–	0.400	–	10.16
L	0.115	0.150	2.92	3.81

PKG.	DIM	PINS	INCHES		MILLIMETERS	
			MIN	MAX	MIN	MAX
P	D	8	0.348	0.390	8.84	9.91
P	D	14	0.735	0.765	18.67	19.43
P	D	16	0.745	0.765	18.92	19.43
P	D	18	0.885	0.915	22.48	23.24
P	D	20	1.015	1.045	25.78	26.54
N	D	24	1.14	1.265	28.96	32.13

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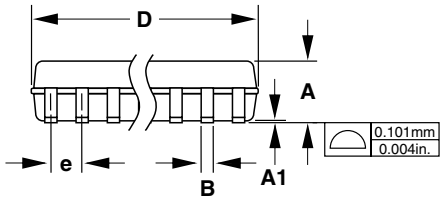

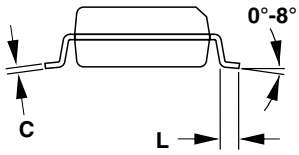

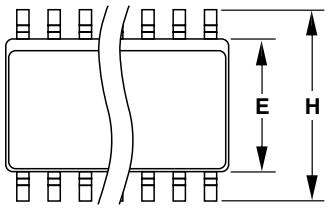

Narrow SO SMALL-OUTLINE PACKAGE (0.150 in.)

DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.053	0.069	1.35	1.75
A1	0.004	0.010	0.10	0.25
B	0.014	0.019	0.35	0.49
C	0.007	0.010	0.19	0.25
E	0.150	0.157	3.80	4.00
e	0.050		1.27	
H	0.228	0.244	5.80	6.20
L	0.016	0.050	0.40	1.27

DIM	PINS	INCHES		MILLIMETERS	
		MIN	MAX	MIN	MAX
D	8	0.189	0.197	4.80	5.00
D	14	0.337	0.344	8.55	8.75
D	16	0.386	0.394	9.80	10.00

21-0041A

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