Absolute Maximum Ratings

(All pins referenced to GND, unless otherwise noted.)
V_{CC} ....-0.3V to +80V
EN, $\overline{EN}$, LOGIC .... -0.3V to (V_{CC} + 0.3V)
INA+, INB-, IN+, IN-, REF, SET............................-0.3V to +12V
OUTA, OUTB, OUT ....-0.3V to +80V
GATE1, GATE2 to V_{CC} ....-12V to +0.3V
GATE1, GATE2 ....-0.3V to (VCC + 0.3V)
Current Sink/Source (all pins) 50mA

Continuous Power Dissipation (T_A = +70°C)
6-Pin TDFN (derate 18.2mW/°C above +70°C) 1455mW
8-Pin TDFN (derate 18.2mW/°C above +70°C) 1455mW
Operating Temperature Range......................... -40°C to +125°C
Maximum Junction Temperature ....+150°C
Storage Temperature Range........................... -60°C to +150°C
Lead Temperature (soldering, 10s) ....+300°C

Stresses beyond those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Electrical Characteristics

(V_{CC} = 14V, T_A = -40°C to +125°C, unless otherwise noted. Typical values are at T_A = +25°C.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
Supply Voltage Range	V_{CC}			5.5		72.0	V
Input Supply Current	I_{CC}	No load	V_{CC} = 12V		20	30	µA
			V_{CC} = 48V		25	40	
V_{CC} Undervoltage Lockout	V_{UVLO}	V_{CC} rising, part enabled, V_{INA+} = 2V, OUTA deasserted (MAX16010/MAX16011), V_{IN} = 2V, V_{OUT} deasserted (MAX16012), V_{SET} = 0V, GATE2 = V_{CLMP} (MAX16013/ MAX16014)		4.75	5	5.25	V
INA+/INB-/SET Threshold Voltage	V_{TH+}			1.215	1.245	1.265	V
	V_{TH-}	0.5% hysteresis, MAX16010/MAX16011		1.21	1.223	1.26	
		5.0% hysteresis, MAX16010/MAX16011/ MAX16013/MAX16014		1.15	1.18	1.21	
		7.5% hysteresis MAX16010/MAX16011		1.12	1.15	1.18	
Threshold-Voltage Hysteresis		MAX16010TAA/MAX16011TAA			0.5		%
		MAX16010TAB/MAX16011TAB/ MAX16013/MAX16014			5.0		
		MAX16010TAC/MAX16011TAC			7.5		
SET/IN_ Input Current		SET/IN_ = 2V		-100		+100	nA
IN_ Operating Voltage Range				0		4	V
Startup Response Time	t_{START}	V_{CC} rising from 0 to 5.5V			100		µs
IN_-to-OUT/SET-to-GATE2 Propagation Delay	t_{PROP}	IN_/SET rising from (V_{TH} - 100mV) to (V_{TH} + 100mV) or falling from (V_{TH} + 100mV) to (V_{TH} - 100mV) (no load)				2	µs
OUT_ Output-Voltage Low	V_{OL}	V_{CC} ≥ 5.5V, I_{SINK} = 3.2mA				0.4	V
		V_{CC} ≥ 2.8V, I_{SINK} = 100µA				0.4	V
OUT_ Leakage Current	I_{LEAK}	OUT_ = 72V				500	nA

Electrical Characteristics (continued)

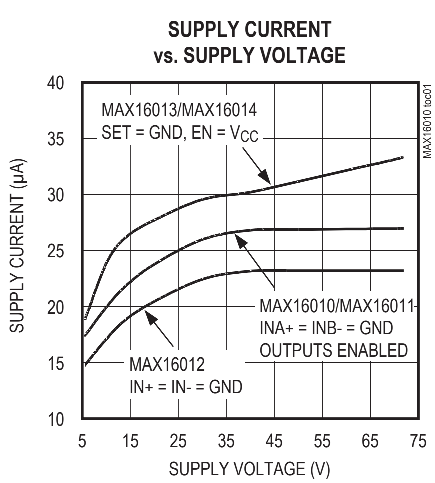
(V_{CC} = 14V, T_A = -40°C to +125°C, unless otherwise noted. Typical values are at T_A = +25°C.) (Note 1)

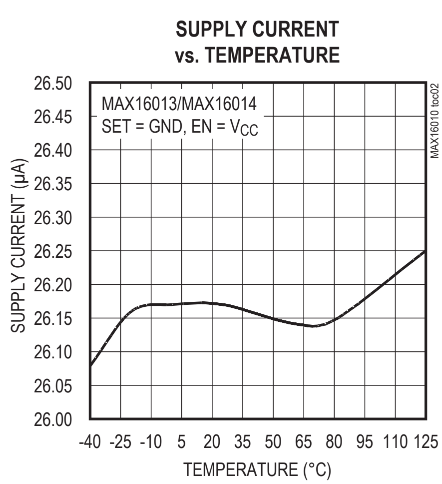
PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
EN/$\overline{EN}$, LOGIC Input Voltage	V_{IL}				0.4	V
	V_{IH}		1.4			
EN/$\overline{EN}$, LOGIC Input Current				1	2	µA
EN/$\overline{EN}$, LOGIC Pulse Width			10			µs
V_{CC}-to-GATE_ Output Low Voltage		I_{GATE_SINK} = 75µA, I_{GATE_SOURCE} = 1µA, V_{CC} = 14V	7		11	V
V_{CC}-to-GATE_ Clamp Voltage		V_{CC} = 24V	12		18	V
MAX16012						
Reference Output Voltage	V_{REF}	No load	1.275	1.3	1.320	V
Reference Short-Circuit Current	I_{SHORT}	REF = GND		100		µA
Reference Load Regulation		Sourcing, 0 ≤ I_{REF} ≤ 1µA		0.1		mV/µA
		Sinking, -1µA P I_{REF} ≤ 0		0.1		
Input Offset Voltage		V_{CM} = 0 to 2V	-12.5		+12.5	mV
Input Offset Current				3		nA
Input Hysteresis				8		mV
Common-Mode Voltage Range	CMVR		0		2.0	V
Common-Mode Rejection Ratio	CMRR	MAX16012, DC		70		dB
Comparator Power-Supply Rejection Ratio	PSRR	MAX16012, DC		70		dB

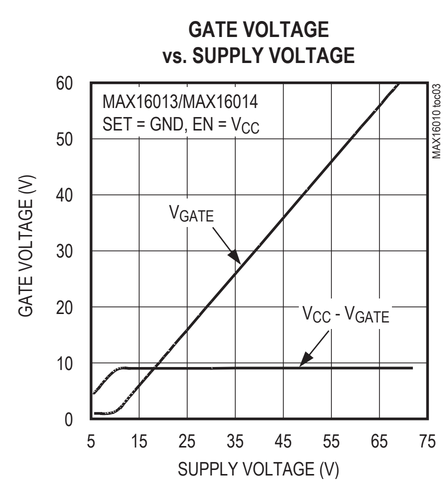
Note 1: 100% production tested at T_A = +25°C and T_A = +125°C. Specifications at T_A = -40°C are guaranteed by design.

Typical Operating Characteristics

(V_{IN} = 14V, T_A = +25°C, unless otherwise noted.)



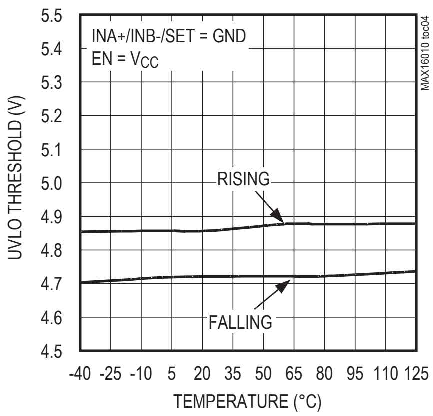




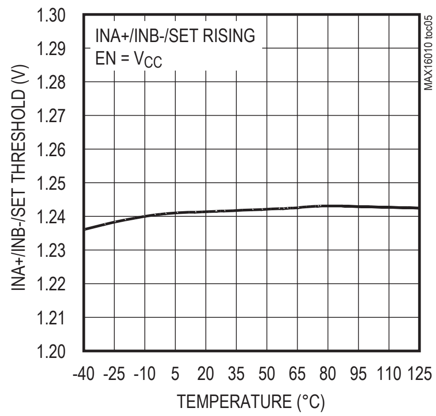
Typical Operating Characteristics (continued)

(V_{IN} = 14V, T_A = +25°C, unless otherwise noted.)

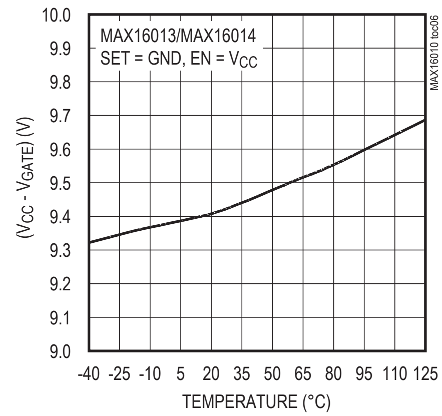
UVLO THRESHOLD vs. TEMPERATURE



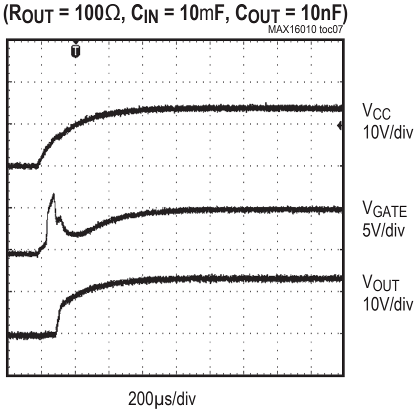
INA+/INB-/SET THRESHOLD vs. TEMPERATURE



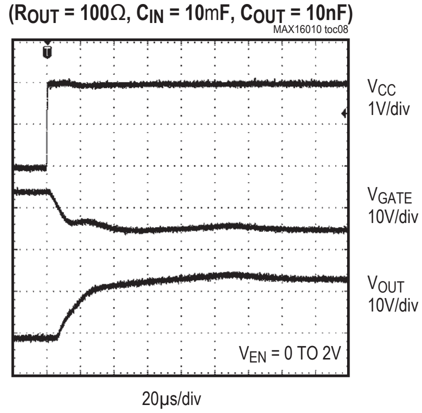
GATE VOLTAGE vs. TEMPERATURE



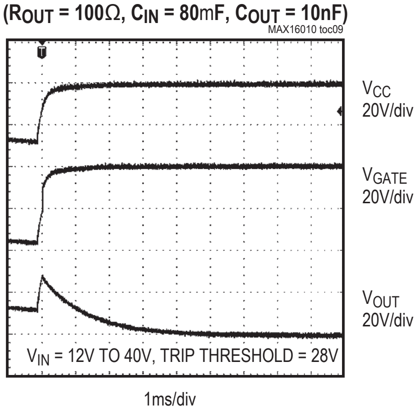
STARTUP WAVEFORM
(R_{OUT} = 100Ω, C_{IN} = 10mF, C_{OUT} = 10nF)



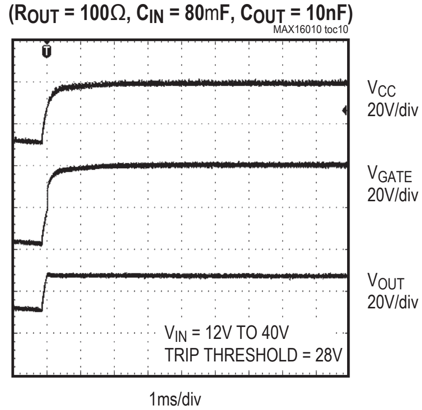
STARTUP WAVEFORM
(R_{OUT} = 100Ω, C_{IN} = 10mF, C_{OUT} = 10nF)



OVERVOLTAGE SWITCH FAULT
(R_{OUT} = 100Ω, C_{IN} = 80mF, C_{OUT} = 10nF)



OVERVOLTAGE LIMIT
(R_{OUT} = 100Ω, C_{IN} = 80mF, C_{OUT} = 10nF)



Pin Description

PIN				NAME	FUNCTION
MAX16010	MAX16011	MAX16012	MAX16013/ MAX16014		
1	1	1	1	V_{CC}	Positive-Supply Input Voltage. Connect V_{CC} to a 5.5V to 72V supply.
2	2	2	2	GND	Ground
3	—	—	—	$\overline{EN}$	Active-Low Enable Input. Drive $\overline{EN}$ low to turn on the voltage detectors. Drive $\overline{EN}$ high to force the OUTA and OUTB outputs low. $\overline{EN}$ is internally pulled up to V_{CC}. Connect $\overline{EN}$ to GND if not used.
4	4	—	—	OUTB	Open-Drain Monitor B Output. Connect a pullup resistor from OUTB to V_{CC}. OUTB goes low when INB- exceeds V_{TH+} and goes high when INB- drops below V_{TH-} (with LOGIC connected to GND for the MAX16011). Drive LOGIC high to reverse OUTB's logic state. OUTB is usually used as an overvoltage output. OUTB goes low (LOGIC = low) or high (LOGIC = high) when V_{CC} drops below the UVLO threshold voltage.
5	5	—	—	INB-	Adjustable Voltage Monitor Threshold Input
6	6	—	5	EN	Active-High ENABLE Input. For the MAX16010/MAX16011, drive EN high to turn on the voltage detectors. Drive EN low to force OUTA low and OUTB low (LOGIC = low) or high (LOGIC = high). For the MAX16013/MAX16014, drive EN high to enhance the p-channel MOSFET (P2), and drive EN low to turn off the MOSFET. EN is internally pulled down to GND. Connect EN to V_{CC} if not used.
7	7	—	—	OUTA	Open-Drain Monitor A Output. Connect a pullup resistor from OUTA to V_{CC}. OUTA goes low when INA+ drops below V_{TH-} and goes high when INA+ exceeds V_{TH+}. OUTA is usually used as an undervoltage output. OUTA also goes low when V_{CC} drops below the UVLO threshold voltage.
8	8	—	—	INA+	Adjustable Voltage Monitor Threshold Input
—	3	—	—	LOGIC	OUTB Logic-Select Input. Connect LOGIC to GND or V_{CC} to configure the OUTB logic. See the MAX16011 output logic table.
—	—	3	—	OUT	Open-Drain Comparator Output. Connect a pullup resistor from OUT to V_{CC}. OUT goes low when IN+ drops below IN-. OUT goes high when IN+ exceeds IN-.
—	—	4	—	IN-	Inverting Comparator Input
—	—	5	—	REF	Internal 1.30V Reference Output. Connect REF to IN+ for active-low output. Connect REF to IN- for active-high output. REF can source and sink up to 1µA. Leave REF floating if not used. REF output is stable with capacitive loads from 0 to 50pF.
—	—	6	—	IN+	Noninverting Comparator Input
—	—	—	3	GATE2	Gate-Driver Output. Connect GATE2 to the gate of an external p-channel MOSFET pass switch. GATE2 is driven low to the higher of V_{CC} - 10V or GND during normal operations and quickly shorted to V_{CC} during an overvoltage condition (SET above the internal threshold). GATE2 is shorted to V_{CC} when the supply voltage goes below the UVLO threshold voltage. GATE2 is shorted to V_{CC} when EN is low.
—	—	—	4	SET	Device Overvoltage-Threshold-Adjustment Input. Connect SET to an external resistive divider network to adjust the desired overvoltage disable or overvoltage limit threshold (see the *Typical Application Circuit and Overvoltage Limiter* section).
—	—	—	6	GATE1	Gate-Driver Output. Connect GATE1 to the gate of an external p-channel MOSFET to provide low drop reverse voltage protection.
—	—	—	—	EP	Exposed Pad. Connect EP to GND.

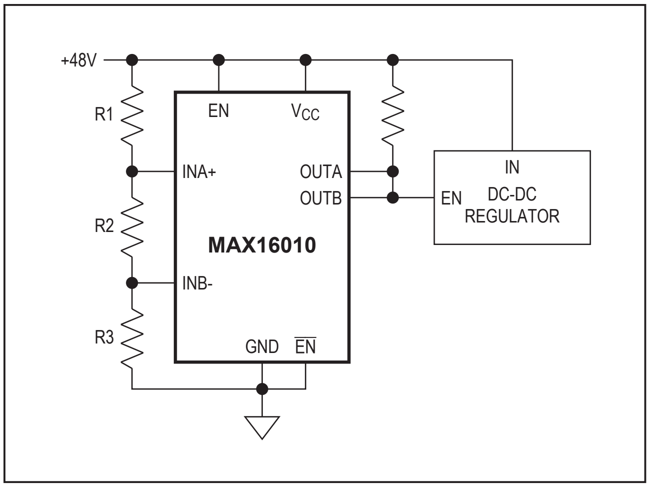


Figure 1. MAX16010 Monitor Circuit

Detailed Description

The MAX16010–MAX16014 is a family of ultra-small, low-power, overvoltage-protection circuits for high-voltage, high-transient systems such as those found in automotive, telecom, and industrial applications. These devices operate over a wide 5.5V to 72V supply voltage range, making them also suitable for other applications such as battery stacks, notebook computers, and servers.

The MAX16010 and MAX16011 offer two independent comparators for monitoring both undervoltage and overvoltage conditions. These comparators offer open-drain outputs capable of handling voltages up to 72V. The MAX16010 features complementary enable inputs (EN/$\overline{EN}$), while the MAX16011 features an active-high enable input and a selectable active-high/low OUTB output.

The MAX16012 offers a single comparator and an independent reference output. The reference output can be directly connected to either the inverting or noninverting input to select the comparator output logic.

The MAX16013 and MAX16014 are overvoltage-protection circuits capable of driving two p-channel MOSFETs to prevent reverse-battery and overvoltage conditions. One MOSFET (P1) eliminates the need for external diodes, thus minimizing the input voltage drop. While the second MOSFET (P2) isolates the load or regulates the output voltage during an overvoltage condition. The MAX16014 keeps the MOSFET (P2) latched off until the input power is cycled.

Voltage Monitoring

The MAX16010/MAX16011 include undervoltage and overvoltage comparators for window detection (see Figure 1). OUT_ asserts high when the monitored voltage is within the selected “window.” OUTA asserts low when the monitored voltage falls below the lower ($V_{TRIPLOW}$) limit of the window, or OUTB asserts low if the monitored voltage exceeds the upper limit ($V_{TRIPHIGH}$). The application in Figure 1 shows OUT_ enabling the DC-DC converter when the monitored voltage is in the selected window.

The resistor values (R1–R3) can be calculated as follows:

$$V_{TRIPLOW} = V_{TH-}\left(\frac{R_{TOTAL}}{R2 + R3}\right)$$

$$V_{TRIPHIGH} = V_{TH+}\left(\frac{R_{TOTAL}}{R3}\right)$$

where R_{TOTAL} = R1 + R2 + R3.

Use the following steps to determine the values for R1–R3.

1) Choose a value for R_{TOTAL}, the sum of R1, R2, and R3. Because the MAX16010/MAX16011 have very high input impedance, R_{TOTAL} can be up to 5MΩ.

2) Calculate R3 based on R_{TOTAL} and the desired upper trip point:

$$R3 = \frac{V_{TH+} \times R_{TOTAL}}{V_{TRIPHIGH}}$$

3) Calculate R2 based on R_{TOTAL}, R3, and the desired lower trip point:

$$R3 = \frac{V_{TH+} \times R_{TOTAL}}{V_{TRIPHIGH}}$$

4) Calculate R1 based on R_{TOTAL}, R3, and R2:

$$R1 = R_{TOTAL} - R2 - R3$$

The MAX16012 has both inputs of the comparator available with an integrated 1.30V reference (REF). When the voltage at IN+ is greater than the voltage at IN-, OUT goes high. When the voltage at IN- is greater than the voltage at IN+, OUT goes low. Connect REF to IN+ or IN- to set the reference-voltage value. Use an external resistive divider to set the monitored voltage threshold.

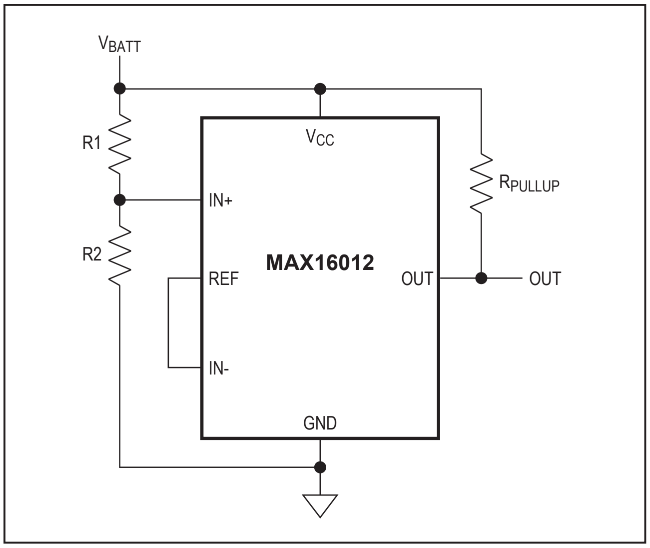


Figure 2. Typical Operating Circuit for the MAX16012

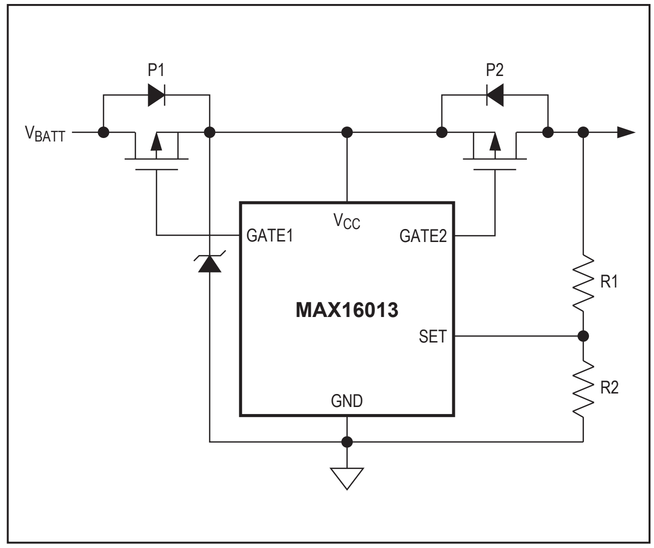


Figure 3. Overvoltage Limiter Protection

The MAX16013/MAX16014 can be configured as an overvoltage switch controller to turn on/off a load (see the *Typical Application Circuit*). When the programmed overvoltage threshold is tripped, the internal fast comparator turns off the external p-channel MOSFET (P2), pulling GATE2 to V_{CC} to disconnect the power source from the load. When the monitored voltage goes below the adjusted overvoltage threshold, the MAX16013 enhances GATE2, reconnecting the load to the power source (toggle ENABLE on the MAX16014 to reconnect the load). The MAX16013 can be configured as an overvoltage-limiter switch by connecting the resistive divider to the load instead of V_{CC} (Figure 3). See the *Overvoltage Limiter* section.

Supply Voltage

Connect a 5.5V to 72V supply to V_{CC} for proper operation. For noisy environments, bypass V_{CC} to GND with a 0.1μF or greater capacitor. When V_{CC} falls below the UVLO voltage, the following states are present (Table 1).

Table 1. UVLO State (V_{CC} < V_{UVLO})

PART	OUTA	OUTB	OUT	GATE2
MAX16010	Low	Low	—	—
MAX16011	Low	Low, LOGIC = low High, LOGIC = high	—	—
MAX16012	—	—	Low	—
MAX16013 MAX16014	—	—	—	High

Hysteresis

Hysteresis adds noise immunity to the voltage monitors and prevents oscillation due to repeated triggering when the monitored voltage is near the threshold trip voltage. The hysteresis in a comparator creates two trip points: one for the rising input voltage (V_{TH+}) and one for the falling input voltage (V_{TH-}). These thresholds are shown in Figure 4.

Enable Inputs (EN or $\overline{EN}$)

The MAX16011 offers an active-high enable input (EN), while the MAX16010 offers both an active-high enable input (EN) and an active-low enable input ($\overline{EN}$). For the MAX16010, drive EN low or $\overline{EN}$ high to force the output low. When the device is enabled (EN = high and $\overline{EN}$ = low) the state of OUTA and OUTB depends on the INA+ and INB- logic states.

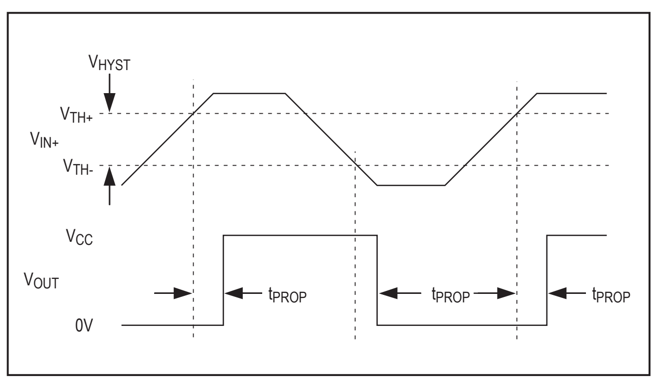


Figure 4. Input and Output Waveforms

Table 2. MAX16011 Output Logic

LOGIC	INA+	INB-	OUTA	OUTB
Low	> V_{TH+}	> V_{TH+}	High Impedance	Low
Low	< V_{TH-}	< V_{TH-}	Low	High Impedance
High	> V_{TH+}	> V_{TH+}	High Impedance	High Impedance
High	< V_{TH-}	< V_{TH-}	Low	Low

For the MAX16011, drive EN low to force OUTA low, OUTB low when LOGIC = low, and OUTB high when LOGIC = high. When the device is enabled (EN = high), the state of OUTA and OUTB depends on the INA+, INB-, and LOGIC input (see Table 2).

For the MAX16013/MAX16014, drive EN low to pull GATE2 to V_{CC}, turning off the p-channel MOSFET (P2). When the device is enabled (EN = high), GATE2 is pulled to the greater of (V_{CC} - 10V) or GND turning on the external MOSFET (P2).

Applications Information

Input Transients Clamping

When the external MOSFET is turned off during an overvoltage occurrence, stray inductance in the power path may cause voltage ringing to exceed the MAX16013/ MAX16014 absolute maximum input (V_{CC}) supply rating. The following techniques are recommended to reduce the effect of transients:

- Minimize stray inductance in the power path using wide traces, and minimize loop area including the power traces and the return ground path.
- Add a zener diode or transient voltage suppresser (TVS) rated below V_{CC} absolute maximum rating (Figure 3).

Overvoltage Limiter

When operating in overvoltage-limiter mode, the MAX16013 drives the external p-channel MOSFET (P2), resulting in the external MOSFET operating as a voltage regulator.

During normal operation, GATE2 is pulled to the greater of (V_{CC} - 10V) or GND. The external MOSFET's drain voltage is monitored through a resistor-divider between the P2 output and SET. When the output voltage rises above the adjusted overvoltage threshold, an internal comparator pulls GATE2 to V_{CC}. When the monitored voltage goes below the overvoltage threshold, the p-channel MOSFET (P2) is turned on again. This process continues to keep the voltage at the output regulated to within approximately a 5% window. The output voltage is regulated during the overvoltage transients and the MOSFET (P2) continues to conduct during the overvoltage event, operating in switched-linear mode.

Caution must be exercised when operating the MAX16013 in voltage-limiting mode for long durations due to the MOSFET's power-dissipation consideration (see the *MOSFET Selection and Operation* section).

MOSFET Selection and Operation (MAX16013 and MAX16014)

Most battery-powered applications must include reverse-voltage protection. Many times this is implemented with a diode in series with the battery. The disadvantage in using a diode is the forward-voltage drop of the diode, which reduces the operating voltage available to downstream circuits (V_{LOAD} = $V_{BATTERY}$ - V_{DIODE}). The MAX16013 and MAX16014 include high-voltage GATE1 drive circuitry, allowing users to replace the high-voltage-drop series diode with a low-voltage-drop MOSFET device (as shown in the *Typical Operating Circuit* and Figure 3). The forward-voltage drop is reduced to I_{LOAD} x R_{DS-ON} of P1. With a suitably chosen MOSFET, the voltage drop can be reduced to millivolts.

In normal operating mode, internal GATE1 output circuitry enhances P1 to a 10V gate-to-source (V_{GS}) for 11V < V_{CC} < 72V. The constant 10V enhancement ensures P1 operates in a low R_{DS-ON} mode, but the gate-source junction is not overstressed during high-battery-voltage applications or transients (many MOSFET devices specify a ±20V V_{GS} absolute maximum). As V_{CC} drops below 10V, GATE1 is limited to GND, reducing P1 V_{GS} to V_{CC} - GND. In normal operation, the P1 power dissipation is very low:

$$P1 = I_{LOAD}^2 \times R_{DS-ON}$$

During reverse-battery applications, GATE1 is limited to GND and the P1 gate-source junction is reverse biased. P1 is turned off and neither the MAX16013/MAX16014 nor the load circuitry is exposed to the reverse-battery voltage. Care should be taken to place P1 (and its internal drain-to-source diode) in the correct orientation for proper reverse-battery operation.

P2 protects the load from input overvoltage conditions. During normal operating modes (the monitored voltage is below the adjusted overvoltage threshold), internal

GATE2 output circuitry enhances P2 to a 10V gate-to-source (V_{GS}) for 11V < V_{CC} < 72V. The constant 10V enhancement ensures P2 operates in a low R_{DS-ON} mode, but the gate-to-source junction is not overstressed during high-battery-voltage applications (many pFET devices specify a ±20V V_{GS} absolute maximum). As V_{CC} drops below 10V, GATE2 is limited to GND, reducing P2 V_{GS} to V_{CC} - GND. In normal operation, the P2 power dissipation is very low:

$$P2 = I_{LOAD}2 \times R_{DS-ON}$$

During overvoltage conditions, P2 is either turned completely off (overvoltage-switch mode) or cycled off-on-off (voltage-limiter mode). Care should be taken to place P2 (and its internal drain-to-source diode) in the correct orientation for proper overvoltage-protection operation. During voltage-limiter mode, the drain of P2 is limited to the adjusted overvoltage threshold, while the battery (V_{CC}) voltage rises. During prolonged overvoltage events, P2 temperature can increase rapidly due to the high power dissipation. The power dissipated by P2 is:

$$P2 = V_{DS-P2} \times I_{LOAD}$$
$$= (V_{CC} - V_{OV-ADJUSTED}) \times I_{LOAD}$$

where V_{CC} ~ $V_{BATTERY}$ and $V_{OV-ADJUSTED}$ is the desired load-limit voltage. For prolonged overvoltage events with high P2 power dissipation, proper heatsinking is required.

Adding External Pullup Resistors

It may be necessary to add an external resistor from V_{CC} to GATE1 to provide enough additional pullup capability when the GATE1 input goes high. The GATE_ output can only source up to 1µA current. If the source current is less than 1µA, no external resistor may be necessary. However, to improve the pullup capability of the GATE_ output when it goes high, connect an external resistor between V_{CC} and the GATE_. The application shows a 2MΩ resistor, which is large enough not to impact the sinking capability of the GATE_ (during normal operation), while providing enough pullup during an overvoltage event. With an 11V (worst case) V_{CC}-to-gate clamp voltage and a sinking current of 75µA, the smallest resistor should be 11V/75µA, or about 147kΩ. However, since the GATE_ is typically low most of the time, a higher value should be used to reduce overall power consumption.

Functional Diagrams

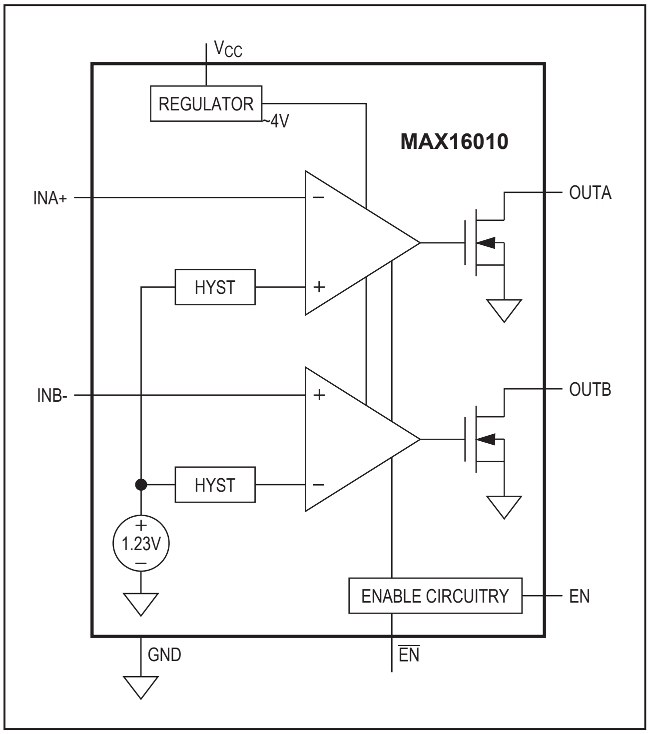


Figure 5. MAX16010 Functional Diagram

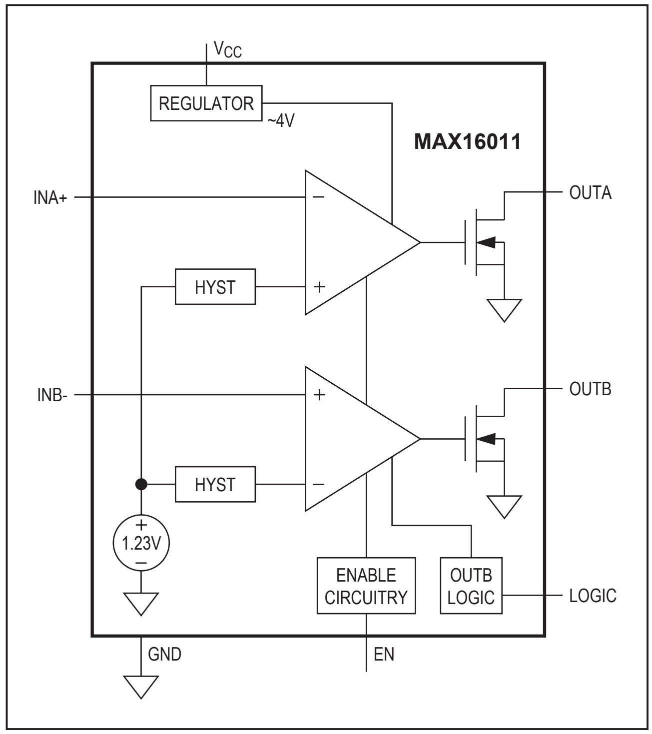


Figure 6. MAX16011 Functional Diagram

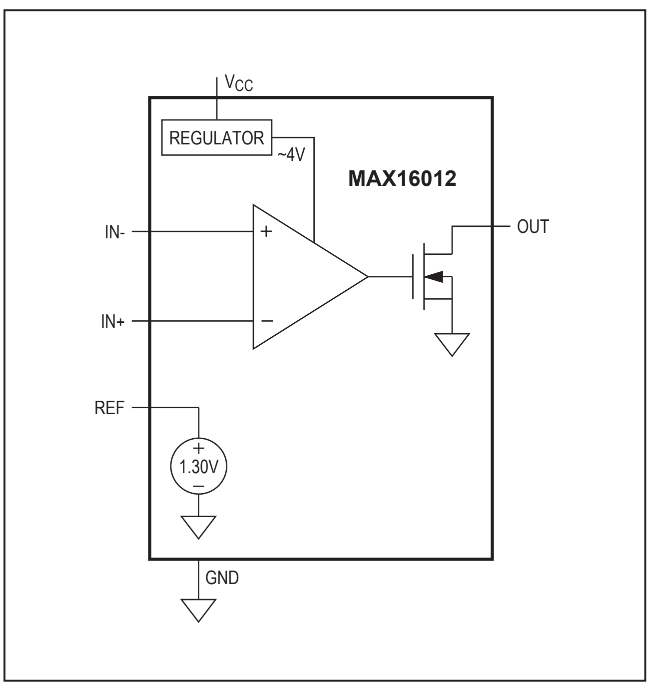


Figure 7. MAX16012 Functional Diagram

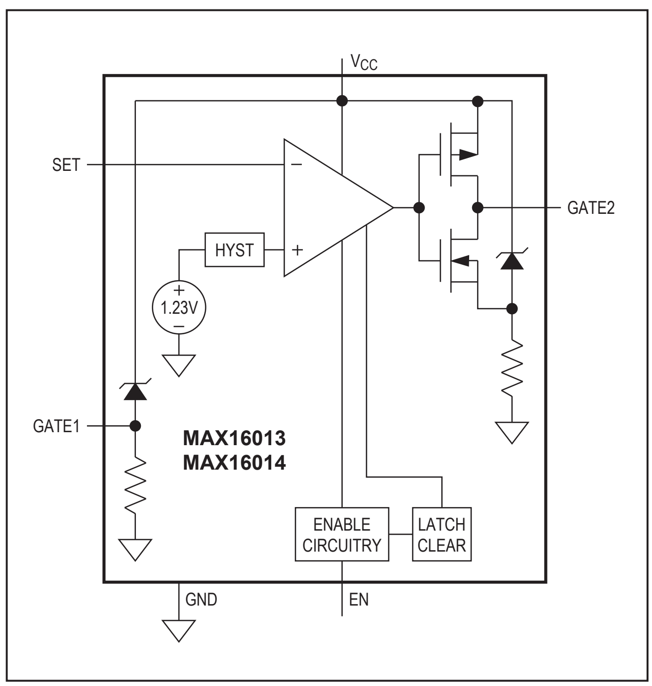
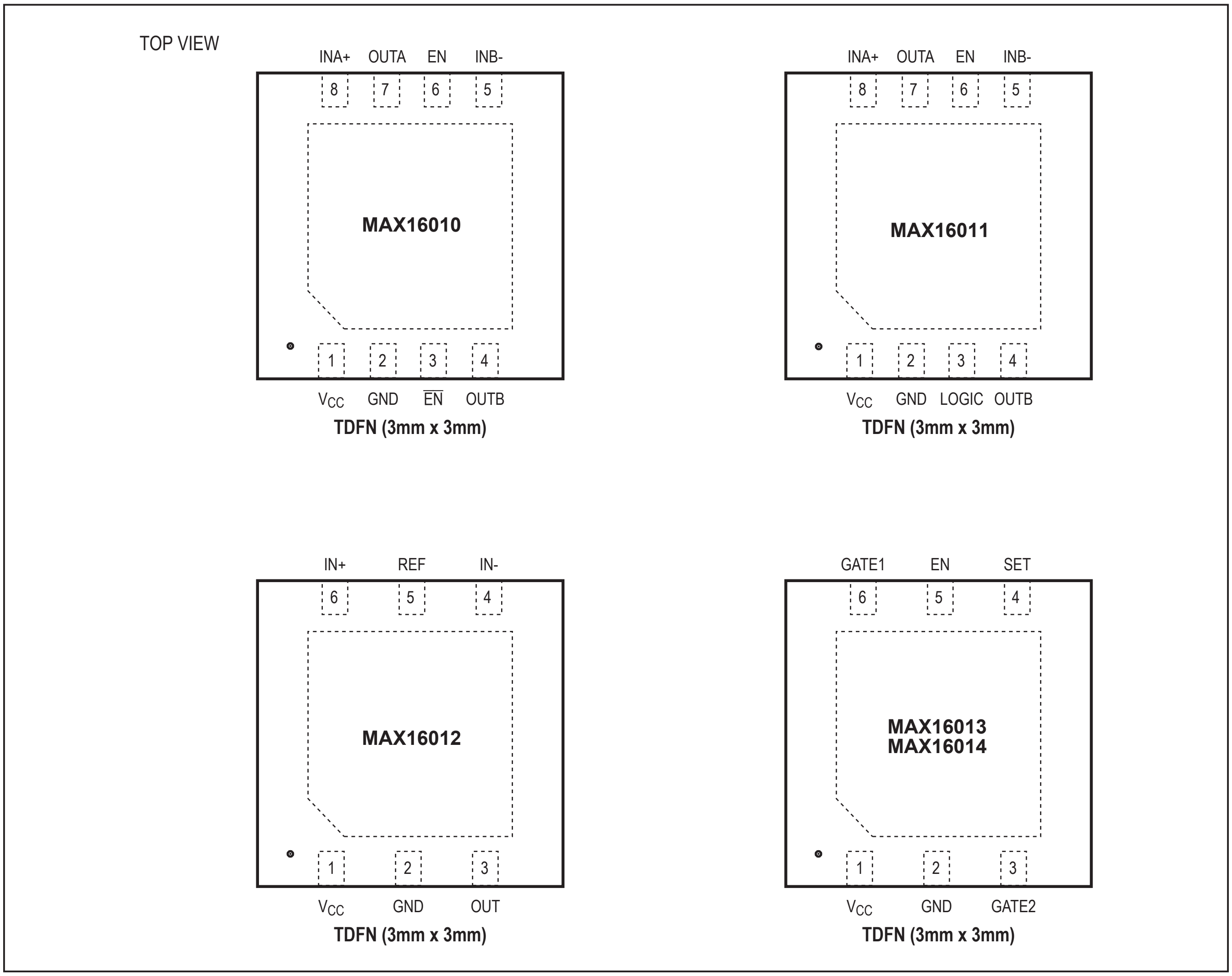


Figure 8. MAX16013/MAX16014 Functional Diagram

Pin Configurations



Chip Information

PROCESS: BiCMOS

Package Information

For the latest package outline information and land patterns (footprints), go to **www.maximintegrated.com/packages**. Note that a "+", "#", or "-" in the package code indicates RoHS status only. Package drawings may show a different suffix character, but the drawing pertains to the package regardless of RoHS status.

PACKAGE TYPE	PACKAGE CODE	DOCUMENT NO.
6 TDFN	T633-2	**21-0137**
8 TDFN	T833-2	**21-0137**

Revision History

REVISION NUMBER	REVISION DATE	DESCRIPTION	PAGES CHANGED
0	6/05	Initial release	—
1	12/05	Removed future product designation for MAX16010/MAX16011	1, 12
2	1/07	Edited Figure 7	1, 10, 12
3	12/07	Fixed text in *Voltage Monitoring* section and updated Package Outline	6, 12
4	9/08	Revised Figures 6 and 8.	10
5	2/15	No /V OPNs in *Ordering Information*; deleted automotive reference from *General Description* and *Applications* sections; deleted *Load Dump* section	1, 8