Characteristics EMIF02-1003M6

## 1 Characteristics

Table 1. Absolute ratings (limiting values at  $T_{amb}$  = 25 °C unless otherwise specified)

Symbol	Parameter	Value	Unit
V <sub>PP</sub>	ESD discharge IEC61000-4-2 air discharge on input and output pins ESD discharge IEC61000-4-2 contact discharge on input and output pins	15 8	kV
T <sub>j</sub>	Junction temperature	125	°C
T <sub>op</sub>	Operating temperature range	-40 to + 85	°C
T <sub>stg</sub>	Storage temperature range	-55 to +150	°C

Table 2. Electrical characteristics ( $T_{amb} = 25$  °C)

Table 2.	Electrical characteristics (Tamb = 25°C	,			
Symbol	Parameter		I A		
V <sub>BR</sub>	Breakdown voltage	   I <sub>E</sub>			
I <sub>RM</sub>	Leakage current @ V <sub>RM</sub>				
V <sub>RM</sub>	Stand-off voltage		VBR	V	
V <sub>CL</sub>	Clamping voltage	V <sub>CL</sub> ↓ V <sub>RM</sub> I <sub>RM</sub> → V		→ V	
R <sub>d</sub>	Dynamic resistance	la			
I <sub>PP</sub>	Peak pulse current				
R <sub>I/O</sub>	Series resistance between Input & Output	lpp			
C <sub>line</sub>	Input capacitance per line		1		
Symbol	Test conditions	Min.	Тур.	Max.	Unit
V <sub>BR</sub>	I <sub>R</sub> = 1 mA	5	6.5	8	V
I <sub>RM</sub>	V <sub>RM</sub> = 3 V per line			100	nA
R <sub>I/O</sub>	Tolerance ± 10%		100		Ω
C <sub>line</sub>	V <sub>R</sub> = 0 V <sub>DC</sub> , V <sub>OSC</sub> = 30 mV, F = 1 MHz		30	39	pF
S21	F = 900 MHz			-26	dB

EMIF02-1003M6 Characteristics

Figure 3. S21(db) attenuation measurement Figure 4. Analog cross talk measurements  $(V_{bias} = 0 \ V)$ 

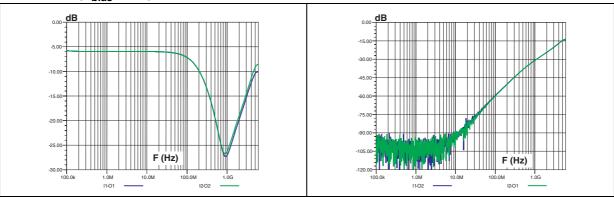


Figure 5. ESD response to IEC 61000-4-2 (+15 kV air discharge) on one input and on one output

Figure 6. ESD response to IEC 61000-4-2 (- 15 kV air discharge) on one input and on one output

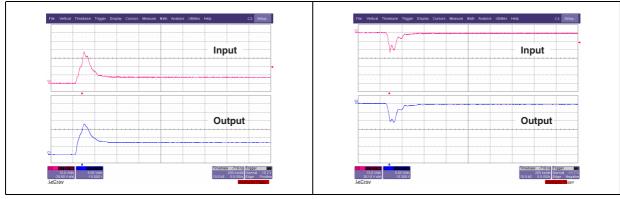
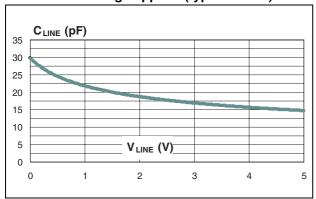


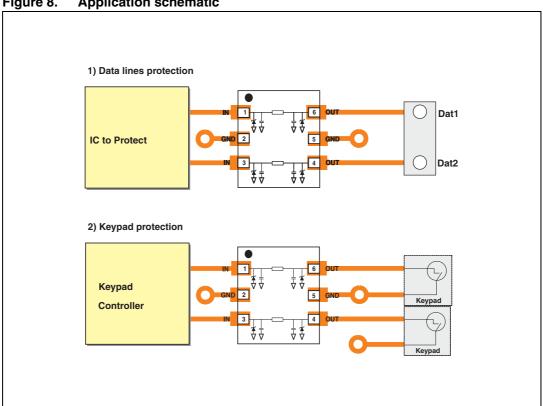
Figure 7. Line capacitance versus reverse voltage applied (typical value)



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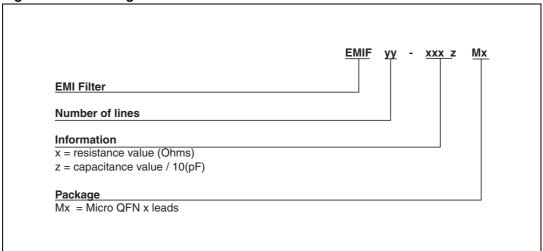
### **Application schematic** 2

Figure 8. **Application schematic** 



### Ordering information scheme 3

Figure 9. **Ordering information scheme** 



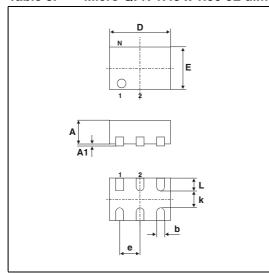
EMIF02-1003M6 Package information

## 4 Package information

### Epoxy meets UL94, V0

In order to meet environmental requirements, ST offers these devices in ECOPACK® packages. These packages have a lead-free second level interconnect. The category of second level interconnect is marked on the package and on the inner box label, in compliance with JEDEC Standard JESD97. The maximum ratings related to soldering conditions are also marked on the inner box label. ECOPACK is an ST trademark. ECOPACK specifications are available at: www.st.com.

Table 3. Micro QFN 1.45 x 1.00 6L dimensions



	Dimensions					
Ref.	Ref. Millimeter		rs	Inches		
	Min.	Тур.	Max.	Min.	Тур.	Max.
Α	0.50	0.55	0.60	0.020	0.022	0.024
A1	0.00	0.02	0.05	0.000	0.001	0.002
b	0.18	0.25	0.30	0.007	0.010	0.012
D		1.45			0.057	
Е		1.00			0.039	
е		0.50			0.020	
K	0.20			0.008		
L	0.30	0.35	0.40	0.012	0.014	0.016

Figure 10. Footprint in mm [inches]

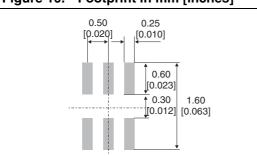


Figure 11. Marking

Dot: Pin 1 Identification

XX = Marking

Package information EMIF02-1003M6

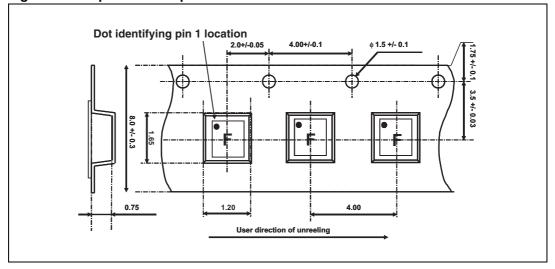


Figure 12. Tape and reel specification

Note:

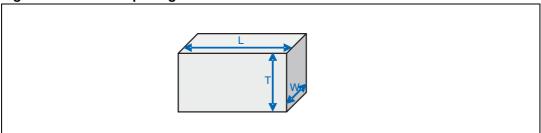
Product marking may be rotated by 90° for assembly plant differentiation. In no case should this product marking be used to orient the component for its placement on a PCB. Only pin 1 mark is to be used for this purpose.

## 5 Recommendation on PCB assembly

## 5.1 Stencil opening design

- 1. General recommendation on stencil opening design
  - a) Stencil Opening Dimensions: L (Length), W (Width), T (Thickness).

Figure 13. Stencil opening dimensions



b) General Design Rule

Stencil thickness (T) = 75 
$$\sim$$
 125  $\mu$ m

Aspect Ratio = 
$$\frac{W}{T} \ge 1.5$$

Aspect Area = 
$$\frac{L \times W}{2T(L+W)} \ge 0.66$$

- 2. Reference design
  - a) Stencil opening thickness: 100 µm
  - b) Stencil opening for central exposed pad: Opening to footprint ratio is 50%.
  - c) Stencil opening for leads: Opening to footprint ratio is 90%.

### 5.2 Solder paste

- 1. Halide-free flux qualification ROL0 according to ANSI/J-STD-004.
- 2. "No clean" solder paste is recommended.
- 3. Offers a high tack force to resist component movement during high speed
- 4. Solder paste with fine particles: powder particle size is 20-45 μm.

### 5.3 Placement

- 1. Manual positioning is not recommended.
- 2. It is recommended to use the lead recognition capabilities of the placement system, not the outline centering
- 3. Standard tolerance of + 0.05 mm is recommended.
- 4. 3.5 N placement force is recommended. Too much placement force can lead to squeezed out solder paste and cause solder joints to short. Too low placement force can lead to insufficient contact between package and solder paste that could cause open solder joints or badly centered packages.
- 5. To improve the package placement accuracy, a bottom side optical control should be performed with a high resolution tool.
- 6. For assembly, a perfect supporting of the PCB (all the more on flexible PCB) is recommended during solder paste printing, pick and place and reflow soldering by using optimized tools.

## 5.4 PCB design preference

- 1. To control the solder paste amount, the closed via is recommended instead of open vias.
- 2. The position of tracks and open vias in the solder area should be well balanced. The symmetrical layout is recommended, in case any tilt phenomena caused by asymmetrical solder paste amount due to the solder flow away.

### 5.5 Reflow profile

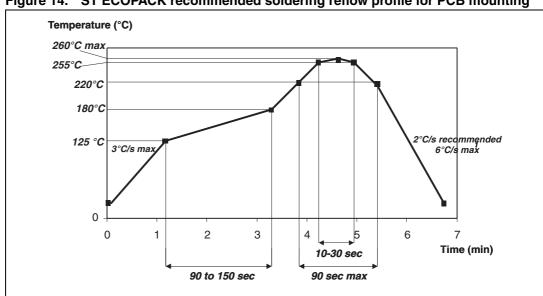


Figure 14. ST ECOPACK recommended soldering reflow profile for PCB mounting

Note: Minimize air convection currents in the reflow oven to avoid component movement.

# 6 Ordering information

Table 4. Ordering information

Part number	Marking	Package	Weight	Base qty	Delivery mode
EMIF02-1003M6	F <sup>(1)</sup>	Micro QFN	2.2 mg	3000	Tape and reel (7")

<sup>1.</sup> The marking can be rotated by  $90^{\circ}$  to differentiate assembly location

# 7 Revision history

Table 5. Document revision history

Date	Revision	Changes
07-Oct-2007	1	Initial release.

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