

50Ω, Dual SPST Analog Switches in UCSP

ABSOLUTE MAXIMUM RATINGS

(All voltages referenced to GND.)

V+	-0.3V to +12V
IN ₋ , COM ₋ , NO ₋ , NC ₋ (Note 1)	-0.3V to (V+ + 0.3V)
Continuous Current (any pin)	±10mA
Peak Current (any pin, pulsed at 1ms, 10% duty cycle)	±20mA
Continuous Power Dissipation (T _A = +70°C)	
8-Pin μMAX (derate 4.5mW/°C above +70°C)	362mW
8-Pin TDFN (derate 24.4mW/°C above +70°C)	1951mW
9-Bump UCSP (derate 4.7mW/°C above +70°C)	379mW

Operating Temperature Range	-40°C to +85°C
Storage Temperature Range	-65°C to +150°C
Maximum Junction Temperature	+150°C
Lead Temperature (soldering, 10s)	+300°C
Bump Temperature (soldering, Note 2)	
Infrared (15s)	+220°C
Vapor Phase (60s)	+215°C

Note 1: Signals on IN₋, NO₋, NC₋, or COM₋ exceeding V+ or GND are clamped by internal diodes. Limit forward-diode current to maximum current rating.

Note 2: This device is constructed using a unique set of packaging techniques that impose a limit on the thermal profile the device can be exposed to during board level solder attach and rework. This limit permits only the use of the solder profiles recommended in the industry-standard specification, JEDEC 020A, paragraph 7.6, Table 3 for IR/VPR and Convection reflow. Pre-heating is required. Hand or wave soldering is not allowed.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS—Single +3V Supply

(V+ = +3V ±10%, V_{IH} = +2.0V, V_{IL} = +0.8V, T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are at V+ = +3V, T_A = +25°C.) (Notes 3, 4)

PARAMETER	SYMBOL	CONDITIONS	T _A	MIN	TYP	MAX	UNITS
ANALOG SWITCH							
Analog Signal Range	V _{COM-} , V _{NO-} , V _{Nc-}			0		V+	V
On-Resistance	R _{ON}	V+ = +2.7V, I _{COM-} = 5mA; V _{NO-} or V _{Nc-} = +1.5V	+25°C		19	50	Ω
			T _{MIN} to T _{MAX}			60	
On-Resistance Matching Between Channels (Notes 5, 6)	ΔR _{ON}	V+ = +2.7V, I _{COM-} = 5mA; V _{NO-} or V _{Nc-} = +1.5V	+25°C		0.8	3.5	Ω
			T _{MIN} to T _{MAX}			4.5	
On-Resistance Flatness (Note 7)	R _{FLAT(ON)}	V+ = +2.7V, I _{COM-} = 5mA; V _{NO-} or V _{Nc-} = +1V, +1.5V, +2V	+25°C		2.3	9	Ω
			T _{MIN} to T _{MAX}			11	
NO ₋ or NC ₋ Off-Leakage Current (Note 8)	I _{NO-(OFF)} I _{NC-(OFF)}	V+ = +3.6V, V _{COM-} = +0.3V, +3V; V _{NO-} or V _{Nc-} = +3V, +0.3V	+25°C	-0.1		+0.1	nA
			T _{MIN} to T _{MAX}	-2		+2	
COM ₋ Off-Leakage Current (Note 8)	I _{COM-(OFF)}	V+ = +3.6V, V _{COM-} = +0.3V, +3V; V _{NO-} or V _{Nc-} = +3V, +0.3V	+25°C	-0.1		+0.1	nA
			T _{MIN} to T _{MAX}	-2		+2	
COM ₋ On-Leakage Current (Note 8)	I _{COM-(ON)}	V+ = +3.6V, V _{COM-} = +0.3V, +3.0V; V _{NO-} or V _{Nc-} = +0.3V, +3V, or floating	+25°C	-0.2		+0.2	nA
			T _{MIN} to T _{MAX}	-4		+4	

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MAX4731/MAX4732/MAX4733

ELECTRICAL CHARACTERISTICS—Single +3V Supply (continued)

(V+ = +3V ±10%, VIH = +2.0V, VIL = +0.8V, TA = TMIN to TMAX, unless otherwise noted. Typical values are at V+ = +3V, TA = +25°C.)
(Notes 3, 4)

PARAMETER	SYMBOL	CONDITIONS	TA	MIN	TYP	MAX	UNITS
DYNAMIC CHARACTERISTICS							
Turn-On Time	tON	VNO_ or VNC_ = +1.5V, RL = 300Ω, CL = 35pF, Figure 2	+25°C		70	150	ns
			TMIN to TMAX			170	
Turn-Off Time	tOFF	VNO_ or VNC_ = +1.5V, RL = 300Ω, CL = 35pF, Figure 2	+25°C		30	60	ns
			TMIN to TMAX			70	
Break-Before-Make (MAX4733 Only, Note 8)	tBBM	VNO_ or VNC_ = +1.5V, RL = 300Ω, CL = 35pF, Figure 3	+25°C		40		ns
			TMIN to TMAX	1			
Charge Injection	Q	VGEN = 0V, RGEN = 0, CL = 1.0nF, Figure 4	+25°C		7.5		pC
On-Channel -3dB Bandwidth	BW	Signal = 0dBm, 50Ω in and out	+25°C		300		MHz
Off-Isolation (Note 9)	VISO	f = 1MHz, VCOM_ = 1VRMS, RL = 50Ω, CL = 5pF, Figure 5	+25°C		-72		dB
Crosstalk (Note 10)	VCT	f = 1MHz, VCOM_ = 1VRMS, RL = 50Ω, CL = 5pF, Figure 6	+25°C		-108		dB
NO_ or NC_ Off-Capacitance	COFF	f = 1MHz, Figure 7	+25°C		20		pF
COM_ Off-Capacitance	CCOM_(OFF)	f = 1MHz, Figure 7	+25°C		20		pF
COM_ On-Capacitance	CCOM_(ON)	f = 1MHz, Figure 7	+25°C		40		pF
LOGIC INPUT							
Input Logic High	VIH			1.4			V
Input Logic Low	VIL					0.8	V
Input Leakage Current	IIN	VIN_ = 0V or V+		-1	+0.005	+1	μA
SUPPLY							
Power-Supply Range	V+			2.0		11	V
Positive Supply Current	I+	V+ = +5.5V, VIN_ = 0V or V+, all switches on or off			0.0001	1	μA

50Ω, Dual SPST Analog Switches in UCSP

MAX4731/MAX4732/MAX4733

ELECTRICAL CHARACTERISTICS—Single +5V Supply

(V+ = +5V ±10%, V_{IH} = +2.0V, V_{IL} = +0.8V, T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are at V+ = +5V, T_A = +25°C.)
(Notes 3, 4)

PARAMETER	SYMBOL	CONDITIONS	T _A	MIN	TYP	MAX	UNITS
ANALOG SWITCH							
Analog Signal Range	V _{COM_} , V _{NO_} , V _{NC_}			0		V+	V
On-Resistance	R _{ON}	V+ = +4.5V, I _{COM_} = 5mA, V _{NO_} or V _{NC_} = +3.5V	+25°C		8.5	25	Ω
			T _{MIN} to T _{MAX}			30	
On-Resistance Matching Between Channels (Notes 5, 6)	ΔR _{ON}	V+ = +4.5V, I _{COM_} = 5mA, V _{NO_} or V _{NC_} = +3.5V	+25°C		0.2	3	Ω
			T _{MIN} to T _{MAX}			4	
On-Resistance Flatness (Note 7)	R _{FLAT(ON)}	V+ = +4.5V, I _{COM_} = 5mA, V _{NO_} or V _{NC_} = +1V, +2V, +3V	+25°C		2	5	Ω
			T _{MIN} to T _{MAX}			7	
NO_ or NC_ Off-Leakage Current (Note 8)	I _{NO_(OFF)} I _{NC_(OFF)}	V+ = +5.5V, V _{COM_} = +1V, +4.5V; V _{NO_} or V _{NC_} = +4.5V, +1V	+25°C	-0.1		+0.1	nA
			T _{MIN} to T _{MAX}	-2		+2	
COM_ Off-Leakage Current (Note 8)	I _{COM_(OFF)}	V+ = +5.5V, V _{COM_} = +1V, +4.5V; V _{NO_} or V _{NC_} = +4.5V, +1V	+25°C	-0.1		+0.1	nA
			T _{MIN} to T _{MAX}	-2		+2	
COM_ On-Leakage Current (Note 8)	I _{COM_(ON)}	V+ = +5.5V, V _{COM_} = +1V, +4.5V; V _{NO_} or V _{NC_} = +1V, +4.5V, or floating	+25°C	-0.2		+0.2	nA
			T _{MIN} to T _{MAX}	-4		+4	
DYNAMIC CHARACTERISTICS							
Turn-On Time	t _{ON}	V _{NO_} or V _{NC_} = +3.0V, R _L = 300Ω, C _L = 35pF, Figure 2	+25°C		47	85	ns
			T _{MIN} to T _{MAX}			95	
Turn-Off Time	t _{OFF}	V _{NO_} or V _{NC_} = +3.0V, R _L = 300Ω, C _L = 35pF, Figure 2	+25°C		23	45	ns
			T _{MIN} to T _{MAX}			55	
Break-Before-Make (MAX4733 Only, Note 8)	t _{BBM}	V _{NO_} or V _{NC_} = +3.0V, R _L = 300Ω, C _L = 35pF, Figure 3	+25°C		25		ns
			T _{MIN} to T _{MAX}	1			
Charge Injection	Q	V _{GEN} = 0V, R _{GEN} = 0, C _L = 1.0nF, Figure 4	+25°C		7.5		pC
On-Channel Bandwidth	BW	Signal = 0dBm, 50Ω in and out	+25°C		300		MHz
Off-Isolation (Note 9)	V _{ISO}	f = 1MHz, V _{COM_} = 1V _{RMS} , R _L = 50Ω, C _L = 5pF, Figure 5	+25°C		-72		dB

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MAX4731/MAX4732/MAX4733

ELECTRICAL CHARACTERISTICS—Single +5V Supply

(V+ = +5V ±10%, V_{IH} = +2.0V, V_{IL} = +0.8V, T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are at V+ = +5V, T_A = +25°C.) (Notes 3, 4)

PARAMETER	SYMBOL	CONDITIONS	T _A	MIN	TYP	MAX	UNITS
Crosstalk (Note 10)	V _{CT}	f = 1MHz, V _{COM_} = 1V _{RMS} , R _L = 50Ω, C _L = 5pF, Figure 6	+25°C		-108		dB
NO_ or NC_ Off-Capacitance	C _{OFF}	f = 1MHz, Figure 7	+25°C		20		pF
COM_ Off-Capacitance	C _{COM_(OFF)}	f = 1MHz, Figure 7	+25°C		20		pF
COM_ On-Capacitance	C _{COM_(ON)}	f = 1MHz, Figure 7	+25°C		40		pF
LOGIC INPUT							
Input Logic High	V _{IH}			2.0			V
Input Logic Low	V _{IL}					0.8	V
Input Leakage Current	I _{IN}	V _{IN_} = 0V or V+		-1	+0.005	+1	μA
SUPPLY							
Power-Supply Range	V+			2.0		11	V
Positive Supply Current	I+	V+ = +5.5V, V _{IN_} = 0V or V+, all switches on or off			0.0001	1	μA

Note 3: The algebraic convention, where the most negative value is a minimum and the most positive value a maximum, is used in this data sheet.

Note 4: UCSP and TDFN parts are 100% tested at +25°C only, and guaranteed by design over temperature. μMAX parts are 100% tested at +85°C and +25°C and guaranteed by design over temperature.

Note 5: ΔR_{ON} = R_{ON(MAX)} - R_{ON(MIN)}.

Note 6: UCSP on-resistance matching between channels and on-resistance flatness guaranteed by design.

Note 7: Flatness is defined as the difference between the maximum and minimum value of on-resistance as measured over the specified analog signal range.

Note 8: Guaranteed by design.

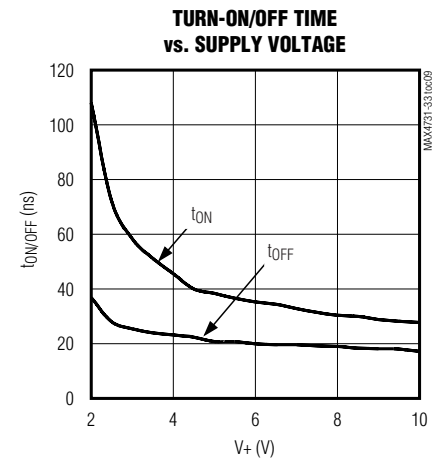
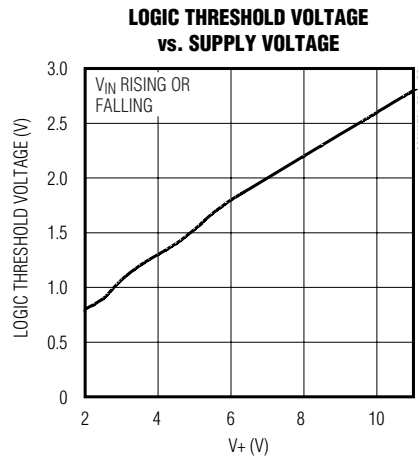
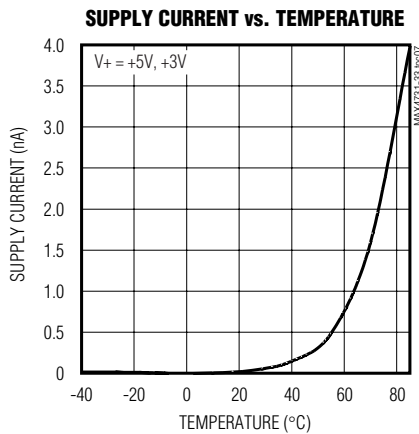
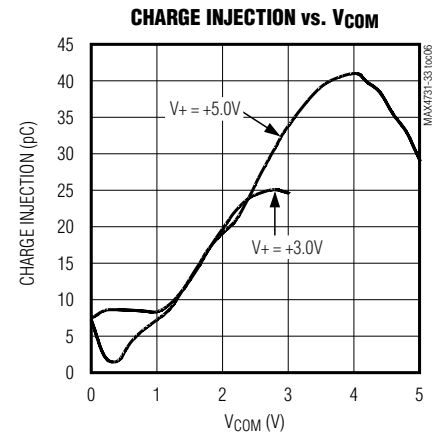
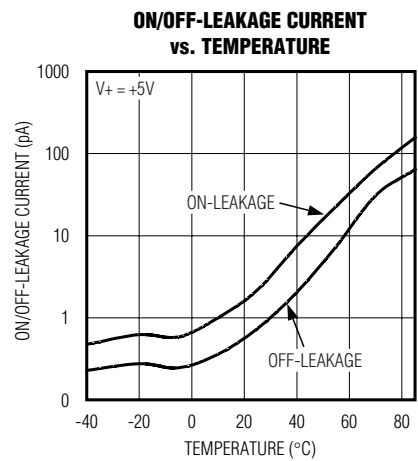
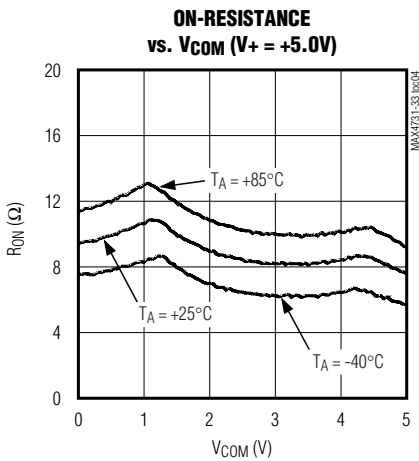
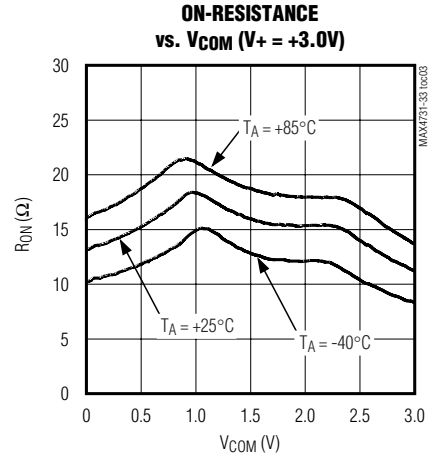
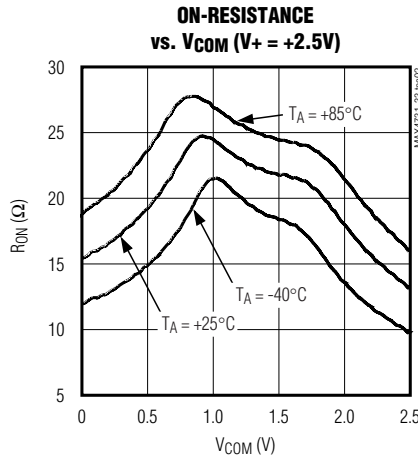
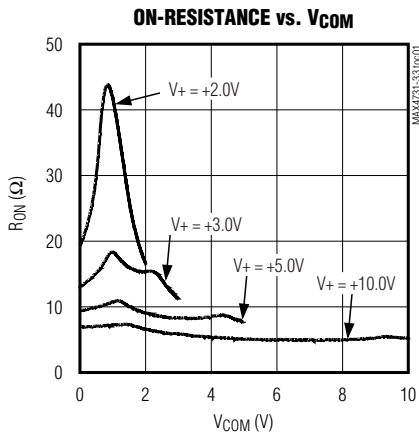
Note 9: Off-Isolation = 20 log₁₀ (V_{NO_}/V_{COM_}), V_{NO_} = output, V_{COM_} = input to off switch.

Note 10: Between any two switches.

50Ω, Dual SPST Analog Switches in UCSP

Typical Operating Characteristics

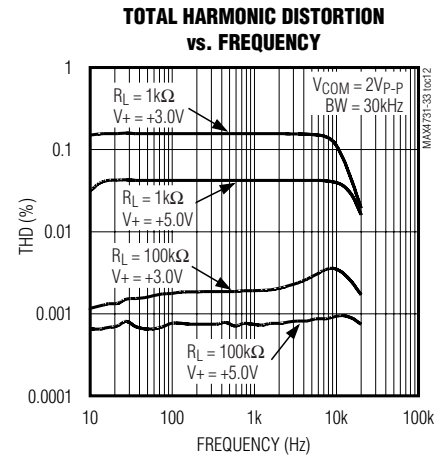
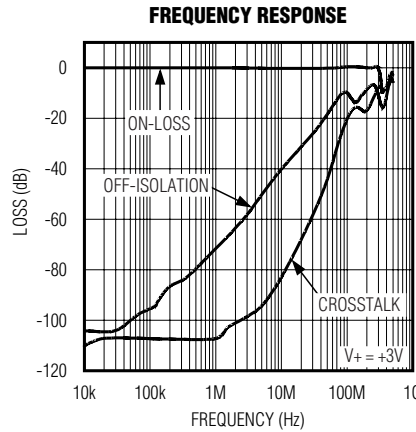
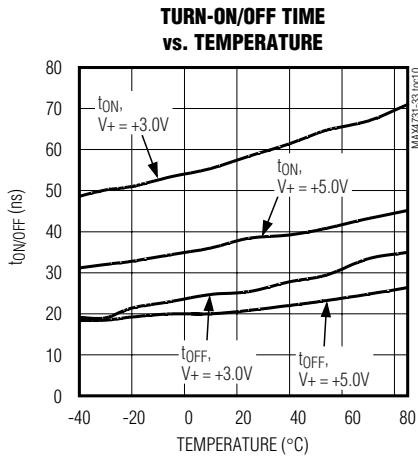
($T_A = +25^\circ\text{C}$, unless otherwise noted.)



50Ω, Dual SPST Analog Switches in UCSP

Typical Operating Characteristics (continued)

($T_A = +25^\circ\text{C}$, unless otherwise noted.)



Pin Description

PIN						NAME	FUNCTION
MAX4731		MAX4732		MAX4733			
UCSP	μMAX/ TDFN	UCSP	μMAX/ TDFN	UCSP	μMAX/ TDFN		
A1	1	—	—	A1	1	NO1	Analog-Switch Normally Open Terminal
A2	2	A2	2	A2	2	COM1	Analog-Switch Common Terminal
A3	4	A3	4	A3	4	GND	Ground. Connect to digital ground.
B1	7	B1	7	B1	7	IN1	Logic-Control Digital Input
B3	3	B3	3	B3	3	IN2	Logic-Control Digital Input
C1	8	C1	8	C1	8	V+	Positive Supply Voltage Input
C2	6	C2	6	C2	6	COM2	Analog-Switch Common Terminal
C3	5	—	—	—	—	NO2	Analog-Switch Normally Open Terminal
—	—	A1	1	—	—	NC1	Analog-Switch Normally Closed Terminal
—	—	C3	5	C3	5	NC2	Analog-Switch Normally Closed Terminal
—	EP (TDFN only)	—	EP (TDFN only)	—	EP (TDFN only)	EP	Exposed Pad. Connect to V+.

Applications Information

Operating Considerations for High-Voltage Supply

The MAX4731/MAX4732/MAX4733 operate to +11V with some precautions. The absolute maximum rating for V+ is +12V (referenced to GND). When operating near this region, bypass V+ with a minimum 0.1μF capacitor to ground as close to the IC as possible.

Logic Levels

The MAX4731/MAX4732/MAX4733 are TTL compatible when powered from a single +5V supply. When powered from other supply voltages, the logic inputs should be driven rail-to-rail. For example, with a +11V supply, IN1 and IN2 should be driven low to 0V and high to 11V. With a +3.3V supply, IN1 and IN2 should be driven low to 0V and high to 3.3V. Driving IN1 and IN2 rail-to-rail minimizes power consumption.

50Ω, Dual SPST Analog Switches in UCSP

Analog Signal Levels

Analog signals that range over the entire supply voltage (GND to V+) pass with very little change in R_{ON} (see *Typical Operating Characteristics*). The bidirectional switches allow NO_, NC_, and COM_ connections to be used as either inputs or outputs.

Power-Supply Sequencing and Overvoltage Protection

CAUTION: Do not exceed the absolute maximum ratings. Stresses beyond the listed ratings can cause permanent damage to the devices.

Proper power-supply sequencing is recommended for all CMOS devices. Always apply V+ before applying analog signals, especially if the analog signal is not current limited. If this sequencing is not possible, and if the analog inputs are not current limited to < 20mA, add a small-signal diode, D1, as shown in Figure 1. If the analog signal can dip below GND, add D2. Adding protection diodes reduces the analog signal range to a diode drop (about 0.7V) below V+ (for D1), and to a diode drop above ground (for D2). Leakage is unaffected by adding the diodes. On-resistance increases slightly at low supply voltages. Maximum supply voltage (V+) must not exceed +11V.

Adding protection diodes causes the logic thresholds to be shifted relative to the power-supply rails. The most significant shift occurs when using low supply voltages (+5V or less). With a +5V supply, TTL compatibility is not guaranteed when protection diodes are added. Driving IN1 and IN2 all the way to the supply rails (i.e., to a diode drop higher than the V+ pin, or to a diode drop lower than the GND pin) is always acceptable.

Protection diodes D1 and D2 also protect against some overvoltage situations. Using the circuit in Figure 1, no damage results if the supply voltage is below the absolute maximum rating (+12V) and if a fault voltage up to the absolute maximum rating (V+ + 0.3V) is applied to an analog signal terminal.

UCSP Applications Information

For the latest application details on UCSP construction, dimensions, tape carrier information, printed circuit board techniques, bump-pad layout, and recommended reflow temperature profile as well as the latest information on reliability testing results, go to the Maxim web site at www.maxim-ic.com/ucsp to find the Application Note: UCSP—A Wafer-Level Chip-Scale Package.

Test Circuits/Timing Diagrams

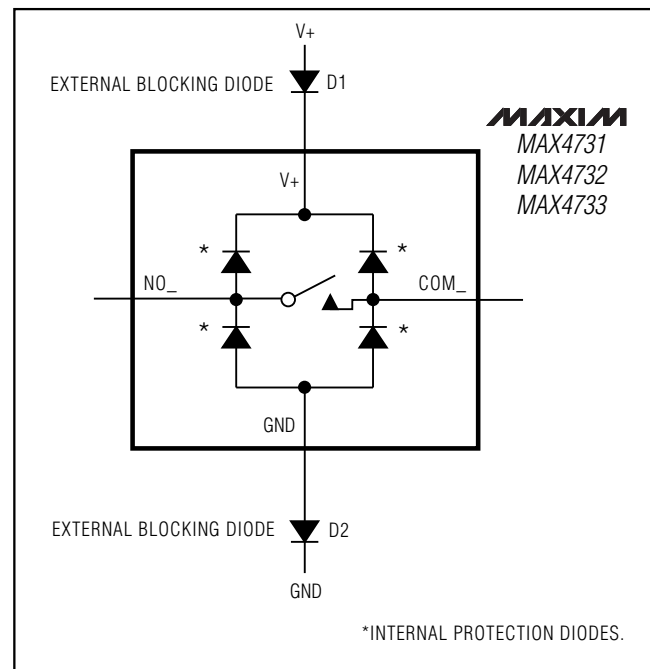


Figure 1. Overvoltage Protection Using External Blocking Diodes

50Ω, Dual SPST Analog Switches in UCSP

Test Circuits/Timing Diagrams (continued)

MAX4731/MAX4732/MAX4733

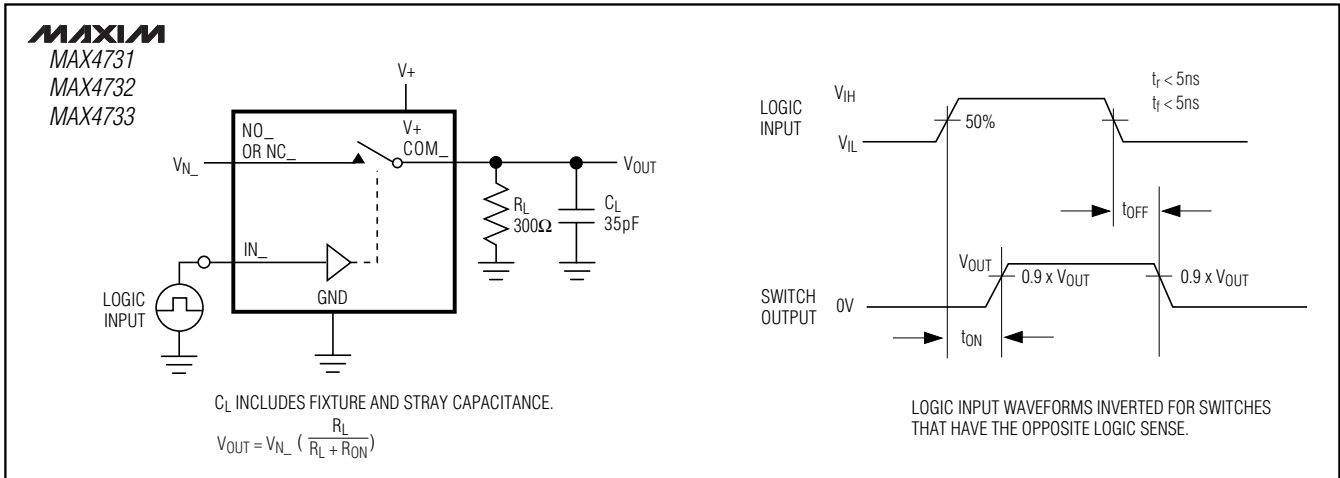


Figure 2. Switching Time

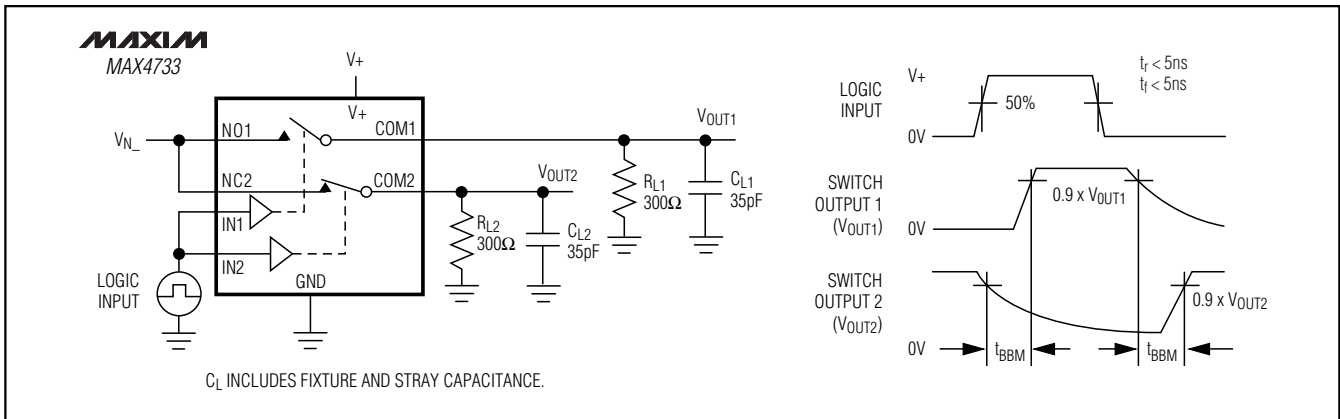


Figure 3. Break-Before-Make Interval (MAX4733 only)

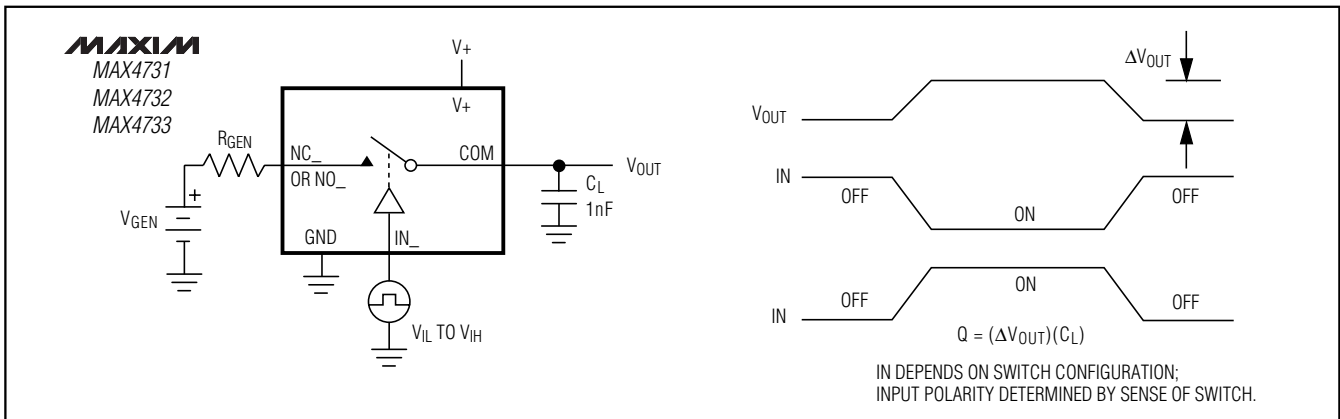


Figure 4. Charge Injection

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Test Circuits/Timing Diagrams (continued)

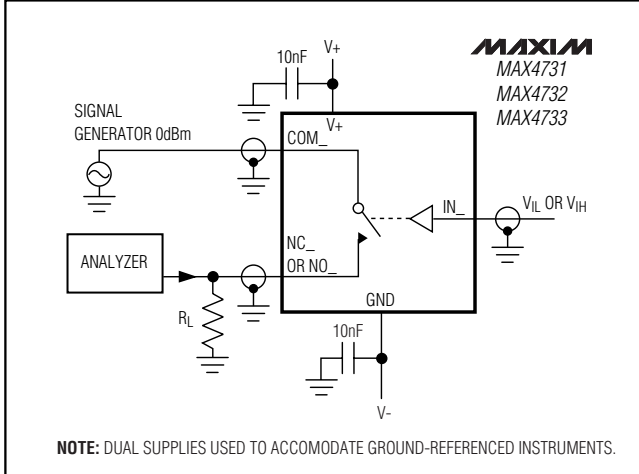


Figure 5. Off-Isolation/On-Channel Bandwidth

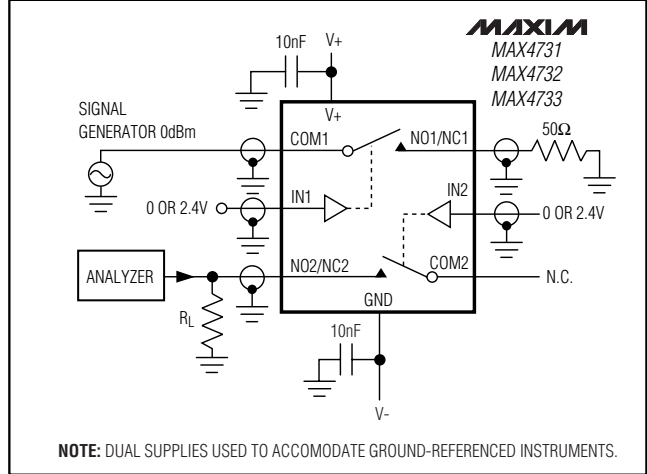


Figure 6. Crosstalk

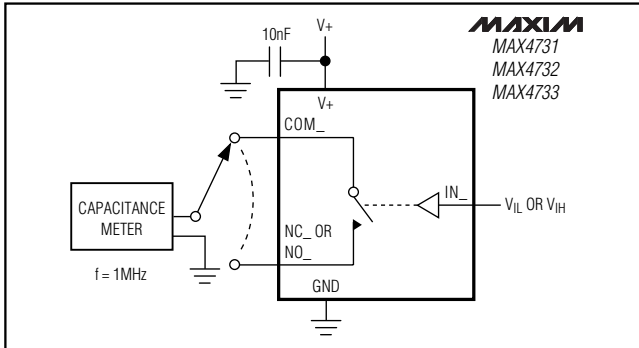


Figure 7. Channel Off/On-Capacitance

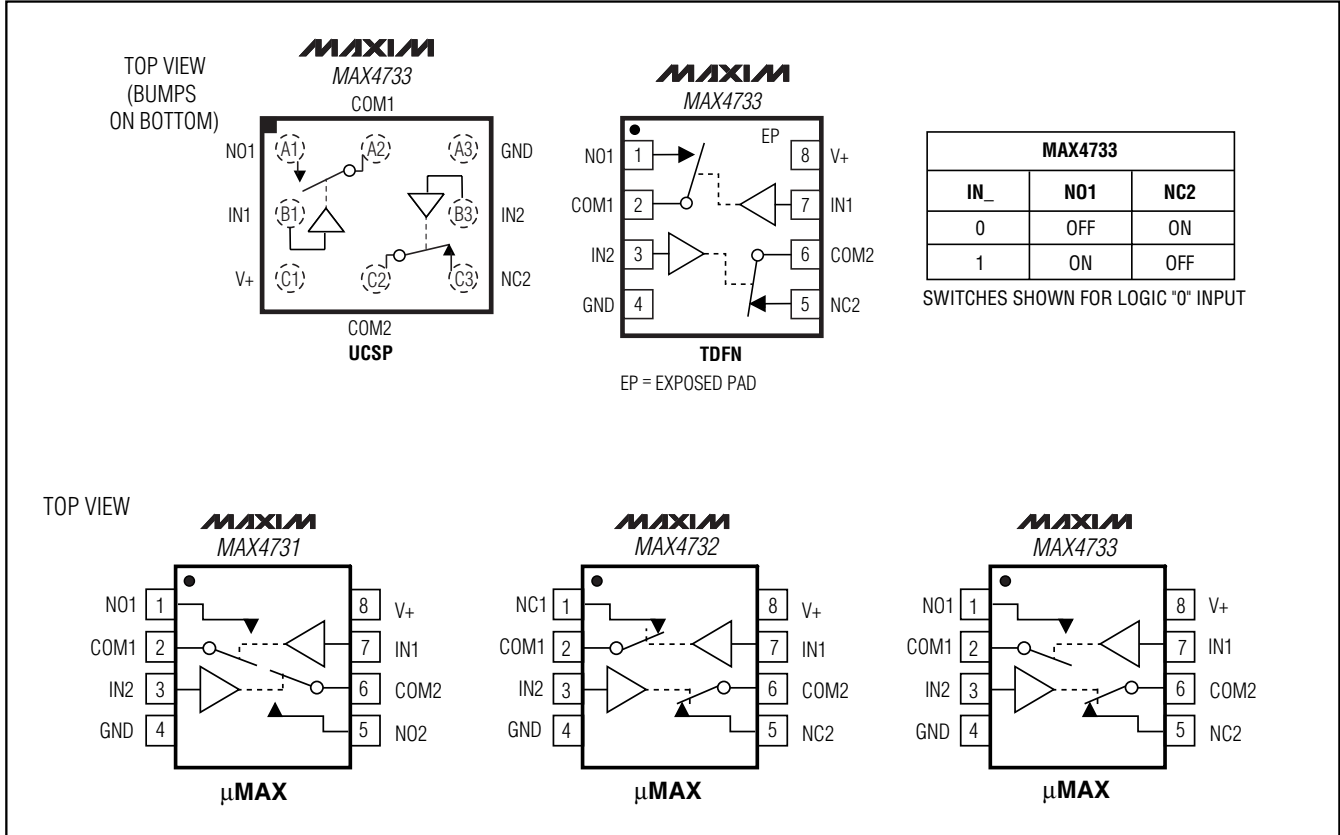
Chip Information

TRANSISTOR COUNT: 68

PROCESS: CMOS

50Ω, Dual SPST Analog Switches in UCSP

Pin Configurations/Functional Diagrams/Truth Tables (continued)



MAX4731/MAX4732/MAX4733

50Ω, Dual SPST Analog Switches in UCSP

Package Information

(The package drawing(s) in this data sheet may not reflect the most current specifications. For the latest package outline information go to www.maxim-ic.com/packages.)

TOP VIEW

COMMON DIMENSIONS	
A	0.62±0.05-0.08
A1	0.29±0.02
A2	0.33 REF.
b	∅0.35±0.03
D1	1.00 BASIC
E1	1.00 BASIC
e	0.50 BASIC
SD	0.00 BASIC
SE	0.00 BASIC

PKG. CODE	VARIABLE DIMENSIONS		DEPOPULATED SOLDER BALLS
	D	E	
B9-1	1.52±0.05	1.52±0.05	NONE
B9-2	1.52±0.05	1.52±0.05	B2
B9-3	1.52±0.05	1.52±0.05	B1, B2, B3
B9-4	1.60±0.05	1.60±0.05	NONE
B9-5	1.60±0.05	1.60±0.05	B2
B9-6	1.60±0.05	1.60±0.05	B1, B2, B3
B9-7	1.52±0.05	1.52±0.05	A2, B1, B2, B3, C2

NOTES:

- ALL DIMENSIONS ARE IN MILLIMETERS.
- PRODUCT MARKING: NUMBER OF CHARACTERS AND LINES VARY PER PRODUCT.

SIDE VIEW

BOTTOM VIEW

DALLAS SEMICONDUCTOR **MAXIM**

TITLE: PACKAGE OUTLINE, 3x3 UCSP

APPROVAL	DOCUMENT CONTROL NO. 21-0093	REV. K	1/1
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-DRAWING NOT TO SCALE-

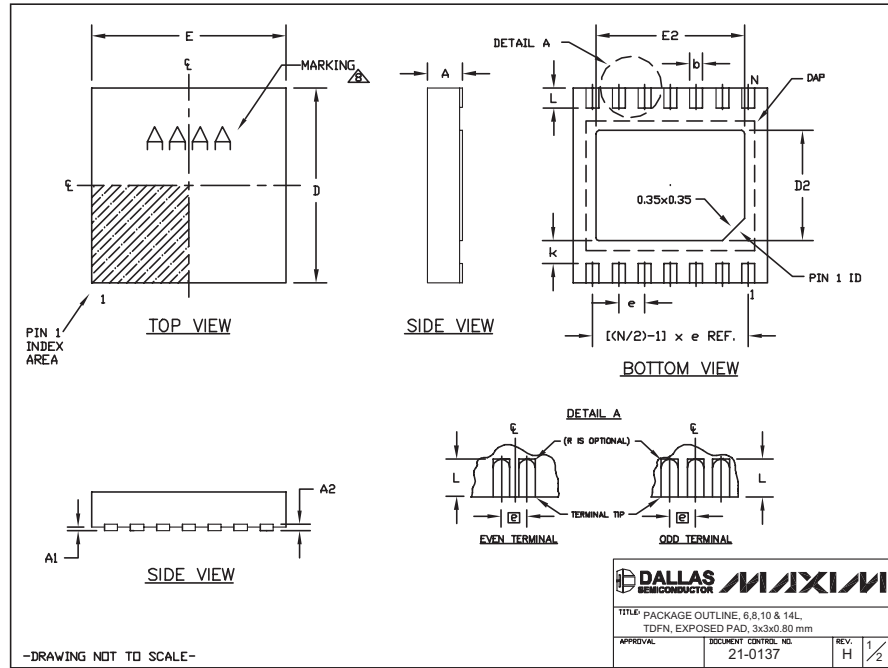
9LUCSP, 3x3 EPS

50Ω, Dual SPST Analog Switches in UCSP

Package Information (continued)

(The package drawing(s) in this data sheet may not reflect the most current specifications. For the latest package outline information go to www.maxim-ic.com/packages.)

MAX4731/MAX4732/MAX4733



COMMON DIMENSIONS			PACKAGE VARIATIONS							
SYMBOL	MIN.	MAX.	PKG. CODE	N	D2	E2	e	JEDEC SPEC	b	[(N/2)-1] x e
A	0.70	0.80	T633-1	6	1.50-0.10	2.30-0.10	0.95 BSC	MO229 / WEEA	0.40-0.05	1.90 REF
D	2.90	3.10	T633-2	6	1.50-0.10	2.30-0.10	0.95 BSC	MO229 / WEEA	0.40-0.05	1.90 REF
E	2.90	3.10	T833-1	8	1.50-0.10	2.30-0.10	0.65 BSC	MO229 / WEEC	0.30-0.05	1.95 REF
A1	0.00	0.05	T833-2	8	1.50-0.10	2.30-0.10	0.65 BSC	MO229 / WEEC	0.30-0.05	1.95 REF
L	0.20	0.40	T833-3	8	1.50-0.10	2.30-0.10	0.65 BSC	MO229 / WEEC	0.30-0.05	1.95 REF
k	0.25 MIN.		T1033-1	10	1.50-0.10	2.30-0.10	0.50 BSC	MO229 / WEED-3	0.25-0.05	2.00 REF
A2	0.20 REF.		T1033-2	10	1.50-0.10	2.30-0.10	0.50 BSC	MO229 / WEED-3	0.25-0.05	2.00 REF
			T1433-1	14	1.70-0.10	2.30-0.10	0.40 BSC	----	0.20-0.05	2.40 REF
			T1433-2	14	1.70-0.10	2.30-0.10	0.40 BSC	----	0.20-0.05	2.40 REF

NOTES:
 1. ALL DIMENSIONS ARE IN mm. ANGLES IN DEGREES.
 2. COPLANARITY SHALL NOT EXCEED 0.08 mm.
 3. WARPAGE SHALL NOT EXCEED 0.10 mm.
 4. PACKAGE LENGTH/PACKAGE WIDTH ARE CONSIDERED AS SPECIAL CHARACTERISTIC(S).
 5. DRAWING CONFORMS TO JEDEC MO229, EXCEPT DIMENSIONS "D2" AND "E2", AND T1433-1 & T1433-2.
 6. "N" IS THE TOTAL NUMBER OF LEADS.
 7. NUMBER OF LEADS SHOWN ARE FOR REFERENCE ONLY.
 8. MARKING IS FOR PACKAGE ORIENTATION REFERENCE ONLY.

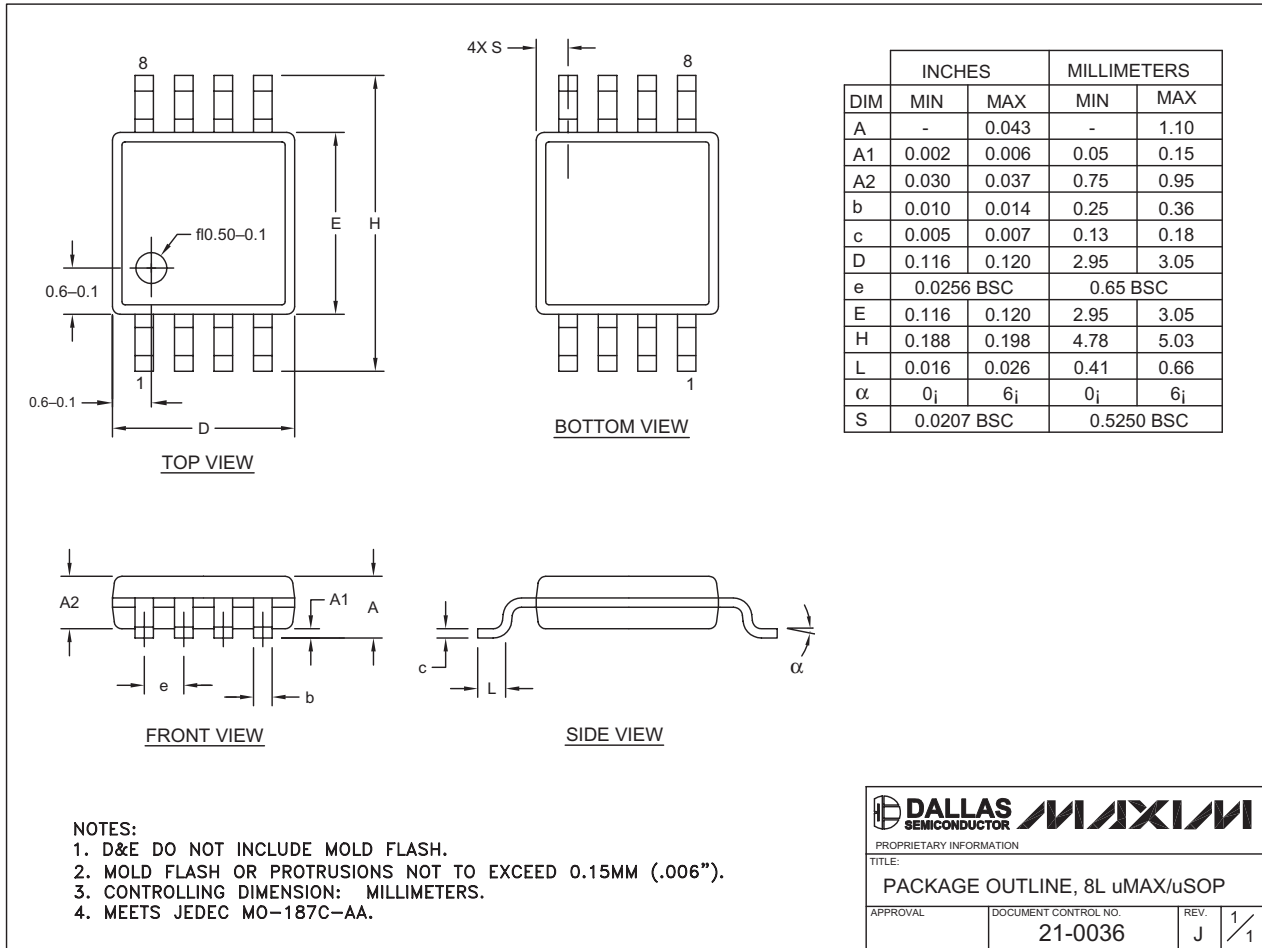
DALLAS SEMICONDUCTOR		MAXIM	
TITLE: PACKAGE OUTLINE, 6, 8, 10 & 14L, DFN, EXPOSED PAD, 3x3x0.80 mm			
APPROVAL:	DOCUMENT CONTROL NO. 21-0137	REV. H	2/2

-DRAWING NOT TO SCALE-

50Ω, Dual SPST Analog Switches in UCSP

Package Information (continued)

(The package drawing(s) in this data sheet may not reflect the most current specifications. For the latest package outline information go to www.maxim-ic.com/packages.)



8LUMAXDEPS

Revision History

Pages changed at Rev 2: 1, 2, 7, 8, 11, 14

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