Absolute Maximum Ratings

V_{DD}, CPVDD to SGND .....-0.3V to +6V
V_{SS}, CPVSS to SGND .....+0.3V to -6V
V_{DD} to CPVDD.....-0.3V to +0.3V
V_{SS} to CPVSS.....-0.3V to +0.3V
$\overline{SHDN}$, DIAG to SGND.....-0.3V to (V_{DD} + 0.3V)
OUT_ to PGND .....(V_{CPVSS} - 0.3V) to +45V
IN_ to SGND (MAX13330).....(V_{SS} - 0.3V) to (V_{DD} + 0.3V)
IN_ to SGND (MAX13331).....-0.3V to (V_{DD} + 0.3V)
C1P to PGND.....-0.3V to (V_{CPVDD} + 0.3V)
C1N to PGND.....(V_{SS} - 0.3V) to +0.3V
Output Short-Circuit Duration.....Continuous
Continuous Power Dissipation (T_A = +70°C)
QSOP (derate 9.6mW/°C above +70°C))).....771.5mW
Operating Temperature Range..... -40°C to +105°C
Junction Temperature.....+150°C
Storage Temperature Range..... -65°C to +150°C
Lead Temperature (soldering, 10s) .....+300°C
Soldering Temperature (reflow).....+260°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Package Thermal Characteristics (Note 1)

QSOP
Junction-to-Ambient Thermal Resistance (θ_{JA}) .....103.7°C/W
Junction-to-Case Thermal Resistance (θ_{JC}).....37°C/W

Note 1: Package thermal resistances were obtained using the method described in JEDEC specification JESD51-7, using a four-layer board. For detailed information on package thermal considerations, refer to **www.maximintegrated.com/thermal-tutorial**.

Electrical Characteristics

(V_{DD} = V_{CPVDD} = +5V, V_{SGND} = V_{PGND} = 0V, $\overline{SHDN}$ = V_{DD}, C1 = C2 = 1µF, R_L = ∞, resistive load referenced to ground, for MAX13330 gain = -1.5V/V (internally set), for MAX13331 gain = -1.5V/V (R_{IN} = 30kΩ, R_{FB} = 45kΩ), T_A = T_J = -40°C to +105°C, unless otherwise noted. Typical values are at T_A = +25°C, unless otherwise noted.) (Note 2)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
GENERAL							
Amplifier Supply Voltage Range	V_{DD}			4.0		5.5	V
Charge-Pump Supply Voltage Range	V_{CPVDD}			4.0		5.5	V
Charge-Pump Output Voltage	V_{CPVSS}				-V_{DD}		V
Quiescent Supply Current	I_{DD}	R_L = ∞			10		mA
Shutdown Supply Current	$I_{\overline{SHDN}}$					10	µA
$\overline{SHDN}$ Input-Logic High	V_{IH}			2			V
$\overline{SHDN}$ Input-Logic Low	V_{IL}					0.8	V
$\overline{SHDN}$ Input Leakage Current				-1		+1	µA
$\overline{SHDN}$ to Full Operation Time	t_{SON}				100		µs
DIAGNOSTICS							
Diagnostic Output Voltage	V_{DIAG}	R_{DIAG} = ∞, T_A = +25°C	No fault			0.02 x V_{DD}	V
			OUTR short to SGND	0.22 x V_{DD}	0.25 x V_{DD}	0.28 x V_{DD}	
			OUTL short to SGND	0.47 x V_{DD}	0.50 x V_{DD}	0.53 x V_{DD}	
			OUTR short to V_{BAT}	0.72 x V_{DD}	0.75 x V_{DD}	0.78 x V_{DD}	
			OUTL short to V_{BAT}	0.97 x V_{DD}			

Electrical Characteristics (continued)

(V_{DD} = V_{CPVDD} = +5V, V_{SGND} = V_{PGND} = 0V, $\overline{SHDN}$ = V_{DD}, C1 = C2 = 1µF, R_L = ∞, resistive load referenced to ground, for MAX13330 gain = -1.5V/V (internally set), for MAX13331 gain = -1.5V/V (R_{IN} = 30kΩ, R_{FB} = 45kΩ), T_A = T_J = -40°C to +105°C, unless otherwise noted. Typical values are at T_A = +25°C, unless otherwise noted.) (Note 2)

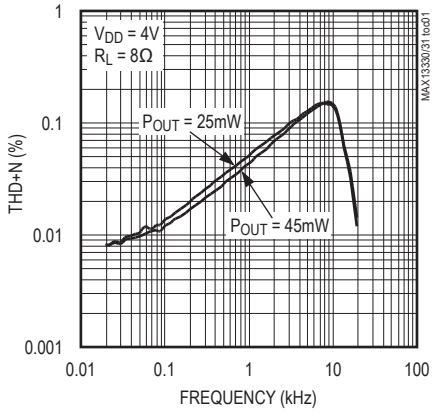
PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
Short-to-SGND Threshold				130			mA
Short-to-V_{BAT} Threshold				130			mA
AMPLIFIERS							
Voltage Gain	A_V	MAX13330		-1.48	-1.5	-1.52	V/V
Gain Matching		MAX13330			±0.2		%
Input Offset Voltage					±1	±6	mV
Input Bias Current		$V_{IN\_}$ = 0V			50		nA
Input Impedance	R_{IN}	MAX13330		20	30		kΩ
Power-Supply Rejection Ratio	PSRR	DC, V_{DD} = 4.0V to 5.5V, input referred			-86		dB
		f =1kHz, V_{RIPPLE} = 100mV_{P-P}			-80		
Output Power Per Channel	$P_{OUT\_}$	THD+N = 1%; V_{DD} = V_{CPVDD} = 5V; f_{IN} = 1kHz	R_L = 8Ω		75		mW
			R_L = 16Ω		120		
			R_L = 32Ω		135		
Output Voltage	$V_{OUT\_}$	R_L = 1kΩ			2		V_{RMS}
Output Impedance in Shutdown					14		kΩ
Total Harmonic Distortion Plus Noise	THD+N	R_L = 16Ω, P_{OUT} = 100mW, f = 1kHz			0.03		%
		R_L = 32Ω, P_{OUT} = 125mW, f = 1kHz			0.01		%
Signal-to-Noise Ratio	SNR	R_L = 32Ω, P_{OUT} = 135mW, f = 22Hz to 22kHz			100		dB
Noise	V_n	f = 22Hz to 22kHz bandwidth; inputs AC-coupled to grounded			6		$µV_{RMS}$
Slew Rate	SR				0.3		V/µs
Maximum Capacitive Load	C_L	No sustained oscillation				3000	pF
Click-and-Pop Level	K_{CP}	Peak voltage, T_A = +25°C, A-weighted, 32 samples per second; Inputs AC-coupled to ground	Into shutdown		-80		dB
			Out of shutdown		-60		
Charge-Pump Oscillator Frequency	f_{OSC}			1.9	2.2	2.5	MHz
Crosstalk		R_L = 32Ω, V_{IN} = 200mV_{P-P}, f = 10kHz			-75		dB
Thermal-Shutdown Temperature					+155		°C
Thermal-Shutdown Hysteresis					10		°C
ESD Protection		Human Body Model (OUTR and OUTL)			±15		kV

Note 2: All devices are 100% tested at T_A = +25°C; specifications over temperature limits are guaranteed by design and QA sampling.

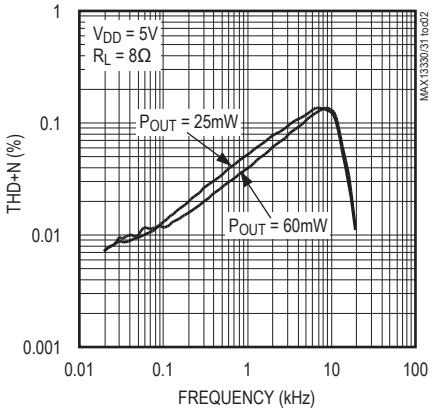
Typical Operating Characteristics

(V_{DD} = V_{CPVDD} = 5V, V_{SGND} = V_{PGND} = 0V, C1 = C2 = 1µF, R_L = ∞, gain = -1.5V/V, THD+N measurement bandwidth = 22Hz to 22kHz, T_A = +25°C, unless otherwise noted.)

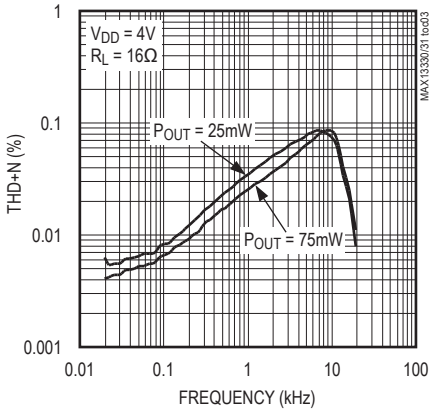
TOTAL HARMONIC DISTORTION PLUS NOISE vs. FREQUENCY



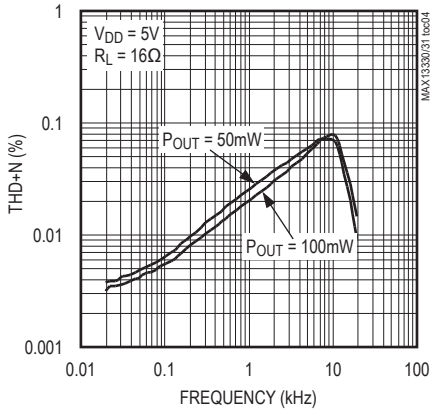
TOTAL HARMONIC DISTORTION PLUS NOISE vs. FREQUENCY



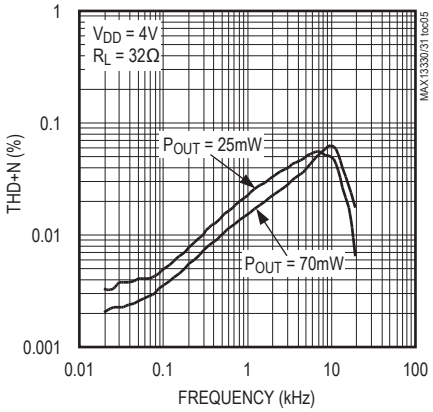
TOTAL HARMONIC DISTORTION PLUS NOISE vs. FREQUENCY



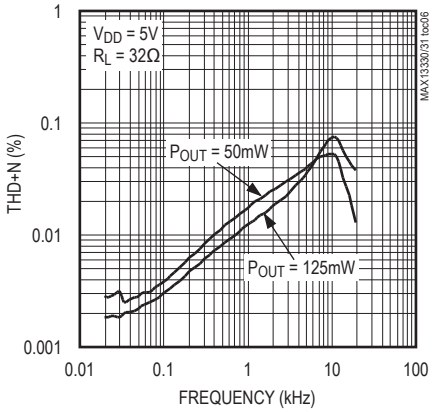
TOTAL HARMONIC DISTORTION PLUS NOISE vs. FREQUENCY



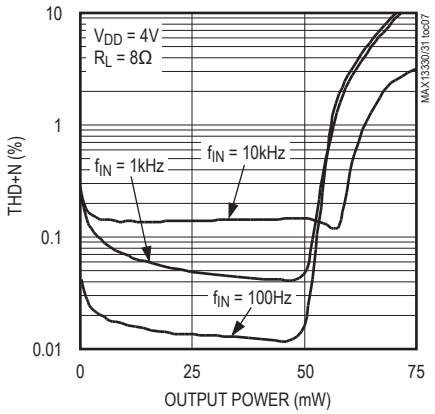
TOTAL HARMONIC DISTORTION PLUS NOISE vs. FREQUENCY



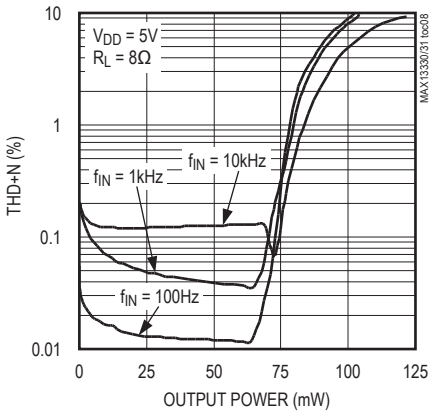
TOTAL HARMONIC DISTORTION PLUS NOISE vs. FREQUENCY



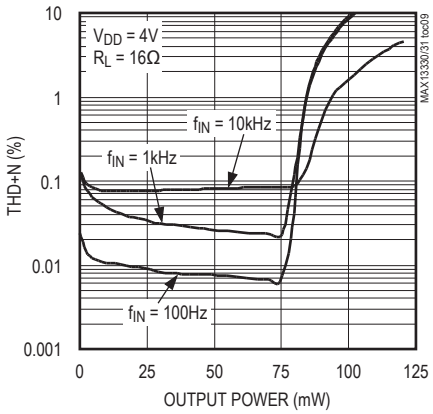
TOTAL HARMONIC DISTORTION PLUS NOISE vs. OUTPUT POWER



TOTAL HARMONIC DISTORTION PLUS NOISE vs. OUTPUT POWER



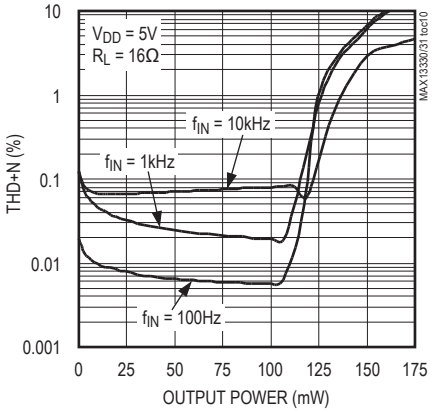
TOTAL HARMONIC DISTORTION PLUS NOISE vs. OUTPUT POWER



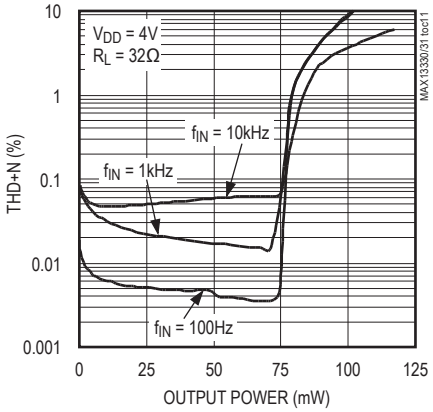
Typical Operating Characteristics (continued)

(V_{DD} = V_{CPVDD} = 5V, V_{SGND} = V_{PGND} = 0V, C1 = C2 = 1µF, R_L = ∞, gain = -1.5V/V, THD+N measurement bandwidth = 22Hz to 22kHz, T_A = +25°C, unless otherwise noted.)

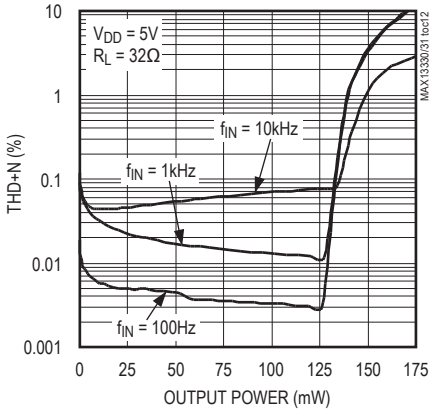
TOTAL HARMONIC DISTORTION PLUS NOISE vs. OUTPUT POWER



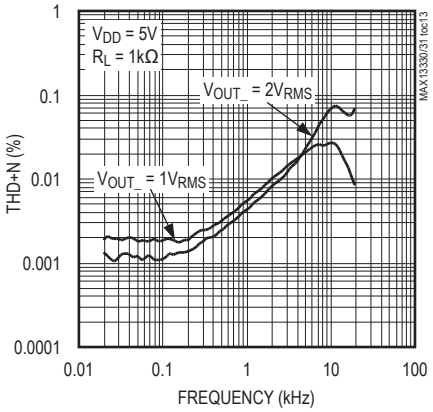
TOTAL HARMONIC DISTORTION PLUS NOISE vs. OUTPUT POWER



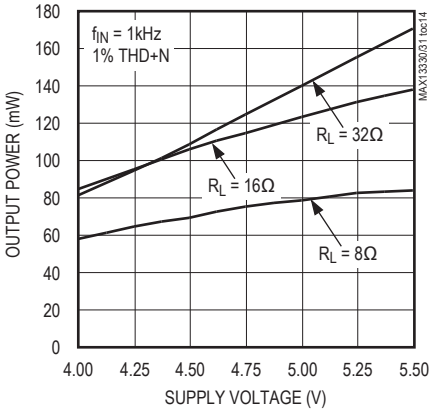
TOTAL HARMONIC DISTORTION PLUS NOISE vs. OUTPUT POWER



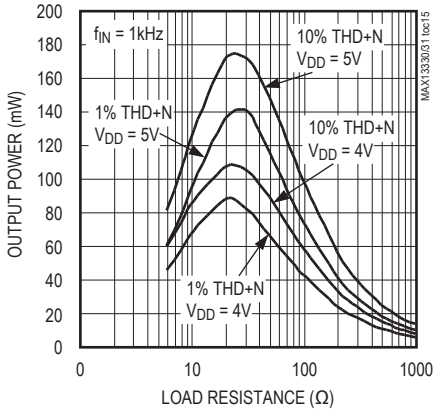
TOTAL HARMONIC DISTORTION PLUS NOISE vs. FREQUENCY



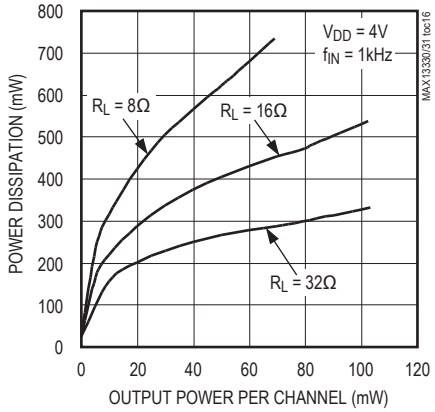
OUTPUT POWER vs. SUPPLY VOLTAGE



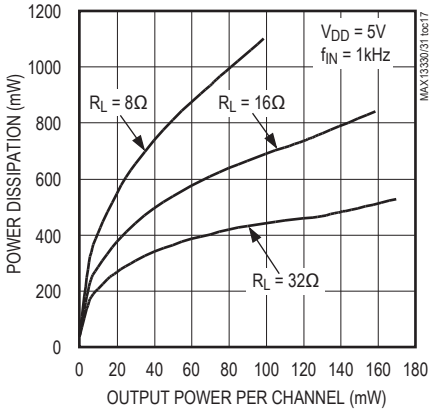
OUTPUT POWER vs. LOAD RESISTANCE



POWER DISSIPATION vs. OUTPUT POWER PER CHANNEL



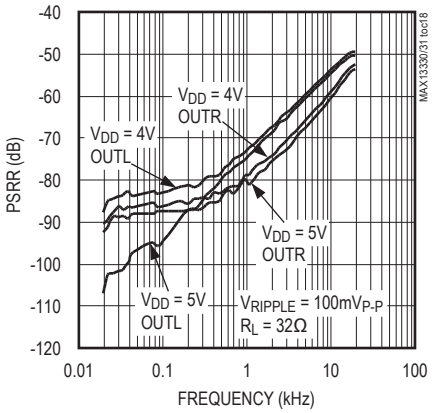
POWER DISSIPATION vs. OUTPUT POWER PER CHANNEL



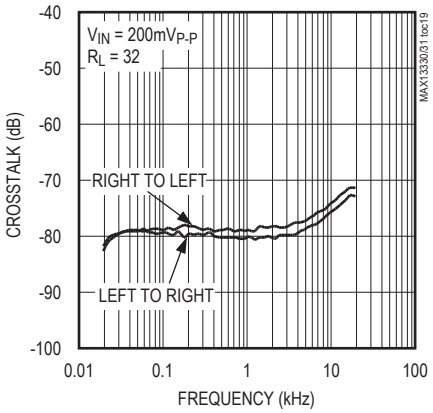
Typical Operating Characteristics (continued)

(V_{DD} = V_{CPVDD} = 5V, V_{SGND} = V_{PGND} = 0V, C1 = C2 = 1µF, R_L = ∞, gain = -1.5V/V, THD+N measurement bandwidth = 22Hz to 22kHz, T_A = +25°C, unless otherwise noted.)

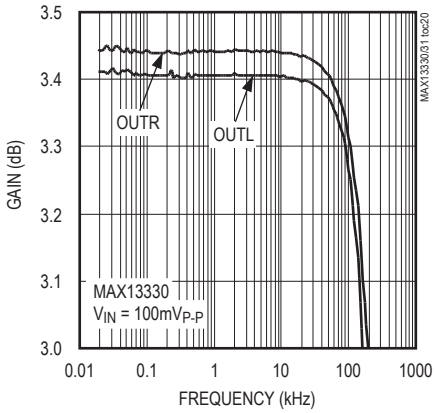
POWER-SUPPLY REJECTION RATIO vs. FREQUENCY



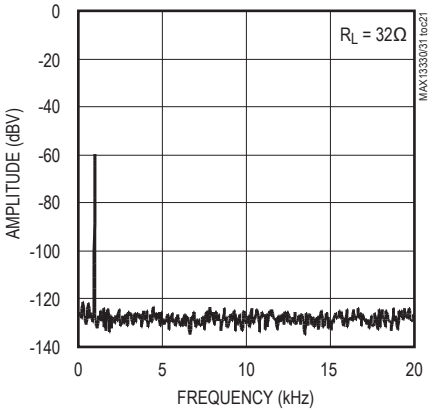
CROSSTALK vs. FREQUENCY



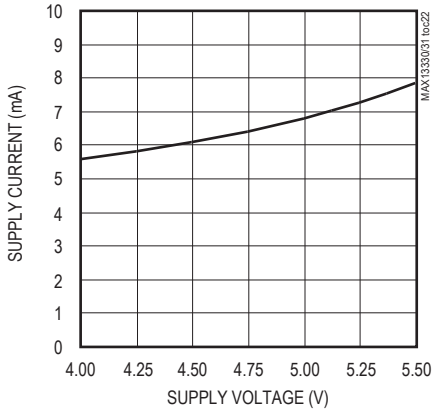
GAIN FLATNESS vs. FREQUENCY



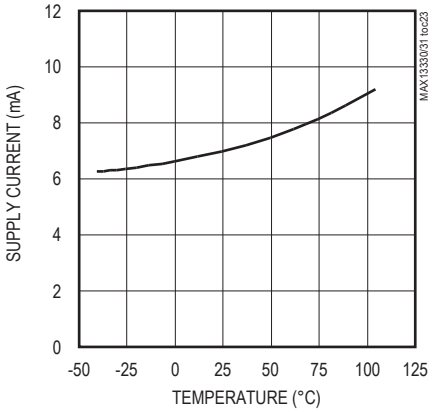
OUTPUT FFT



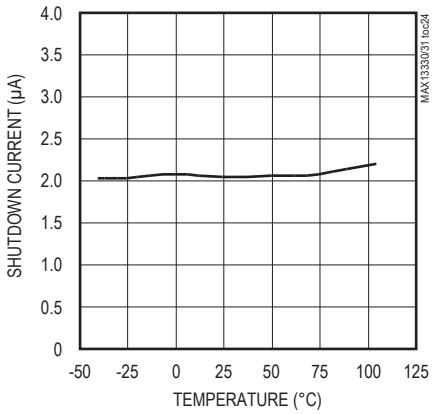
SUPPLY CURRENT vs. SUPPLY VOLTAGE



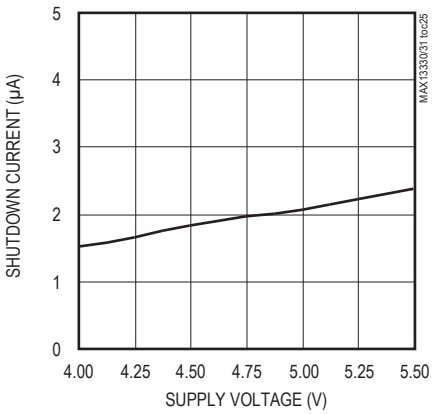
SUPPLY CURRENT vs. TEMPERATURE



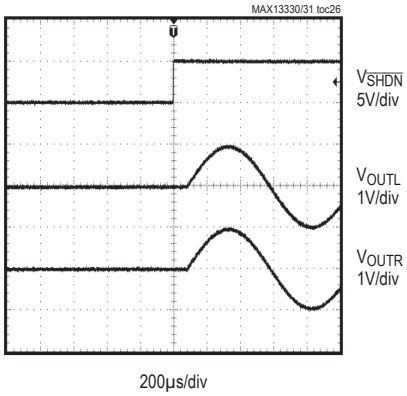
SHUTDOWN CURRENT vs. TEMPERATURE



SHUTDOWN CURRENT vs. SUPPLY VOLTAGE



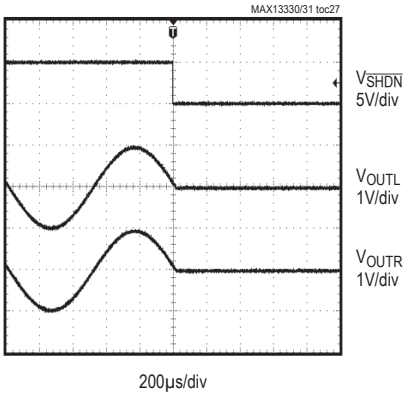
EXITING SHUTDOWN TRANSIENT



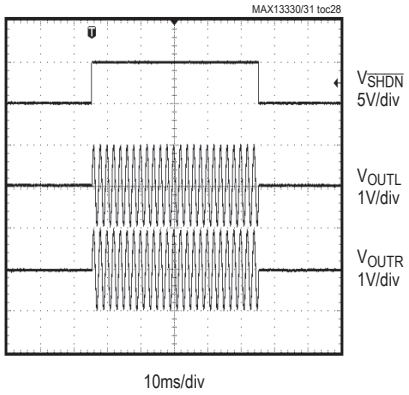
Typical Operating Characteristics (continued)

(V_{DD} = V_{CPVDD} = 5V, V_{SGND} = V_{PGND} = 0V, C1 = C2 = 1µF, R_L = ∞, gain = -1.5V/V, THD+N measurement bandwidth = 22Hz to 22kHz, T_A = +25°C, unless otherwise noted.)

ENTERING SHUTDOWN TRANSIENT



POWER-UP/-DOWN TRANSIENT



Pin Description

PIN	NAME	FUNCTION
1	INL	Inverting Left-Channel Audio Input
2, 4	SGND	Amplifier Signal Ground. The noninverting inputs of the amplifiers are connected to the amplifier signal ground. Connect both to the signal ground plane.
3	INR	Inverting Right-Channel Audio Input
5	V_{DD}	Amplifier Positive-Power Supply. Connect to positive supply. Bypass with a 1µF capacitor to SGND as close to the pin as possible.
6	$\overline{SHDN}$	Active-Low Shutdown Input
7	CPVDD	Charge-Pump Power Supply. Powers charge-pump inverter, charge-pump logic, and oscillator. Connect to positive supply. Bypass with a 1µF capacitor to PGND as close to the pin as possible.
8	C1P	Flying-Capacitor Positive Terminal. Connect a 1µF capacitor between C1P and C1N.
9, 15	PGND	Power Ground. Connect both to the power ground plane.
10	C1N	Flying-Capacitor Negative Terminal. Connect a 1µF capacitor between C1P and C1N.
11	CPVSS	Charge-Pump Output. Connect to V_{SS} and bypass with a 1µF capacitor to PGND.
12	DIAG	Diagnostic Voltage Output
13	OUTR	Right-Channel Output
14	V_{SS}	Amplifier Negative Power Supply. Connect to CPVSS.
16	OUTL	Left-Channel Output

Detailed Description

The MAX13330/MAX13331 headphone amplifiers feature Maxim's DirectDrive architecture, eliminating the large output-coupling capacitors required by conventional single-supply headphone amplifiers. The devices consists of two Class AB headphone amplifiers, under-voltage lockout (UVLO), low-power shutdown control, comprehensive click-and-pop suppression, output short-circuit/ESD protection and output short-circuit diagnostics.

These devices can drive loads as low as 8Ω, and deliver up to 120mW per channel into 16Ω and 135mW into 32Ω. The MAX13330 features a fixed gain of -1.5V/V, and the MAX13331 features a programmable gain configured with external resistors. The headphone outputs feature ±15kV Human Body Model ESD protection, and enhanced short-circuit protection to ground or battery (V_{BAT} up to +45V). An integrated short-circuit diagnostic output provides the status of the MAX13330/MAX13331 during operation as a fraction of the analog supply voltage.

DirectDrive

Conventional single-supply headphone amplifiers have their outputs biased about a nominal DC voltage (typically half the supply) for maximum dynamic range. Large coupling capacitors are needed to block this DC bias from the headphone. Without these capacitors, a significant amount of DC current flows to the headphone, resulting in unnecessary power dissipation and possible damage to both the headphone and the headphone amplifier.

Maxim's DirectDrive architecture uses a charge pump to create an internal negative-supply voltage, allowing the MAX13330/MAX13331 outputs to be biased about SGND (Figure 1). With no DC component, there is no need for the large DC-blocking capacitors. Instead of two large (220µF, typ) tantalum capacitors, the MAX13330/MAX13331 charge pump requires two small ceramic capacitors, conserving board space, reducing cost, and improving the frequency response of the headphone amplifier. See the Output Power vs. Load Resistance graph in the *Typical Operating Characteristics* for details of the possible capacitor sizes. There is a low DC voltage on the amplifier outputs due to amplifier offset. However, the output offset of the MAX13330 is typically ±2.5mV which, when combined with a 32Ω load, results in less than ±78µA of DC current flow to the headphones. Previous attempts to eliminate the output-coupling capacitors involved biasing the headphone return (sleeve) to the DC-bias voltage of the headphone amplifiers.

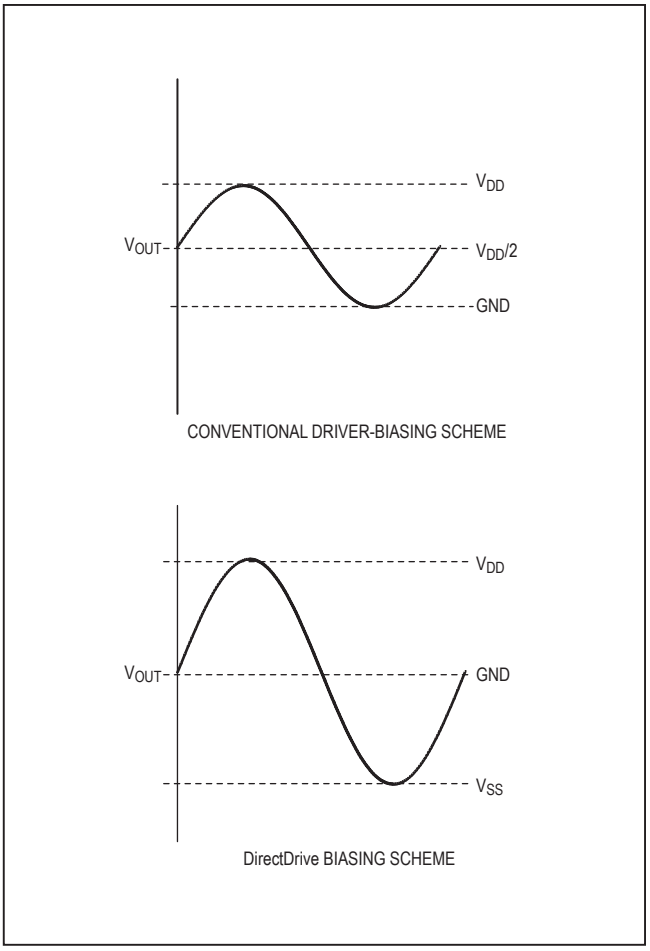


Figure 1. Conventional Driver Output Waveform vs. MAX13330/MAX13331 Output Waveform

This method raises some issues:

- The sleeve is typically grounded to the chassis. Using this biasing approach, the sleeve must be isolated from system ground, complicating product design.
- During an ESD strike, the amplifier's ESD structures are the only path to system ground. Thus, the amplifier must be able to withstand the full ESD strike.
- When using the headphone jack as a line out to other equipment, the bias voltage on the sleeve may conflict with the ground potential from other equipment, resulting in possible damage to the amplifiers.

Low-Frequency Response

In addition to the cost and size disadvantages of the DCblocking capacitors required by conventional headphone amplifiers, these capacitors limit the amplifier's low-frequency response and can distort the audio signal:

1) The impedance of the headphone load and the DC-blocking capacitor form a highpass filter with the -3dB point set by:

$$f_{-3dB} = \frac{1}{2\pi \times R_L \times C_{OUT}} (Hz)$$

where R_L is the impedance of the headphone and C_{OUT} is the value of the DC-blocking capacitor. The highpass filter is required by conventional singleended, single power-supply headphone amplifiers to block the midrail DC-bias component of the audio signal from the headphones. The drawback to the filter is that it can attenuate low-frequency signals. Larger values of C_{OUT} reduce this effect but result in physically larger, more expensive capacitors. Figure 2 shows the relationship between the size of C_{OUT} and the resulting low-frequency attenuation. Note that the -3dB point for a 16Ω headphone with a 100µF blocking capacitor is 100Hz, well within the normal audio band, resulting in low-frequency attenuation of the reproduced signal.

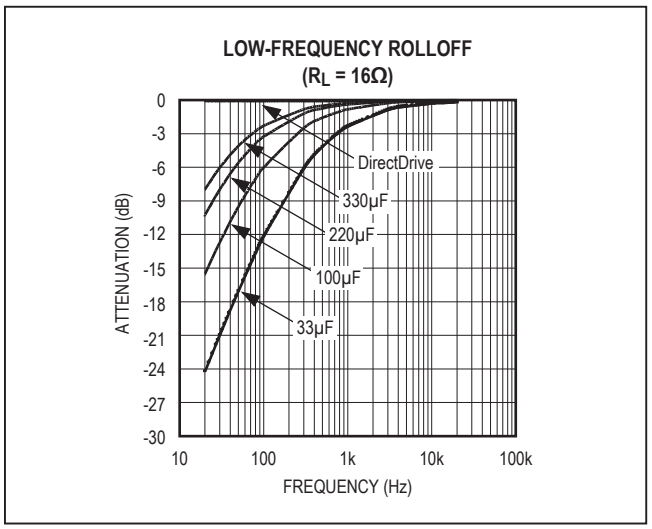


Figure 2. Low-Frequency Attenuation for Common DC-Blocking Capacitor Values

2) The voltage coefficient of the DC-blocking capacitor contributes distortion to the reproduced audio signal as the capacitance value varies and the function of the voltage across the capacitor changes. The reactance of the capacitor dominates at frequencies below the -3dB point and the voltage coefficient appears as frequency-dependent distortion. Figure 3 shows the THD+N introduced by two different capacitor dielectric types. Note that below 100Hz, THD+N increases rapidly. The combination of low-frequency attenuation and frequency-dependent distortion compromises audio reproduction in portable audio equipment that emphasizes low-frequency effects such as in multimedia laptops, MP3, CD, and DVD players. By eliminating the DC-blocking capacitors through DirectDrive technology, these capacitor-related deficiencies are eliminated.

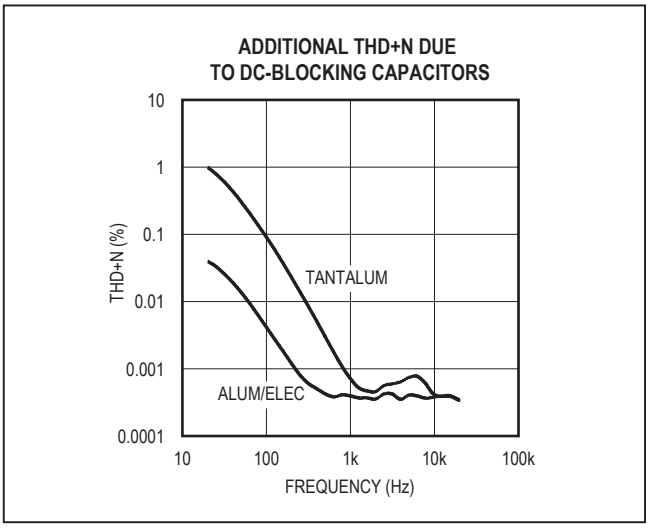


Figure 3. Distortion Contributed by DC-Blocking Capacitors

Charge Pump

The MAX13330/MAX13331 feature a low-noise charge pump. The 2.2MHz (typ) switching frequency is well beyond the audio range. It does not interfere with the audio signals and avoids AM band interference. The switch drivers feature a controlled switching speed that minimizes noise generated by turn-on and turn-off transients. By limiting the switching speed of the charge pump, the di/dt noise caused by the parasitic bond wire and trace inductance is minimized. Although not typically required, additional high-frequency noise attenuation can be achieved by increasing the value of C2 (see the *Typical Application Circuits*).

Diagnostic Output

The MAX13330/MAX13331 provides an analog diagnostic output as a fraction of the analog supply voltage V_{DD}. The voltage at DIAG will correspond to the fault condition with the highest priority that is present in the system, as shown in Table 1. When simultaneous fault conditions occur on both headphone outputs, the diagnostic output will only report the fault condition at OUTR until it is cleared or removed. Only then will the fault condition at OUTL be reported at DIAG. Connect DIAG to a high-impedance input.

Table 1. MAX13330/MAX13331 Diagnostic Priority

V_{DIAG}	STATE	PRIORITY
V_{DD}	OUTL Short to V_{BAT}	3
3/4 V_{DD}	OUTR Short to V_{BAT}	1
1/2 V_{DD}	OUTL Short to SGND	4
1/4 V_{DD}	OUTR Short to SGND	2
0	No Fault	5
Three State	Shutdown	—

For both headphone outputs, short circuits to V_{BAT} are dynamic and V_{DIAG} will be automatically cleared as soon as the fault condition is removed. Short circuits to GND occurring when a positive output voltage is present on OUTL or OUTR, will result in V_{DIAG} being latched until the fault condition is cleared.

When V_{DIAG} is latched, it can be cleared by either toggling $\overline{SHDN}$ low for less than 5µs or initiating a full reset of the MAX13330/MAX13331. Toggling $\overline{SHDN}$ low for less than 5µs will cause the fault to ground to be cleared without shutting down the device or interrupting the output state of the amplifiers. A full reset requires $\overline{SHDN}$ to be pulled low for more than 50µs. The amplifier outputs will enter high impedance and remain in that state until the device exits shutdown.

Click-and-Pop Suppression

In conventional single-supply audio amplifiers, the output-coupling capacitor is a major contributor of audible clicks and pops. Upon startup, the amplifier charges the coupling capacitor to its bias voltage, typically half the supply. Likewise, on shutdown, the capacitor is discharged to $\overline{SGND}$. This results in a DC shift across the capacitor which appears as an audible transient at the speaker. Since the MAX13330/MAX13331 does not require output-coupling capacitors, this problem does not arise.

Additionally, the MAX13330/MAX13331 feature extensive click-and-pop suppression that eliminates any audible transient sources internal to the device. The Power-Up/-Down Transient graph in the *Typical Operating Characteristics* shows that there is minimal DC shift and no spurious transients at the output upon startup or shutdown.

In most applications, the output of the preamplifier driving the MAX13330/MAX13331 has a DC bias of typically half the supply. At startup, the input-coupling capacitor is charged to the preamplifier's DC-bias voltage through the feedback resistor of the MAX13330/MAX13331, resulting in a DC shift across the capacitor and an audible click/pop. Delaying the rise of $\overline{SHDN}$ 4 to 5 time constants (80ms to 100ms) based on R_{IN} and C_{IN} relative to the startup of the preamplifier, eliminates this click/pop caused by the input filter.

Shutdown

The MAX13330/MAX13331 feature shutdown control allowing audio signals to be shut down or muted.

Driving $\overline{SHDN}$ low disables the amplifiers and the charge pump, sets the amplifier output impedance to 14kΩ (typ), and reduces the supply current. In shutdown mode, the supply current is reduced to 2µA. The charge pump is enabled once $\overline{SHDN}$ is driven high.

Applications Information

Power Dissipation

Under normal operating conditions, linear power amplifiers can dissipate a significant amount of power. The maximum power dissipation for each package is given in the *Absolute Maximum Ratings* section under continuous power dissipation or can be calculated by the following equation:

$$P_{DISSPKG(MAX)} = \frac{\left(T_{J(MAX)} - T_A\right)}{\theta_{JA}}$$

where $T_{J(MAX)}$ is +145°C, T_A is the ambient temperature, and θ_{JA} is the reciprocal of the derating factor in °C/W as specified in the *Absolute Maximum Ratings* section. The thermal resistance θ_{JA} of the QSOP package is 120°C/W.

The MAX13330/MAX13331 have two power dissipation sources: the charge pump and two amplifiers. If power dissipation for a given application exceeds the maximum allowed for a particular package, either reduce V_{DD}, increase load impedance, decrease the ambient temperature, or add heatsinking to the device. Large output, supply, and ground traces improve the maximum power dissipation in the package.

Thermal-overload protection limits total power dissipation in the MAX13330/MAX13331. When the junction temperature exceeds +145°C (typ), the thermal-protection circuitry disables the amplifier output stage. The amplifiers are enabled once the junction temperature cools by 5°C. This results in a pulsing output under continuous thermal-overload conditions.

Output Power

The device has been specified for the worst-case scenario, when both inputs are in-phase. Under this condition, the amplifiers simultaneously draw current from the charge pump, leading to a proportional reduction in V_{SS} headroom. In typical stereo audio applications, the left and right signals have differences in both magnitude and phase, subsequently leading to an increase in the maximum attainable output power. Figure 4 shows the two extreme cases for in- and out-of-phase. In reality, the available power lies between these extremes.

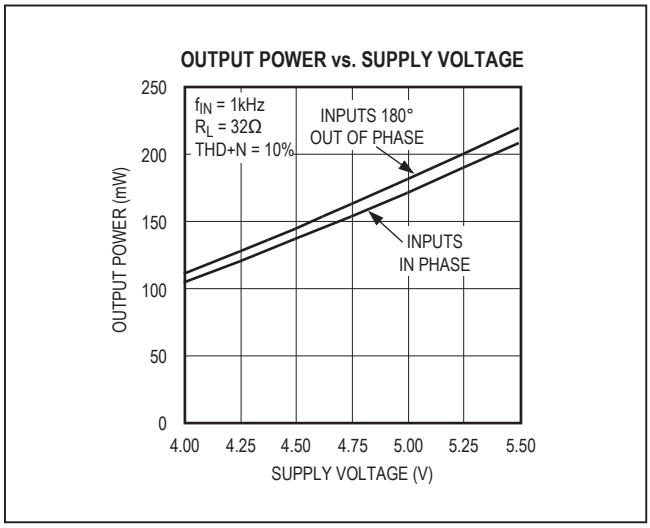


Figure 4. Output Power vs. Supply Voltage

UVLO

The MAX13330/MAX13331 feature a UVLO function that prevents the device from operating if the supply voltage is less than 3.6V (typ). This feature ensures proper operation during brownout conditions and prevents deep battery discharge. Once the supply voltage reaches the UVLO threshold, the charge-pump is turned on and the amplifiers are powered.

Component Selection

Gain-Setting Resistors (MAX13331 Only)

The gain of the MAX13330 is internally set at -1.5V/V. All gain-setting resistors are integrated into the device, reducing external component count. The internally set gain, in combination with DirectDrive, results in a headphone amplifier that requires only five tiny 1µF capacitors to complete the amplifier circuit: two for the charge-pump, two for audio input coupling, and one for power-supply bypassing (see the *Typical Application Circuits*). The gain of the MAX13331 amplifier is set externally as shown in the *Typical Application Circuits*, the gain is:

$$A_V = -\frac{R_F}{R_{IN}} (V/V)$$

Choose feedback resistor values of 10kΩ. Values other than 10kΩ increase output offset voltage due to the input bias current, which in turn, increases the amount of DC current flow to the load.

Input Filtering

The input capacitor (C_{IN}), in conjunction with the input resistor (R_{IN}), forms a highpass filter that removes the DC bias from an incoming signal (see the *Typical Application Circuits*). The AC-coupling capacitor allows the device to bias the signal to an optimum DC level.

Assuming zero source impedance, the -3dB point of the highpass filter is given by:

$$f_{-3dB} = \frac{1}{2\pi \times R_{IN} \times C_{IN}} (Hz)$$

Choose C_{IN} so f_{-3dB} is well below the lowest frequency of interest. For the MAX13330, use the value of R_{IN} as given in the *Electrical Characteristics* table. Setting f-3dB too high affects the device's low-frequency response. Use capacitors whose dielectrics have lowvoltage coefficients, such as tantalum or aluminum electrolytic. Capacitors with high-voltage coefficients, such as ceramics, can result in increased distortion at low frequencies.

Charge-Pump Capacitor Selection

Use capacitors with an ESR less than 100mΩ for optimum performance. Low-ESR ceramic capacitors minimize the output resistance of the charge pump. For best performance over the extended temperature range, select capacitors with an X7R dielectric.

Flying Capacitor (C1)

The value of the flying capacitor (C1) affects the charge pump's load regulation and output resistance. A C1 value that is too small degrades the device's ability to provide sufficient current drive, which leads to a loss of output voltage. Increasing the value of C1 improves load regulation and reduces the charge-pump output resistance to an extent. See the Output Power vs. Load Resistance graph in the *Typical Operating Characteristics*. Above 1µF, the on-resistance of the switches and the ESR of C1 and C2 dominate.

Holding Capacitor (C2)

The hold capacitor value and ESR directly affect the ripple at CPVSS. Increasing the value of C2 reduces output ripple. Likewise, decreasing the ESR of C2 reduces both ripple and output resistance. Lower capacitance values can be used in systems with low maximum output power levels. See the Output Power vs. Load Resistance graph in the *Typical Operating Characteristics*.

Power-Supply Bypass Capacitor (C3)

The power-supply bypass capacitor (C3) lowers the output impedance of the power supply and reduces the impact of the MAX13330/MAX13331 charge-pump switching transients. Bypass CPVDD with C3, the same value as C1, and place it physically close to the CPVDD and PGND pins.

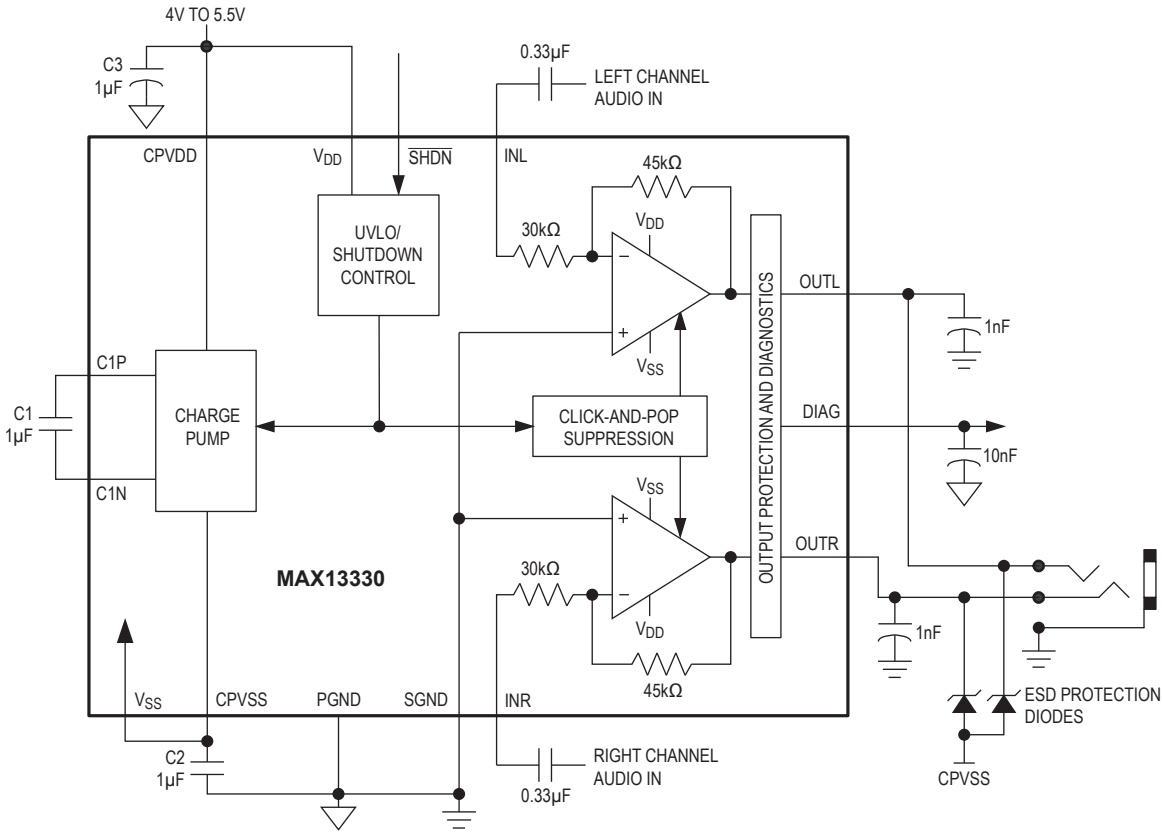
Layout and Grounding

Proper layout and grounding are essential for optimum performance. Connect CPVDD and V_{DD} together at the device. Connect CPVSS and V_{SS} together at the device. Bypassing of both supplies is accomplished by charge-pump capacitors C2 and C3 (see the *Typical Application Circuits*). Place capacitors C2 and C3 as close to the device as possible and bypass them to the PGND plane. Keep PGND and all traces that carry switching transients as short as possible to minimize EMI. Route them away from SGND, the audio signal path, and the external feedback components (MAX13331). Connect the PGND plane and the SGND plane together at a single point on the PCB. Refer to the MAX13330/MAX13331 Evaluation Kit for layout guidelines.

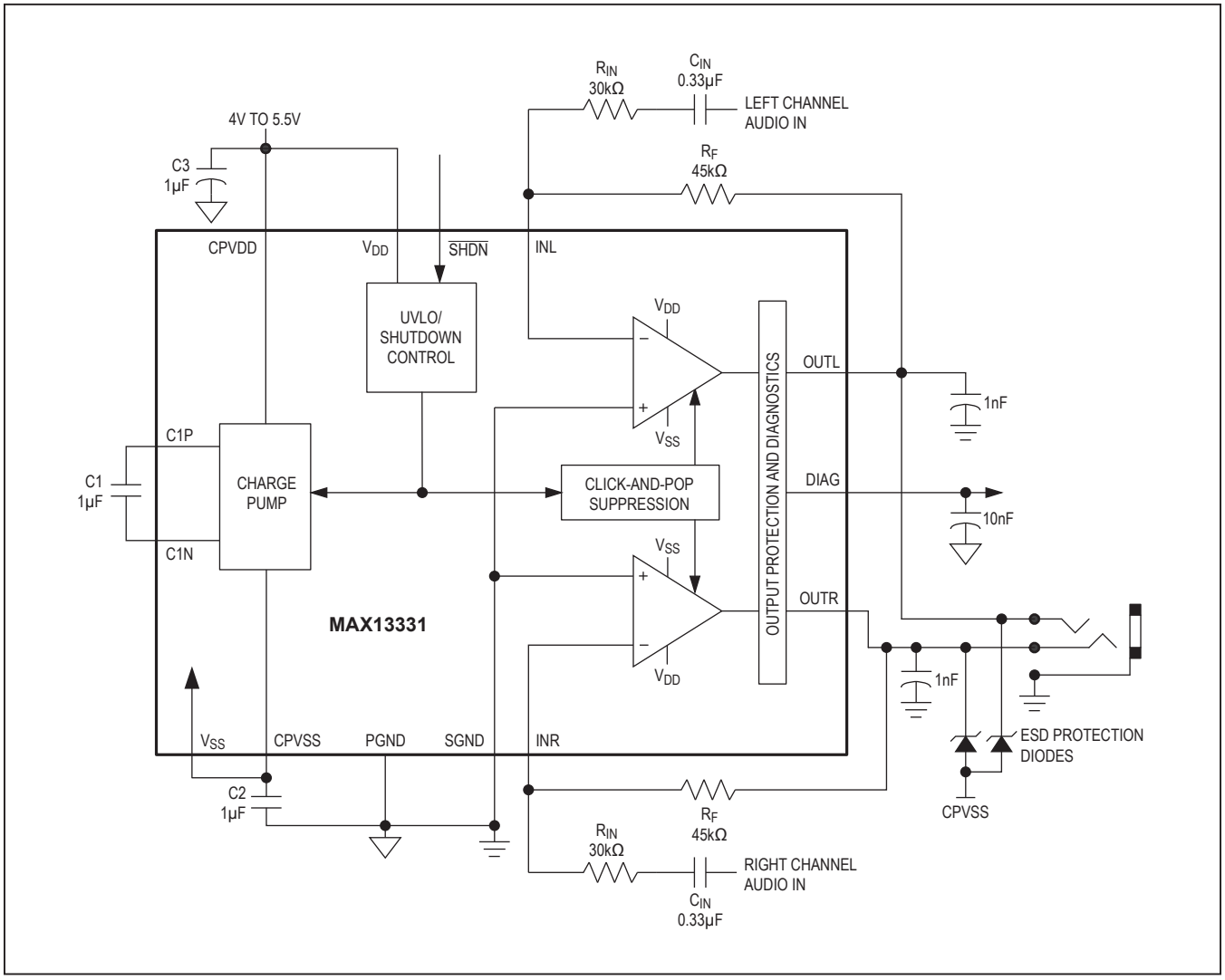
ESD Protection

To pass module level ESD requirements, it may be necessary to add ESD diodes to the MAX13330/MAX13331 outputs. Connect the anode to the CPVSS supply, and connect the cathode to an output pin, as shown in the *Typical Application Circuits*.

Typical Application Circuits



Typical Application Circuits (continued)



Package Information

For the latest package outline information and land patterns (footprints), go to **www.maximintegrated.com/packages**. Note that a "+", "#", or "-" in the package code indicates RoHS status only. Package drawings may show a different suffix character, but the drawing pertains to the package regardless of RoHS status.

PACKAGE TYPE	PACKAGE CODE	OUTLINE NO.	LAND PATTERN NO.
16 QSOP	E16+1	21-0055	90-0167

Revision History

REVISION NUMBER	REVISION DATE	DESCRIPTION	PAGES CHANGED
0	10/08	Initial release	—
1	4/09	Corrected the *Features* section for THD+N, style edits	1, 2, 3, 15
2	5/11	Updated the continuous power dissipation numbers in the *Absolute Maximum Ratings* section; added the *Package Thermal Characteristics* section; added the *ESD Protection* section; updated the *Typical Application Circuits* to add the ESD protection diodes	2, 12, 13, 14
3	7/11	Corrected the units for the click-and-pop level parameter from V to dB in the *Electrical Characteristics* table	3
4	11/15	Corrected package code	14
5	3/21	Updated *Absolute Maximum Ratings* section	2

Mouser Electronics

Authorized Distributor

Click to View Pricing, Inventory, Delivery & Lifecycle Information:

Maxim Integrated:

MAX13330GEE/V+ MAX13330GEE/V+T MAX13331GEE/V+ MAX13331GEE/V+T