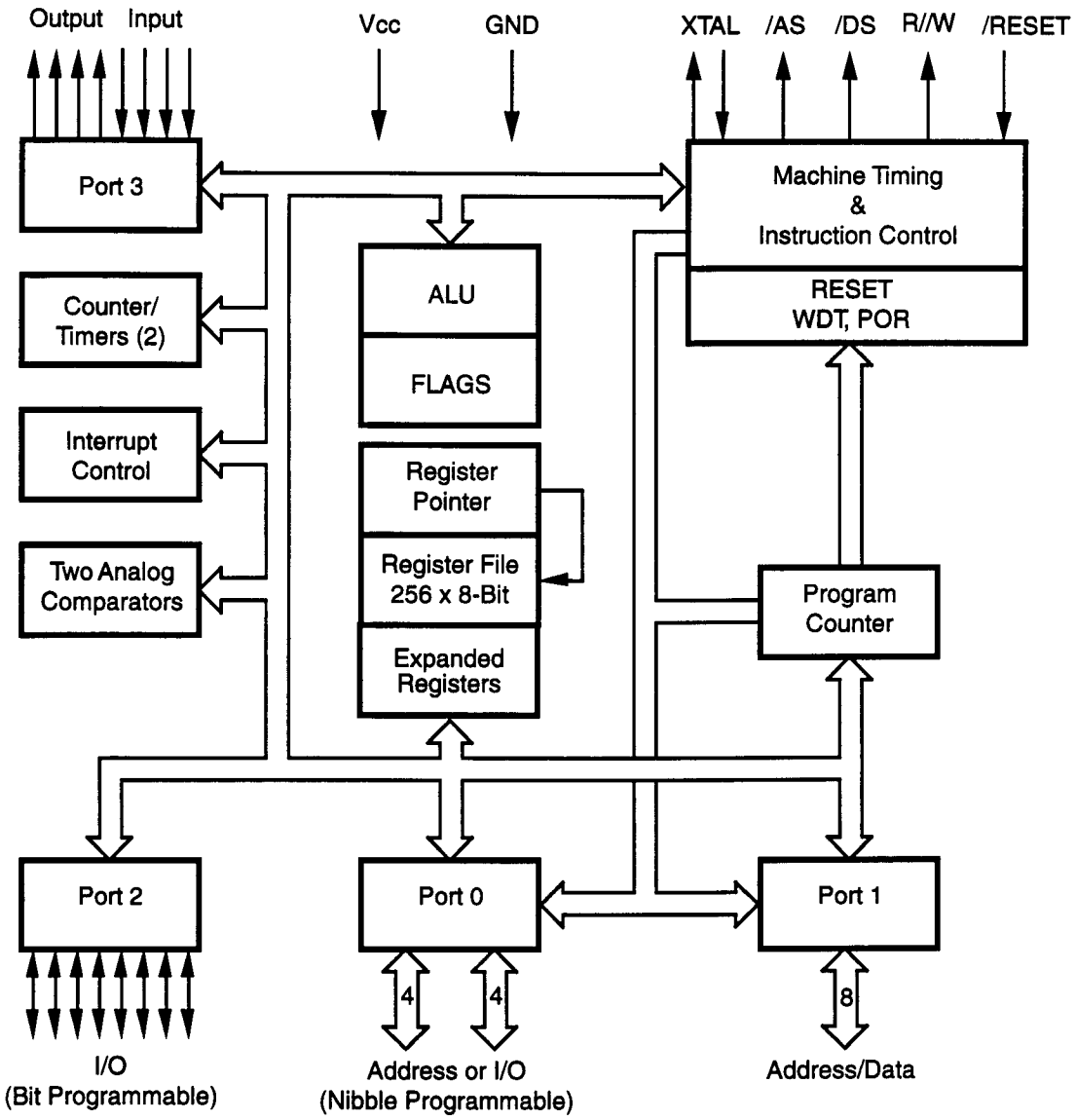
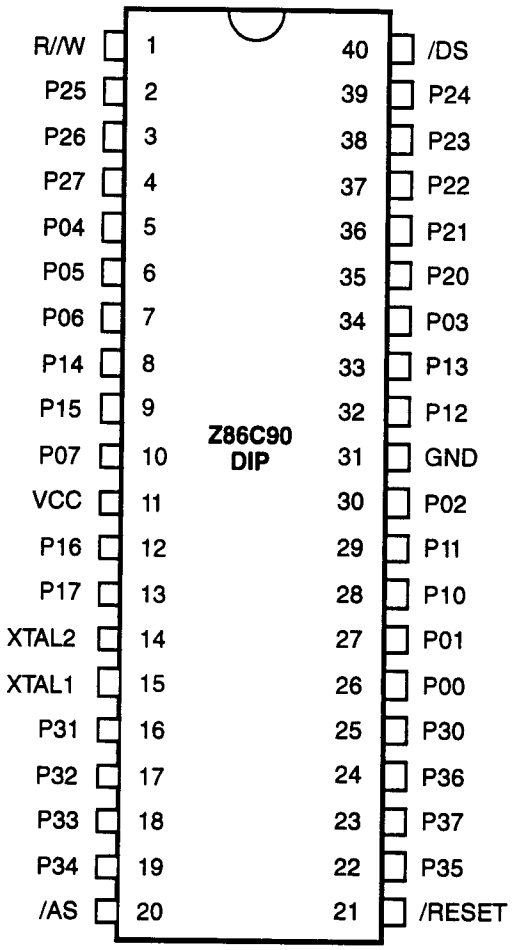
GENERAL DESCRIPTION (Continued)

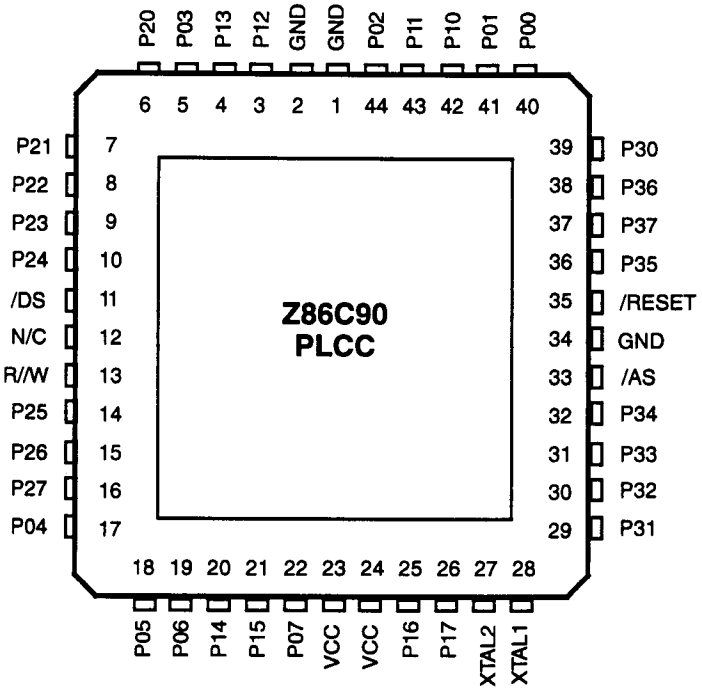


Functional Block Diagram

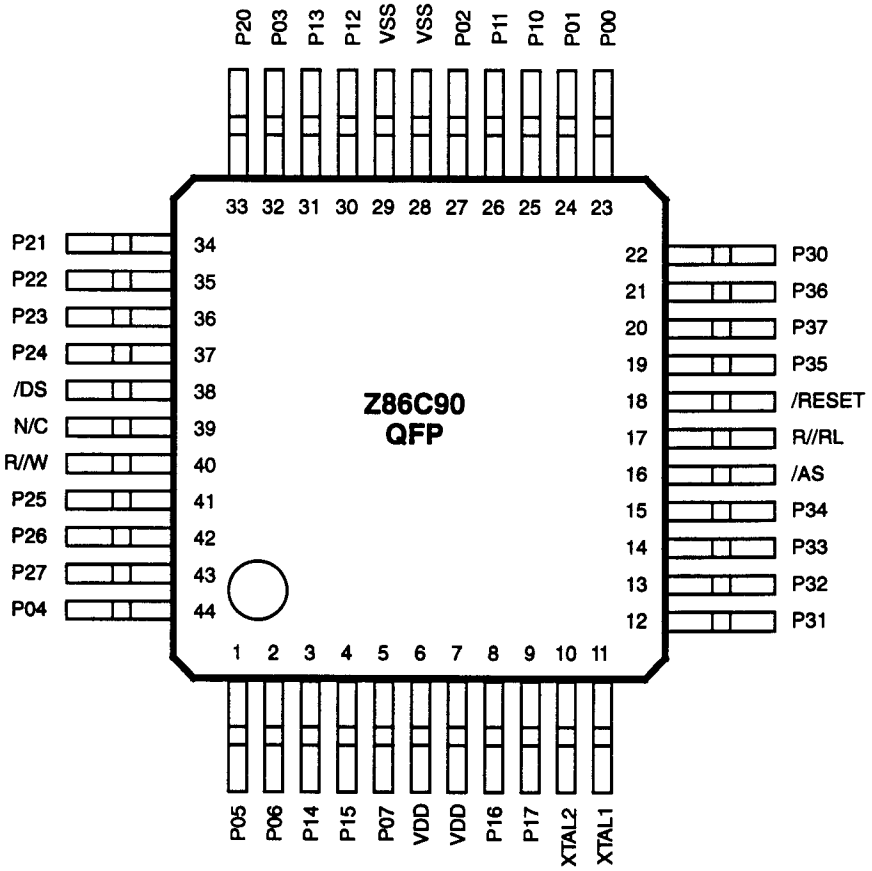


40-Pin DIP Pin Assignments

PIN DESCRIPTION (Continued)



44-Pin PLCC Pin Assignments



44-Pin QFP Pin Assignments

ABSOLUTE MAXIMUM RATINGS

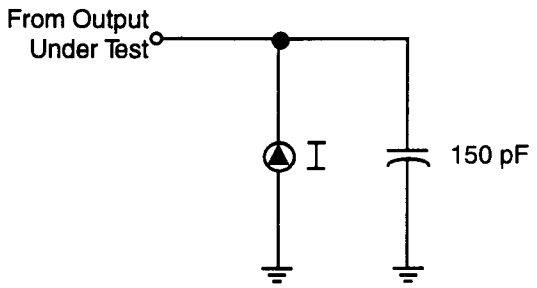
Symbol	Description	Min	Max	Units
V_{DD}	Supply Voltage (*)	–0.3	+7.0	V
T_{STG}	Storage Temp	–65	+150	C
T_A	Oper Ambient Temp			C
	Power Dissipation		2.2	W

Notes:
* Voltage on all pins with respect to GND.
See Ordering Information.

Stress greater than those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; operation of the device at any condition above those indicated in the operational sections of these specifications is not implied. Exposure to absolute maximum rating conditions for an extended period may affect device reliability.

STANDARD TEST CONDITIONS

The characteristics listed below apply for standard test conditions as noted. All voltages are referenced to GND. Positive current flows into the referenced pin (see Test Load Diagram).



Test Load Diagram

CAPACITANCE

T_A = 25°C, V_{DD} = GND = 0V, f = 1.0 MHz, Unmeasured pins to GND

Parameter	Min	Max
Input capacitance	0	12 pF
Output capacitance	0	12 pF
I/O capacitance	0	12 pF

PLEASE NOTE

(1) When ROM Protect is selected, instructions LDC, LDCI, LDE and LDEI are disabled from accessing memory locations 0000H to OFFFH.

(2) The current samples will not have the enhanced ROM Protect feature. See note (1). It will be added after the first samples are evaluated and approved. The final production version will therefore have the enhanced ROM Protection such that LDC, LDCI, LDE, and LDEI instructions can access the memory locations OOOOH and OFFFH.

(3) The Port 3 outputs are reset to High State after Reset, except after Stop-Mode Recovery, at which the outputs remain in the last state.

(4) Extended timing is operable.

(5) P0/P1/P2/P3 is Low EMI software programmable.

(6) P0/P1/P2 is software programmable for open-drain.

(7) Expanded register PCON is Write Only.

(8) WDTMR is writeable only within the first 64 system clocks (128 XTAL clocks) after Reset. Afterward, the WDTMR is write protected.

(9) Device functions down to the V_{BO} threshold. At temperatures below or colder than 25°C, the V_{BO} threshold will rise to a maximum V_{DD} of 3.6V.

(10) Low EMI is 70% of standard pull-down output driver and 60% of standard pull-up output driver.

DC ELECTRICAL CHARACTERISTICS

Sym	Parameter	V_{DD} Note [3]	T_A = –40° C to 105°C Min	Max	T_A = 0° C to 70°C Min	Max	Typical at 25°C	Units	Conditions	Notes
	Max Input Voltage	5.0V		7		7		V	I_{IN} <250 uA	
V_{CH}	Clock Input High Voltage	5.0V	0.7 V_{DD}	V_{DD}+0.3	0.7 V_{DD}	V_{DD}+0.3	2.5	V	Driven by External Clock Generator	
V_{CL}	Clock Input Low Voltage	5.0V	V_{SS}-0.3	0.2 V_{DD}	V_{SS}-0.3	0.2 V_{DD}	1.5	V	Driven by External Clock Generator	
V_{IH}	Input High Voltage	5.0V	0.7 V_{DD}	V_{DD}+0.3	0.7 V_{DD}	V_{DD}+0.3	2.5	V		
V_{IL}	Input Low Voltage	5.0V	V_{SS}-0.3	0.2 V_{DD}	V_{SS}-0.3	0.2 V_{DD}	1.5	V		
V_{OH}	Output High Voltge Low EMI Mode	5.0V	V_{DD}–0.4		V_{DD}–0.4		4.8	V	I_{OH} = –0.5 mA	
V_{OH1}	Output High Voltage	5.0V	V_{DD}–0.4		V_{DD}–0.4		4.8	V	I_{OH} = –2.0 mA	[8]
V_{OL}	Output Low Voltage Low EMI Mode	5.0V		0.4		0.4	0.2	V	I_{OL} = 1.0 mA	
V_{OL1}	Output Low Voltage	5.0V		0.4		0.4	0.1	V	I_{OL} = +4.0 mA	[8]
V_{OL2}	Output Low Voltage	5.0V		1.2		1.2	0.5	V	I_{OL} = +12 mA, 3 Pin Max	[8]
V_{RH}	Reset Input High Voltage	5.0V	.8 V_{DD}	V_{DD}	.8 V_{DD}	V_{DD}	2.1	V		
V_{RL}	Reset Input Low Voltage	5.0V	V_{SS}–0.3	0.2 V_{DD}	V_{SS}–0.3	0.2 V_{DD}	1.7			
V_{OFFSET}	Comparator Input Offset Voltage	5.0V		25		25	10	mV		
V_{ICR}	Input Common Mode Voltage Range	5.0V	0	V_{DD} –1.5V	0	V_{DD} –1.0V		V		[10]
I_{IL}	Input Leakage	5.0V	–1	2	–1	1	<1	µA	V_{IN} = 0V, V_{DD}	
I_{OL}	Output Leakage	5.0V	–1	2	–1	1	<1	µA	V_{IN} = 0V, V_{DD}	
I_{IR}	Reset Input Current	5.0V		–180		–180	–112	µA		
I_{DD}	Supply Current	5.0V		20		20	15	mA	@ 12 MHz	[4,5]
		5.0V		25		25	20	mA	@ 16 MHz	[4,5]

DC ELECTRICAL CHARACTERISTICS (Continued)

Sym	Parameter	V_{DD} Note [3]	T_A = -40°C to 105°C Min	Max	T_A = 0°C to 70°C Min	Max	Typical at 25°C	Units	Conditions	Notes
I_{DD1}	Standby Current	5.0V		6		6	3.2	mA	@ 12 MHz	[4,5]
	(Halt Mode)	5.0V		5		5	2.5	mA	Clock Div. by 16 @12 MHz	[4,5]
I_{DD2}	Standby Current	5.0V		8		8	3.7	mA	@ 16 MHz	[4,5]
	(Halt Mode)	5.0V		7		7	2.9	mA	Clock Div. by 16 @16 MHz	[4,5]
I_{DD2}	Standby Current	5.0V		20		10	2	µA	WDT is Running	[6,11,2]
	(Stop Mode)	5.0V		1000		800	600	µA	WDT is Running	[6,11,2]
I_{ALL}	Auto Latch Low Current	5.0V		40		36	23	µA	$0V < V_{IN} < V_{DD}$	[9]
I_{ALH}	Auto Latch High Current	5.0V		-36		-32	-17	µA	$0V < V_{IN} < V_{DD}$	[9]
V_{BO}	V_{CC} Brown Out Voltage		2.0	3.6	2.2	3.3	3.0	V	2 MHz max INT CLK Freq.	[7]

Note:

[1] I_{DD1}

	Typ	Max	Unit	Freq
Clock Driven on XTAL	0.3 mA	5	mA	8 MHz
Crystal or Resonator	2.4 mA	5	mA	8 MHz

[2] GND=0V.

[3] The V_{DD} voltage spec. of 5.0V guarantees 5.0V ± 0.5V.

[4] All outputs unloaded, I/O pins floating, inputs at V_{DD}, GND rail.

[5] CL1= CL2 = 100pF.

[6] Same as note [4] except inputs at V_{CC}.

[7] -40°C testing is done at V_{CC} = 3.6 due to max. V_{BO} level. The V_{BO} threshold increases as the temperature decreases and overlaps device functionality.

[8] STD Mode (not Low EMI Mode).

[9] Auto Latch (mask option) selected.

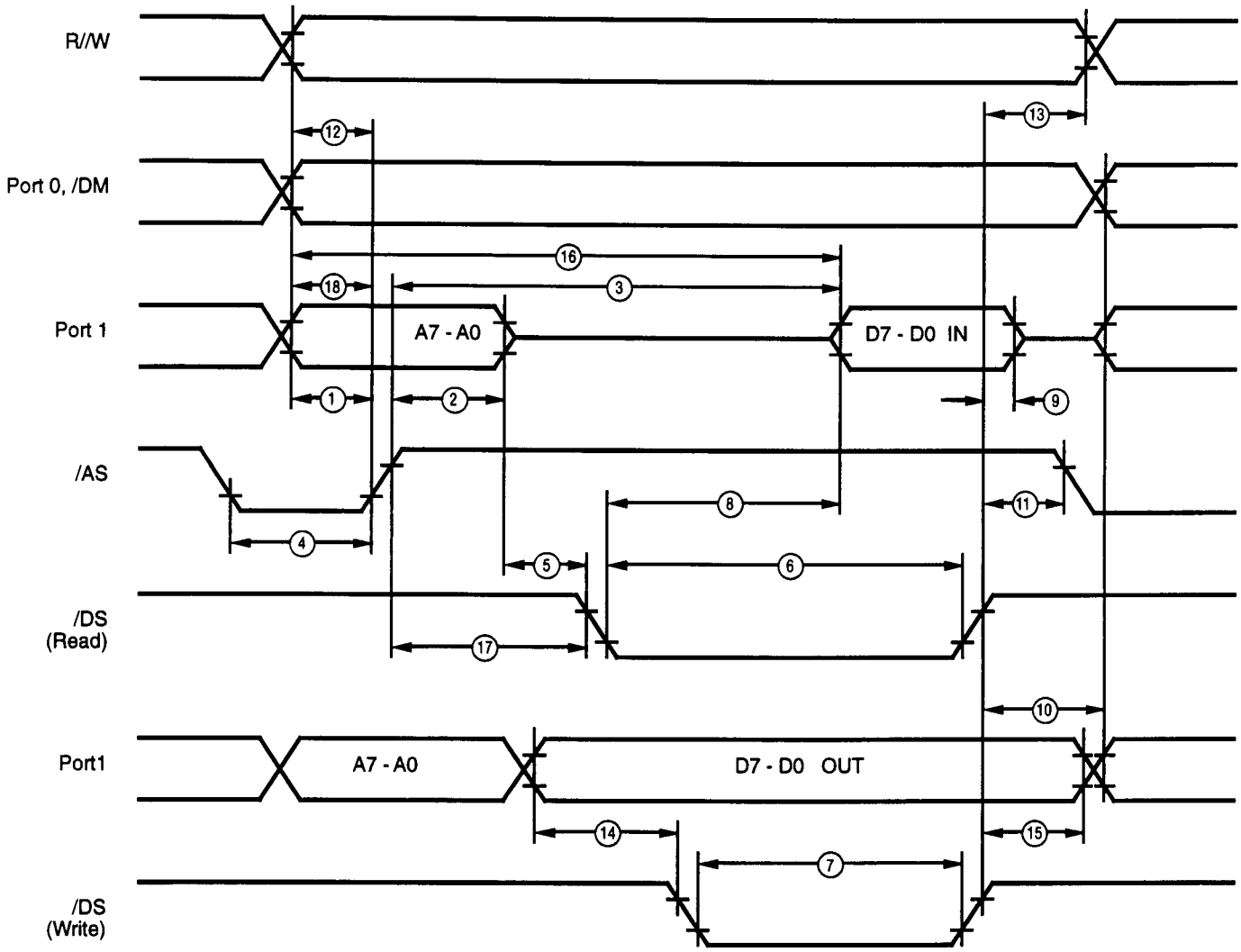
[10] For analog comparator inputs when analog comparators are enabled.

[11] Clock must be forced Low, when XTAL1 is clock driven and XTAL2 is floating.

[12] Typicals are at V_{CC} = 5.0V.

AC CHARACTERISTICS

External I/O or Memory Read and Write Timing Diagram



External I/O or Memory Read/Write Timing

AC CHARACTERISTICS

External I/O or Memory Read and Write Timing Table

No	Symbol	Parameter	V_{DD} [3]	T_A = -40°C to 105°C, T_A = 0°C to 70°C 12 MHz Min	12 MHz Max	16 MHz Min	16 MHz Max	Units	Notes
1	TdA(AS)	Address Valid to /AS Rise Delay	5.0	35		25			[2,4]
2	TdAS(A)	/AS Rise to Address Float Delay	5.0	45		35		ns	[2,4]
3	TdAS(DR)	/AS Rise to Read Data Req'd Valid	5.0		250		180	ns	[1,2,4]
4	TwAS	/AS Low Width	5.0	55		40		ns	[2,4]
5	TdAS(DS)	Address Float to /DS Fall	5.0	0		0		ns	
6	TwDSR	/DS (Read) Low Width	5.0	180		135		ns	[1,2,4]
7	TwDSW	/DS (Write) Low Width	5.0	110		80		ns	[1,2,4]
8	TdDSR(DR)	/DS Fall to Read Data Req'd Valid	5.0		160		75	ns	[1,2,4]
9	ThDR(DS)	Read Data to /DS Rise Hold Time	5.0	0		0		ns	[2,4]
10	TdDS(A)	/DS Rise to Address Active Delay	5.0	55		50		ns	[2,4]
11	TdDS(AS)	/DS Rise to /AS Fall Delay	5.0	45		35		ns	[2,4]
12	TdR/W(AS)	R/W Valid to /AS Rise Delay	5.0	45		25		ns	[2,4]
13	TdDS(R/W)	/DS Rise to R/W Not Valid	5.0	45		35		ns	[2,4]
14	TdDW(DSW)	Write Data Valid to /DS Fall (Write) Delay	5.0	55		25		ns	[2,4]
15	TdDS(DW)	/DS Rise to Write Data Not Valid Delay	5.0	55		35		ns	[2,4]
16	TdA(DR)	Address Valid to Read Data Req'd Valid	5.0		310		230	ns	[1,2,4]
17	TdAS(DS)	/AS Rise to /DS Fall Delay	5.0	65		45		ns	[2,4]
18	TdDM(AS)	/DM Valid to /AS Fall Delay	5.0	30		60		ns	[2,4]

Notes:

[1] When using extended memory timing add 2 TpC.

[2] Timing numbers given are for minimum TpC and System Clock is XTAL frequency divide-by-two only.

[3] The V_{DD} voltage spec. of 5.0V guarantees 5.0V ± 0.5V.

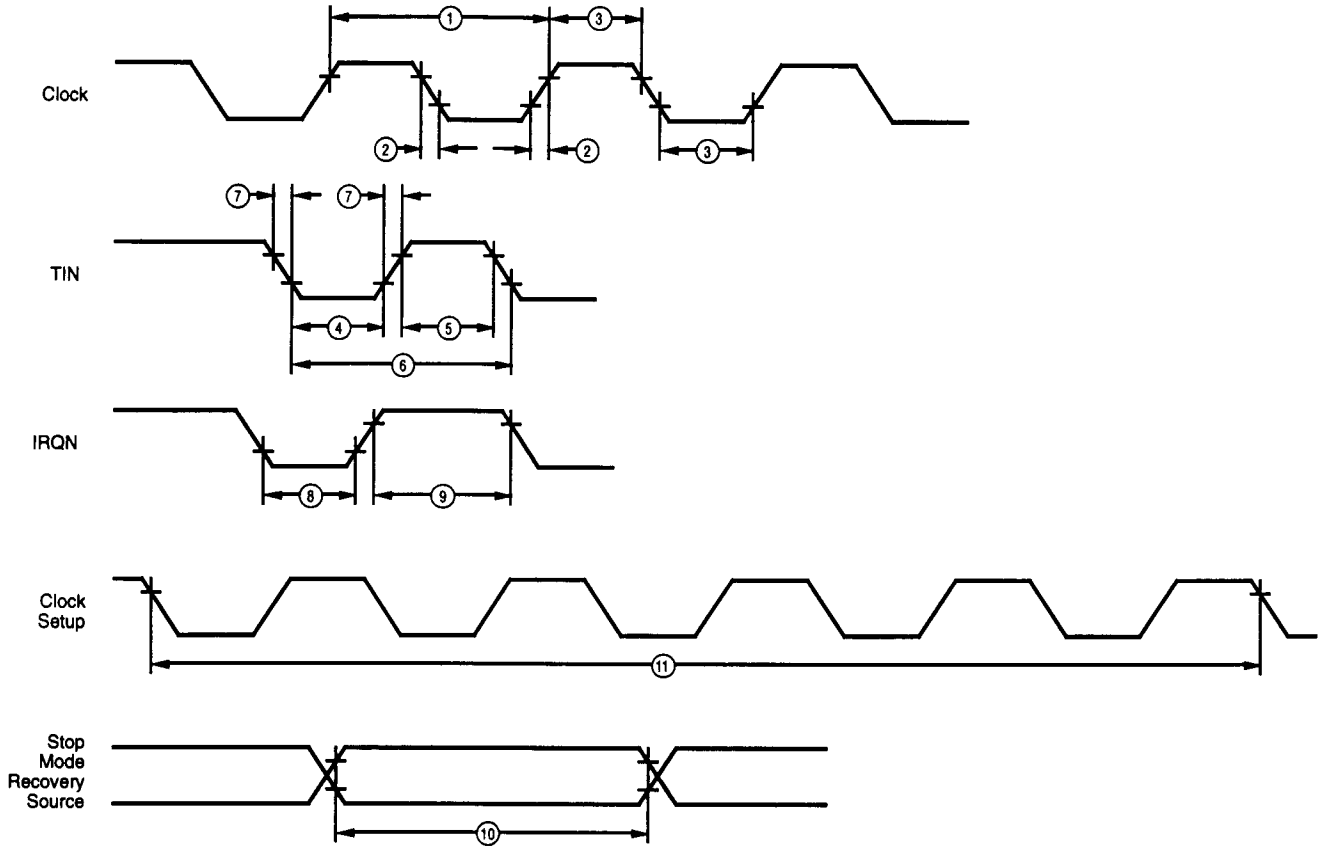
[4] Standard Mode (not Low EMI Mode for outputs), SMR D1 = 0, D0 = 0.

Standard Test Load

All timing references use 0.7 V_{DD} for a logic 1 and 0.2 V_{DD} for a logic 0.

AC ELECTRICAL CHARACTERISTICS

Additional Timing Diagram



Additional Timing

AC ELECTRICAL CHARACTERISTICS

Additional Timing Table (Divide-By-One Mode)

No	Symbol	Parameter	V_{DD} Note [6]	T_A = –40°C to 105°C, T_A = 0°C to 70°C, 4 MHz Min	Max	Units	Notes
1	TpC	Input Clock Period	5.0V	250	DC	ns	[1,5,7,8]
2	TrC,TfC	Clock Input Rise & Fall Times	5.0V		25	ns	[1,5,7,8]
3	TwC	Input Clock Width	5.0V	100		ns	[1,5,7,8]
4	TwTinL	Timer Input Low Width	5.0V	70		ns	[1,7,8]
5	TwTinH	Timer Input High Width	5.0V	5TpC			[1,7,8]
6	TpTin	Timer Input Period	5.0V	8TpC			[1,7,8]
7	TrTin, TfTin	Timer Input Rise & Fall Timer	5.0V		100	ns	[1,7,8]
8A	TwIL	Int. Request Low Time	5.0V	70		ns	[1,2,7,8]
8B	TwIL	Int. Request Low Time	5.0V	5TpC			[1,3,7,8]
9	TwIH	Int. Request Input High Time	5.0V	5TpC			[1,2,7,8]
10	Twsm	STOP Mode Recovery Width Spec	5.0V	12		ns	[4,8]
11	Tost	Oscillator Startup Time	5.0V		5TpC		[4,8,9]

Notes:

[1] Timing Reference uses 0.7 V_{DD} for a logic 1 and 0.2 V_{DD} for a logic 0.

[2] Interrupt request via Port 3 (P31-P33).

[3] Interrupt request via Port 3 (P30).

[4] SMR-D5 = 1, POR STOP Mode Delay is on.

[5] Divide-By-One mode is programmed independently of Low EMI oscillator mode.

[6] The V_{DD} voltage spec. of 5.0V guarantees 5.0V ± 0.5V.

[7] SMR D1 = 0.

[8] Maximum frequency for internal system clock is 4 MHz when using XTAL divide-by-one mode.

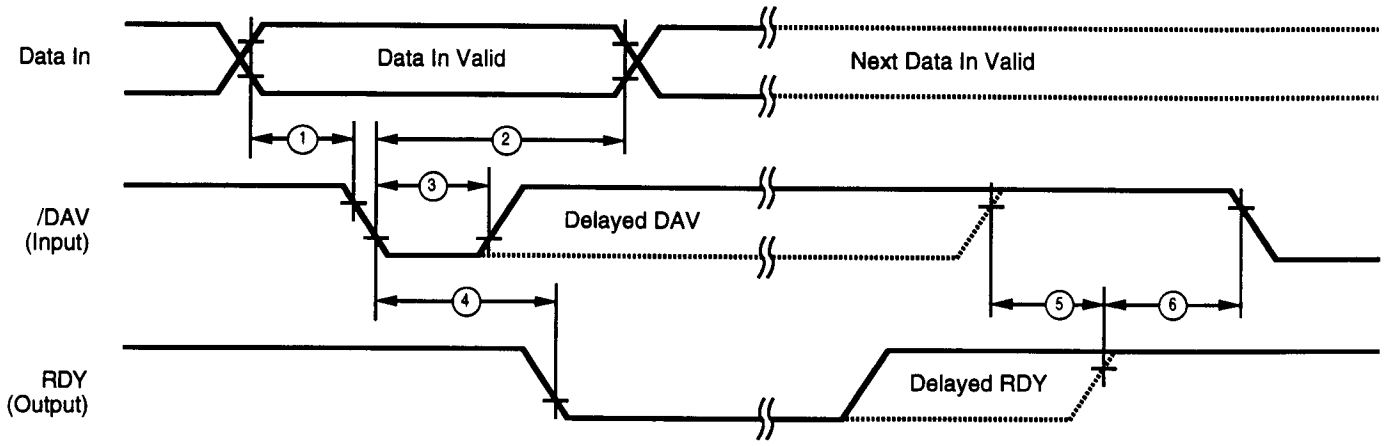
[9] For RC and LC oscillator, and for oscillator driven by clock driver.

AC ELECTRICAL CHARACTERISTICS
Additional Timing Table

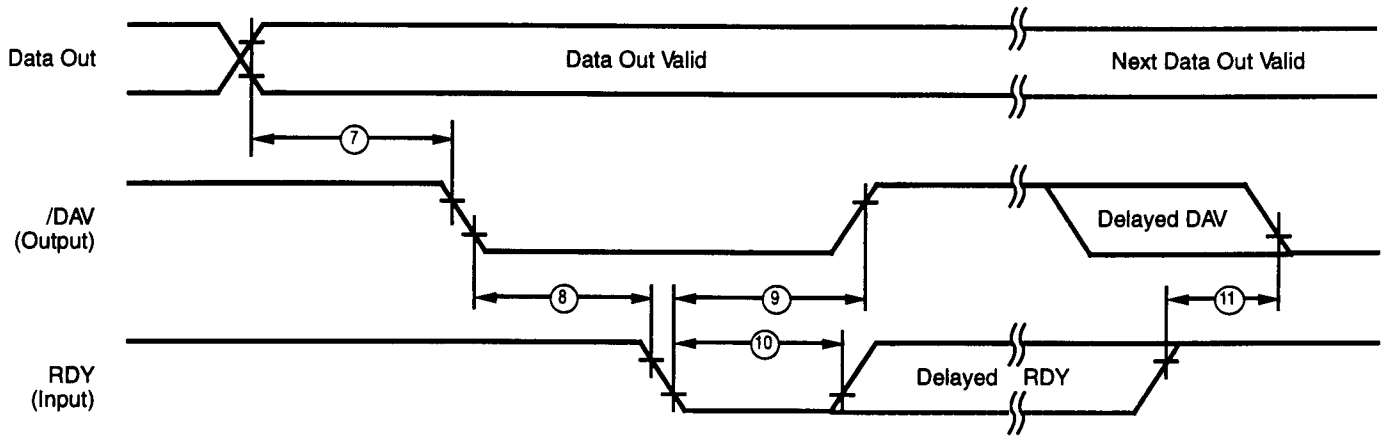
No	Symbol	Parameter	V_{DD} Note [6]	T_A = -40°C to 105°C T_A = °C to 70°C 12 MHz Min	12 MHz Max	16 MHz Min	16 MHz Max	Units	Notes
1	TpC	Input Clock Period	5.0V	83	DC	62.5	DC	ns	[1,7,8]
2	TrC,TfC	Clock Input Rise & Fall Times	5.0V		15		15	ns	[1,7,8]
3	TwC	Input Clock Width	5.0V	26		31		ns	[1,7,8]
4	TwTinL	Timer Input Low Width	5.0V	70		70		ns	[1,7,8]
5	TwTinH	Timer Input High Width	5.0V	5TpC		5TpC			[1,7,8]
6	TpTin	Timer Input Period	5.0V	8TpC		8TpC			[1,7,8]
7	TrTin, TfTin	Timer Input Rise & Fall Timer	5.0V		100		100	ns	[1,7,8]
8A	TwIL	Int. Request Low Time	5.0V	70		70		ns	[1,2,7,8]
8B	TwIL	Int. Request Low Time	5.0V	5TpC		5TpC			[1,3,7,8]
9	TwIH	Int. Request Input High Time	5.0V	5TpC		5TpC			[1,2,7,8]
10	Twsm	STOP Mode Recovery Width Spec	5.0V	12		12		ns	[4,8]
11	Tost	Oscillator Startup Time	5.0V		5TpC		5TpC		[4,9]
12	Twdt	Watchdog Timer Delay Time	5.0V	3		3		ms	D1 = 0 [5,10]
			5.0V	8		8		ms	D1 = 0 [5,10]
			5.0V	16		16		ms	D1 = 1 [5,10]
			5.0V	66		66		ms	D1 = 1 [5,10]
13	Tpor	Power On Reset Delay	5.0V	1.0	14	1.0	14	ms	

Notes:
[1] Timing Reference uses 0.7 V_{DD} for a logic 1 and 0.2 V_{DD} for a logic 0.
[2] Interrupt request via Port 3 (P31-P33).
[3] Interrupt request via Port 3 (P30).
[4] SMR-D5 = 1, POR STOP Mode Delay is on.
[5] Reg. WDTMR.
[6] The V_{DD} voltage spec. of 5.0V guarantees 5.0V ± 0.5V.
[7] SMR D1 = 0.
[8] Maximum frequency for internal system clock is 4 MHz when using XTAL divide-by-one mode.
[9] For RC and LC oscillator, and for oscillator driven by clock driver.
[10] Using internal RC.

AC ELECTRICAL CHARACTERISTICS
Handshake Timing Diagrams



Input Handshake Timing



Output Handshake Timing

AC ELECTRICAL CHARACTERISTICS

Handshake Timing Table

No	Symbol	Parameter	V_{DD} Note [1]	T_A = –40°C to 105°C, T_A = 0°C to70°C 12 MHz Min	12 MHz Max	16 MHz Min	16 MHz Max	Data Direction	Notes
1	TsDI(DAV)	Data In Setup Time	5.0V	0			0	IN	[2]
2	ThDI(DAV)	Data In Hold Time	5.0V	115			115	IN	[2]
3	TwDAV	Data Available Width	5.0V	110		110		IN	[2]
4	TdDAVI(RDY)	DAV Fall to RDY Fall Delay	5.0V		115		115	IN	[2]
5	TdDAVId(RDY)	DAV Out to DAV Fall Delay	5.0V		80		80	IN	[2]
6	RDY0d(DAV)	RDY Rise to DAV Fall Delay	5.0V	0		0		IN	[2]
7	TdD0(DAV)	Data Out to DAV Fall Delay	5.0V	42		31		OUT	[2]
8	TdDAV0(RDY)	DAV Fall to RDY Fall Delay	5.0V	0		0		OUT	[2]
9	TdRDY0(DAV)	RDY Fall to DAV Rise Delay	5.0V		115		115	OUT	[2]
10	TwRDY	RDY Width	5.0V	80		80		OUT	[2]
11	TdRDY0d(DAV)	RDY Rise to DAV Fall Delay	5.0V		80		80	OUT	[2]

Notes:

[1] Timing Reference uses 0.7 V_{DD} for a logic 1 and 0.2 V_{DD} for a logic 0.

[2] Standard Mode (not Low EMI Mode on output ports).

[3] The V_{DD} voltage spec. of 5.0V guarantees 5.0V ± 0.5V.

Pre-Characterization Product:
The product represented by this CPS is newly introduced and Zilog has not completed the full characterization of the product. The CPS states what Zilog knows about this product at this time, but additional features or non-conformance with some aspects of the CPS may be found, either by Zilog or its customers in the course of further application and characterization work. In addition, Zilog cautions that delivery may be uncertain at times, due to start-up yield issues.

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Customer is advised that this product does not meet Zilog's internal guardbanded test policies for the specification requested and is supplied on an exception basis. Customer is cautioned that delivery may be uncertain and that, in addition to all other limitations on Zilog liability stated on the front and back of the acknowledgement, Zilog makes no claim as to quality and reliability under the CPS. The product remains subject to standard warranty for replacement due to defects in materials and workmanship.

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