

ABSOLUTE MAXIMUM RATINGS (T _A = 25°C unless otherwise noted) (Note 1)						
PARAMETER	SYMBOL	LIMIT	UNIT			
Supply Voltage	V _{cc}	+36 or ±18	V			
Differential Input Voltage	V _{IDR}	36	V			
Input Common Mode Voltage Range	V _{ICR}	-0.3 to 36	V			
Input Current	I _{IN}	50	mA			
Output Short Circuit to Ground	I _{SC}	Continuous				
Output Sink Current	I _{SINK}	20	mA			
Operating Temperature Range	T _{OPR}	0 ~ +70	°C			
Junction Temperature	TJ	150	°C			
Storage Temperature Range	T _{STG}	-65 ~ +150	°C			
Lead Temperature 1.6mm (1/16") from case for 10s.	T _{LEAD}	260	°C			

PARAMETER	SYMBOL	MIN	ТҮР	MAX	UNIT
Input Offset Voltage (note 3)	V _{IO}		2	5	mV
Input Offset Current				50	
I _{IN(+)} - I _{IN(-)} , V _{CM} =0V	I _{IO}			50	nA
Input Offset Current (note 4)				050	
I _{IN(+)} - I _{IN(-)} , V _{CM} =0V	I _{IB}			250	nA
Input Common Mode Voltage Range (note 5)		0			Ň
V _{CC} =30V	V _{ICR}	-0		V _{CC} -1.5	V
Voltage Gain	Δ.	50	200		
R _L ≥15K, V _{CC} =15V, Vo=1V~11V	A _{VOL}	50	200		V/mV
Large Signal Response Time					
Vin=TTL Logic Swing. V _{REF} = 1.4V,			300		ns
V_{RL} =5V. R_{L} =5.1 $k\Omega$					
Response Time (note 6)	4		1.3		μs
V_{RL} =5V. R_{L} =5.1k Ω	t _{TLH}		1.3		
Output Sink Current		6.0	16		mA
V _{IN} (-)=1V, V _{IN} (+)=0V, Vo≤1.5V	I _{SINK}	0.0	10		ША
Output Saturation Voltage			250	400	m\/
V _{IN} (-)=1V, V _{IN} (+)=0V, I _{SINK} ≤4mA	V _{OL}		250	400	mV
Output Leakage Current			0.1		nA
V _{IN} (-)=0V, V _{IN} (+)=1V, Vo=5V	I _{OL}		0.1		ПА
Supply Current					
$R_L = \infty$, $V_{CC} = 5V$	I _{cc}		0.4	1.0	mA
$R_L = \infty$, $V_{CC} = 36V$			1.0	2.5	

ELECTRICAL CHARACTERISTICS

Note:

- 1. The max. Output current may be as high as 20mA, independent of the magnitude of V_{CC}, output short circuits to V_{CC} can cause excessive heating and eventual destruction.
- 2. This magnitude of input current will only occur if the input leads are driven more negative than ground or the negative supply voltage. This is due to the input PNP collector base junction becoming forward biased acting as an input clamp diode. There is also a lateral PNP parasitic transistor action on the IC chip. This phenomenon can cause the output voltage of the comparators to go to the V_{CC} voltage level (or ground if overdrive is large) during the time the input is driven negative. This will not destroy the device and normal output states will recover when the inputs become -0.3V of ground or negative supply.
- 3. At output switch point, $V_0=1.4Vdc$, $R_S=0\Omega$ with V_{CC} from 5Vdc to 30Vdc, and over the full input common-mode
- 4. Due to the PNP transistor inputs, bias current will flow out of the inputs, this current is essentially constant independent of the output state, therefore, no loading changes will exist on the input lines.
- 5. Input common mode of either input should not be permitted to go more than 0.3V negative of ground or minus supply. The upper limit of common mode range is V_{CC} 1.5V but either or both inputs can be taken to as high as 30volts without damage.
- 6. Response time is specified with a 100mV step and 5.0mV of overdrive. With larger magnitudes of overdrive faster response times are obtainable.

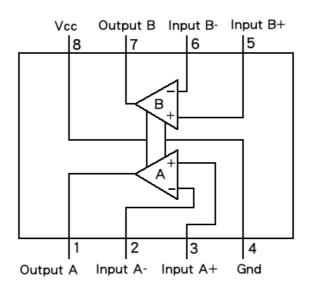
ORDERING INFORMATION

PART NO.	PACKAGE	PACKING
TS393CD C3G	DIP-8	50pcs / Tube
TS393CS RLG	SOP-8	2,500pcs / 13" Reel

Note:

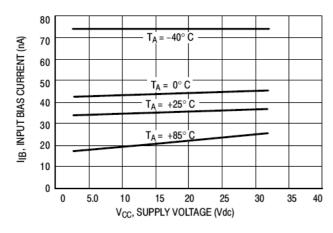
- 1. Compliant to RoHS Directive 2011/65/EU and in accordance to WEEE 2002/96/EC.
- 2. Halogen-free according to IEC 61249-2-21 definition.

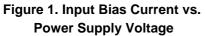
BLOCK DIAGRAM

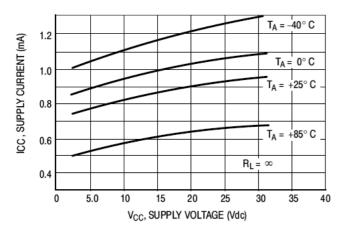


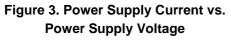


ELECTRICAL CHARACTERISTICS CURVE









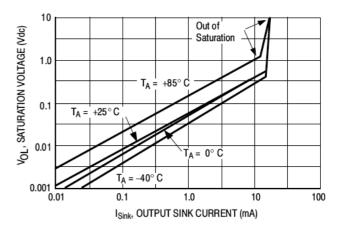
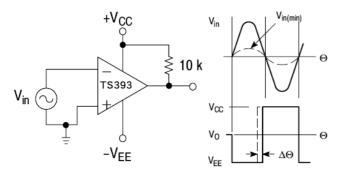


Figure 2. Output Saturation Voltage vs. Output Sink Current



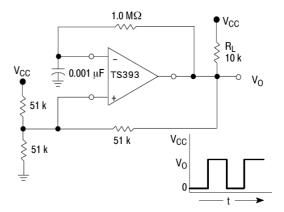
APPLICATION INFORMATION

This dual comparator feature high gain, wide bandwidth characteristics. This gives the device oscillation tendencies if the outputs are capacitive coupled to the inputs via stray capacitance. This oscillation manifests itself during output transitions (V_{OL} to V_{OH}). To alleviate this situation input resistors<10k Ω should be used. The addition of positive feedback (<10 mV) is also recommended. It is good design practice to ground all unused pins. Differential input voltages may be larger than supply voltage without damaging the comparator's inputs. Voltages more negative than -0.3V should not be used.



 $V_{in(min)} \approx$ 0.4 V peak for 1% phase distortion ($\Delta \Theta$).







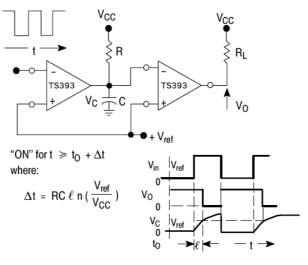
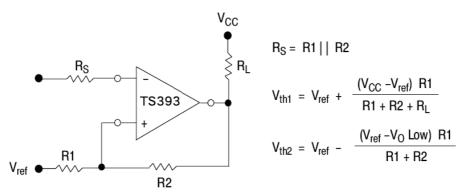


Figure 6. Zero Crossing Detector (Single Supply)







PACKAGE OUTLINE DIMENSIONS (Unit: Millimeters)

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MARKING DIAGRAM

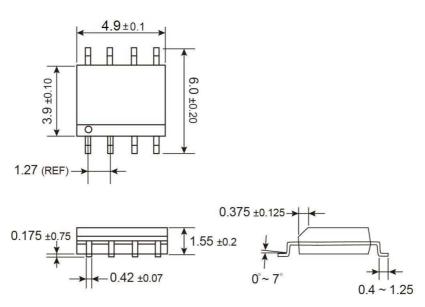
ഺ൨൷൷	Y	= Year Code						
TS393CD	M = Month Code for Halogen Free Product							
		O =Jan	Ρ	=Feb	Q	=Mar	R	=Apr
<u> </u> #1┠┎┖┖┚	•	S =May	Т	=Jun	U	=Jul	V	=Aug
		W =Sep	Х	=Oct	Y	=Nov	Ζ	=Dec
L = Lot Code (1~9, A~Z)								

DIP-8

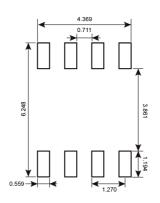


PACKAGE OUTLINE DIMENSIONS (Unit: Millimeters)

SOP-8



SUGGESTED PAD LAYOUT (Unit: Millimeters)



MARKING DIAGRAM

, A. A. A. A.	Y	= Year Code					
TS393CS	М	= Month Code	e for Haloge	n Fr	ee Proc	duct	
YML 5		O =Jan	P =Feb	Q	=Mar	R	=Apr
	•	S =May	T =Jun	U	=Jul	V	=Aug
#1UUUU		W =Sep	X =Oct	Υ	=Nov	Ζ	=Dec
L = Lot Code (1~9, A~Z)							



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