4-Pin, Low-Power µP Reset Circuits with Manual Reset

Absolute Maximum Ratings

Terminal Voltage (with respect to GND)	Continuous Power Dissipation (T _A = +70°C)
V _{CC} 0.3V to +6V	4-Pin SOT143 (derate 4mW/°C above +70°C)
Push/Pull RESET or RESET, MR0.3V to (V _{CC} + 0.3V)	Operating Temperature Range40°C to +125°C
Open-Drain RESET0.3V to +6V	Junction Temperature+150°C
Input Current (V _{CC})20mA	Storage Temperature Range65°C to +150°C
Output Current (RESET, RESET)	Lead Temperature (soldering, 10s)+300°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Electrical Characteristics

(V_{CC} = full range, T_A = -40°C to +125°C, unless otherwise noted. Typical values are at V_{CC} = +5.0V and T_A = +25°C, reset not asserted.) (Note 1)

PARAMETER	SYMBOL	cc	ONDI	TIONS	MIN	TYP	MAX	UNITS	
Supply Voltage Range		$T_{1} = 0^{\circ}C t_{0} \pm 125^{\circ}C$		MAX6803/MAX6804	0.7		5.5		
		$T_A = 0^{\circ}C$ to +125°C	τſ	MAX6805	1.0		5.5	v	
(Note 1)	V _{CC}	$ T_{\Lambda} = -40^{\circ}C \text{ to } +125^{\circ}C$	F°0	MAX6803/MAX6804	0.78		5.5		
			MAX6805	1.2		5.5			
Supply Current	1			V _{CC} = +3.0V		4	10		
Supply Current	Icc	No load		V _{CC} = +5.0V		5	12	μA	
Depart Threshold		MAX680 US D	-T,	T _A = +25°C	V _{TH} - 1.8%	V _{TH}	V _{TH} + 1.8%	v	
Reset Threshold	V _{TH}	Table 1	_	T _A = -40°C to +125°C	V _{TH} - 3%	V _{TH}	V _{TH} + 3%		
V _{CC} Falling Reset Delay		V _{CC} falling at 10V/ms			30		μs		
	t _{RP}	MAX680_USD1-T		1	1.5	2			
Reset Active Timeout Period		MAX680_USD2-T		20	30	40	ms		
		MAX680_USD3	MAX680_USD3-T		100	150	200		
MR Minimum Pulse Width				1			μs		
MR Glitch Immunity					50		ns		
MR Reset Delay						0.1		μs	
MR Input Voltage	VIL					(0.3 × V _{CC}	; v	
	VIH			0.7 × V _{CC}		V			
MR Pullup Resistance					12	20	30	kΩ	
RESET Output Low Voltage (MAX6804/MAX6805)			I _{SINK} = 50µA, V _{CC} ≥ 1.0V				0.4		
	V _{OL}	Reset I _{SI}	I_{SINK} = 1.2mA, $V_{CC} \ge 2.5V$				0.3	V	
			INK =	3.2mA, V _{CC} ≥ 4.25V			0.4		
RESET Output High Voltage	V _{OH}	Reset not ISC	OURC	_E = 500µA, V _{CC} ≥ 3.0V	0.8 × V _C	С		v	
(MAX6804)		asserted I _{SOUF}		_E = 800µA, V _{CC} ≥ 5.0V	0.8 × V _C	С		v	

$\begin{array}{l} \mbox{4-Pin, Low-Power} \\ \mbox{μP$ Reset Circuits with Manual Reset} \end{array}$

Electrical Characteristics (continued)

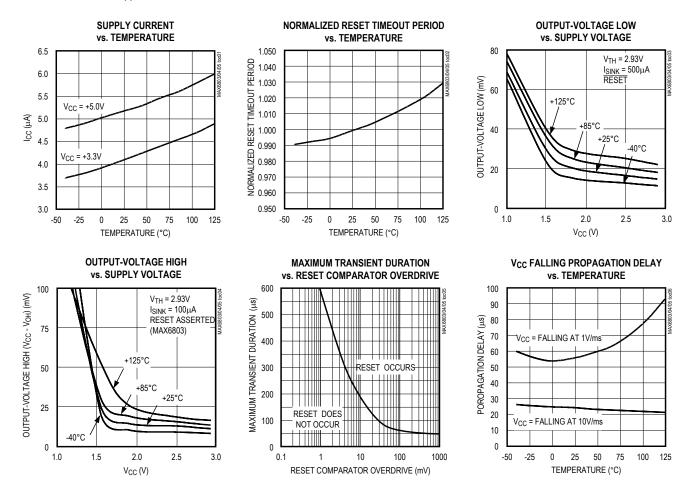
(V_{CC} = full range, T_A = -40°C to +125°C, unless otherwise noted. Typical values are at V_{CC} = +5.0V and T_A = +25°C, reset not asserted.) (Note 1)

PARAMETER	SYMBOL		CONDITIONS	MIN	TYP	MAX	UNITS
RESET Output Voltage (MAX6803)	V _{OH}	Reset asserted	I _{SOURCE} = 1µA, V _{CC} ≥ 1.0V	0.8 × V ₀	C		
			$I_{\text{SOURCE}} = 200 \mu \text{A}, V_{\text{CC}} \ge 1.8 \text{V}$	0.8 × V _C	С		V
			I _{SOURCE} = 800µA, V _{CC} ≥ 4.25V	0.8 × V _C	С		
	V _{OL}	Reset not asserted	I _{SINK} = 1.2mA, V _{CC} ≥ 3.0V			0.3	v
			I _{SINK} = 3.2mA, V _{CC} ≥ 5.0V			0.4	
RESET Output Leakage Current (MAX6805)		$V_{CC} > V_{TH}$, RESET not asserted				0.5	μA

Note 1: All parts are production tested at $T_A = +25$ °C. Over temperature limits are guaranteed by design and not production tested. **Note 2:** I_{SOURCE} for the MAX6803 is 100nA; I_{SINK} for the MAX6804 is 100nA; I_{SINK} for the MAX6805 is 50µA.

Typical Operating Characteristics

(Reset not asserted, $T_A = +25^{\circ}C$, unless otherwise noted.)



4-Pin, Low-Power µP Reset Circuits with Manual Reset

Pin Description

PI	N			
MAX6803	MAX6804 MAX6805	NAME	FUNCTION	
1	1	GND	Ground	
_	2	RESET	Active-Low Reset Output. $\overline{\text{RESET}}$ is asserted while VCC is below the reset threshold, or while $\overline{\text{MR}}$ is asserted. $\overline{\text{RESET}}$ remains asserted for a reset timeout period (tRP) after VCC rises above the reset threshold or $\overline{\text{MR}}$ is deasserted. $\overline{\text{RESET}}$ on the MAX6804 is push/pull. $\overline{\text{RESET}}$ on the MAX6805 is open-drain.	
2	_	RESET	Active-High Reset Output. RESET is asserted high while VCC is below the reset threshold or while $\overline{\text{MR}}$ is asserted, and RESET remains asserted for a reset timeout period (tRP) after VCC rises above the reset threshold or $\overline{\text{MR}}$ is deasserted. RESET on the MAX6803 is push/pull.	
3	3	MR	Manual-Reset Input. A logic low on $\overline{\text{MR}}$ asserts reset. Reset remains asserted as long as $\overline{\text{MR}}$ is low, and for the reset timeout period (tRP) after $\overline{\text{MR}}$ goes high. Leave unconnected or connect to VCC if not used.	
4	4	Vcc	Supply Voltage Input	

Applications Information

Manual-Reset Input

Many μ P-based products require manual-reset capability, allowing the operator, a test technician, or external logic circuitry to initiate a reset. A logic low on \overline{MR} asserts reset. Reset remains asserted while \overline{MR} is low, and for the reset active timeout period after \overline{MR} returns high. \overline{MR} has an internal 20k Ω pullup resistor, so it can be left unconnected if not used. Connect a normally open momentary switch from \overline{MR} to GND to create a manual-reset function; external debounce circuitry is not required.

Interfacing to µPs with Bidirectional Reset Pins

Since the RESET output on the MAX6805 is open-drain, this device interfaces easily with μ Ps that have bidirectional reset pins, such as the Motorola 68HC11. Connecting the μ P supervisor's RESET output directly to the microcontroller's (μ C's) RESET pin with a single pullup resistor allows either device to assert reset (Figure 1).

Negative-Going V_{CC} Transients

In addition to issuing a reset to the μ P during power-up, power-down, and brownout conditions, these devices are relatively immune to short-duration, negative-going V_{CC} transients (glitches). The *Typical Operating Characteristics* show the Maximum Transient Duration vs. Reset Comparator Overdrive graph. The graph shows the maximum pulse width that a negative-going V_{CC} transient may typically have without issuing a reset signal. As the amplitude of the transient increases, the maximum allowable pulse width decreases.

Ensuring a Valid Reset Output Down to $V_{CC} = 0$

When V_{CC} falls below 1V and approaches the minimum operating voltage of 0.7V, push/pull-structured reset sinking (or sourcing) capabilities decrease drastically. High-impedance CMOS-logic inputs connected to the RESET pin can drift to indeterminate voltages. This does not present a problem in most cases, since most

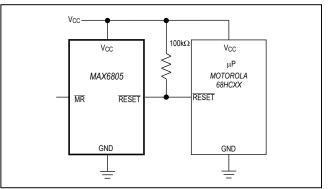


Figure 1. Interfacing to μ Ps with Bidirectional Reset Pins

μPs and circuitry do not operate when V_{CC} drops below 1V. For the MAX6804 application where RESET must be valid down to 0, adding a pulldown resistor between RESET and GND removes stray leakage currents, holding RESET low (Figure 2a). The pulldown resistor value is not critical; 100kΩ is large enough not to load RESET, and small enough to pull it low. For the MAX6803, where RESET must be valid to V_{CC} = 0, a 100kΩ pullup resistor between RESET and V_{CC} will hold RESET high when V_{CC} falls below 0.7V (Figure 2b).

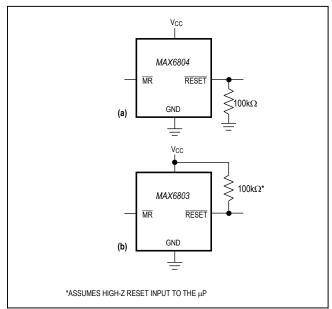
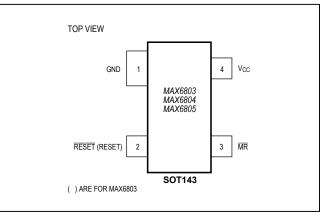


Figure 2. Ensuring Reset Valid down to $V_{CC} = 0$

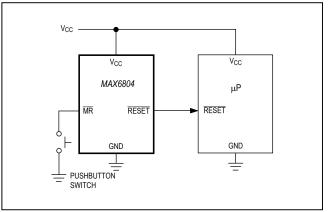
4-Pin, Low-Power µP Reset Circuits with Manual Reset

Since the MAX6805 has an open-drain, active-low out-put, it typically uses a pullup resistor. With this device, RESET will most likely not maintain an active condition, but will drift to a non-active level due to the pullup resistor and the reduced sinking capability of the opendrain device. Therefore, this device is not recommended for applications where the RESET pin is required to be valid down to $V_{CC} = 0$.

Pin Configuration



Typical Operating Circuit



4-Pin, Low-Power µP Reset Circuits with Manual Reset

RESET THRESHOLD	RESET T ₄			T _A = -40°C	to +125°C
SUFFIX	MIN	TYP (V _{TH})	MAX	MIN	MAX
48	4.714	4.80	4.886	4.656	4.944
47	4.615	4.70	4.785	4.559	4.841
46	4.547	4.63	4.713	4.491	4.769
45	4.419	4.50	4.581	4.365	4.635
44	4.301	4.38	4.459	4.249	4.511
43	4.223	4.30	4.377	4.171	4.429
42	4.124	4.20	4.276	4.074	4.326
41	4.026	4.10	4.174	3.977	4.223
40	3.928	4.00	4.072	3.880	4.120
39	4.830	3.90	3.970	3.783	4.017
38	3.732	3.80	3.868	3.686	3.914
37	3.633	3.70	3.767	3.589	3.811
36	3.535	3.60	3.665	3.492	3.708
35	3.437	3.50	3.563	3.395	3.605
34	3.339	3.40	3.461	3.298	3.502
33	3.241	3.30	3.359	3.201	3.399
32	3.142	3.20	3.258	3.104	3.296
31	3.025	3.08	3.135	2.988	3.172
30	2.946	3.00	3.054	2.910	3.090
29	2.877	2.93	2.983	2.842	3.018
28	2.750	2.80	2.850	2.716	2.884
27	2.651	2.70	2.749	2.619	2.781
26	2.583	2.63	2.677	2.551	2.709

Table 1. Factory-Trimmed Reset Thresholds

4-Pin, Low-Power µP Reset Circuits with Manual Reset

PART	OUTPUT STAGE	NOMINAL V _{TH} (V)	MIN RESET TIMEOUT (ms)	SOT TOP MARK
MAX6803US26D3-T	Push/Pull RESET	2.63	100	KACH
MAX6803US29D3-T	Push/Pull RESET	2.93	100	KACI
MAX6803US31D3-T	Push/Pull RESET	3.08	100	KACJ
MAX6803US44D3-T	Push/Pull RESET	4.38	100	KACK
MAX6803US46D3-T	Push/Pull RESET	4.63	100	KACL
MAX6804US26D3-T	Push/Pull RESET	2.63	100	KACN
MAX6804US29D3-T	Push/Pull RESET	2.93	100	KACP
MAX6804US31D3-T	Push/Pull RESET	3.08	100	KACQ
MAX6804US44D3-T	Push/Pull RESET	4.38	100	KACR
MAX6804US46D3-T	Push/Pull RESET	4.63	100	KACS
MAX6805US26D3-T	Open-Drain RESET	2.63	100	KACO
MAX6805US29D3-T	Open-Drain RESET	2.93	100	KACU
MAX6805US31D3-T	Open-Drain RESET	3.08	100	KACV
MAX6805US44D3-T	Open-Drain RESET	4.38	100	KACW
MAX6805US46D3-T	Open-Drain RESET	4.63	100	KACX

Selector Guide (Standard Versions*)

*Sample stock is generally held on all standard versions.

Chip Information

TRANSISTOR COUNT: 505 PROCESS: BICMOS

Package Information

For the latest package outline information and land patterns (footprints), go to <u>www.maximintegrated.com/packages</u>. Note that a "+", "#", or "-" in the package code indicates RoHS status only. Package drawings may show a different suffix character, but the drawing pertains to the package regardless of RoHS status.

PACKAGE	PACKAGE	OUTLINE	LAND
TYPE	CODE	NO.	PATTERN NO.
4 SOT143	U4-1	<u>21-0052</u>	<u>90-0183</u>

4-Pin, Low-Power µP Reset Circuits with Manual Reset

Revision History

REVISION	REVISION	DESCRIPTION	PAGES
NUMBER	DATE		CHANGED
3	7/14	No /V OPNs; removed Automotive reference from Applications section	1

For pricing, delivery, and ordering information, please contact Maxim Direct at 1-888-629-4642, or visit Maxim Integrated's website at www.maximintegrated.com.

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