CMOS, 12-Bit, Serial-Input Multiplying DAC

ABSOLUTE MAXIMUM RATINGS

V_{DD} to GND ..... +17V
VREF to GND ..... ±25V
VRFB to GND ..... ±25V
Digital Input Voltage to GND ..... -0.3V, V_{DD} + 0.3V
V_{IOUT} to GND ..... -0.3V, V_{DD} + 0.3V
Continuous Power Dissipation (T_A = +70°C)
8-Pin Plastic DIP (derate 9.09mW/°C above +70°C) .. 727mW
8-Pin SO (derate 5.88mW/°C above +70°C) 471mW
16-Pin Wide SO (derate 9.52mW/°C above +70°C) .. 762mW
8-Pin CERDIP (derate 8.00mW/°C above +70°C) 640mW

Operating Temperature Ranges:
MAX543AC/BC _ _ ..... 0°C to +70°C
MAX543AE/BE _ _ ..... -40°C to +85°C
MAX543AM/BMJA ..... -55°C to +125°C
Storage Temperature Range ..... -65°C to +150°C
Lead Temperature (soldering, 10 sec) ..... +300°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

(V_{DD} = +5V, +12V or +15V; VREF = +10V; V_{IOUT} = GND = 0V; T_A = T_{MIN} to T_{MAX}, unless otherwise noted.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS			MIN	TYP	MAX	UNITS
STATIC PERFORMANCE								
Resolution	N				12			Bits
Integral Nonlinearity	INL			MAX543A			±1/2	LSB
				MAX543B			±1	
Differential Nonlinearity	DNL	Guaranteed monotonic to 12 bits over temperature		MAX543A			±1/2	LSB
				MAX543B			±1	
Gain Error	FSE	Using internal R_{FB}	T_A = +25°C	MAX543A			±1	LSB
				MAX543B			±2	
			T_A = T_{MIN} to T_{MAX}	All grades			±2	
Gain Tempco ΔGain/ΔTemp (Note 2)	TCFS	Using internal R_{FB}				±1	±5	ppm/°C
DC Supply Rejection	PSR	ΔV_{DD} = ±5%					±0.001	%/%
DYNAMIC PERFORMANCE (Note 2)								
Current Settling Time	ts	T_A = +25°C, to 1/2LSB, I_{OUT} load is 100Ω||3pF, DAC register alternately loaded with all 1s and all 0s				0.25	1	µs
Digital-to-Analog Glitch	Q	VREF = 0V, I_{OUT} load is 100Ω||13pF, DAC register alternately loaded with all 1s and all 0s				2	20	nV-s
AC Feedthrough at I_{OUT}	FTE	VREF = ±10V_{p-p} at 10kHz, DAC register loaded with all 0s				0.4	1	mV_{p-p}
Total Harmonic Distortion	THD	VREF = 6V_{rms} at 1kHz, DAC register loaded with all 1s				-85		dB
Output Noise-Voltage Density	e_n	10Hz to 100kHz, measured between R_{FB} and I_{OUT}				13	15	$nV/\sqrt{Hz}$
REFERENCE INPUT								
Input Resistance	RREF				7	11	15	kΩ
Input Resistance Tempco	TCR					-200		ppm/°C

ELECTRICAL CHARACTERISTICS (continued)

(V_{DD} = +5V, +12V or +15V; VREF = +10V; V_{IOUT} = GND = 0V; T_A = T_{MIN} to T_{MAX}, unless otherwise noted.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS			MIN	TYP	MAX	UNITS
ANALOG OUTPUT								
I_{OUT} Leakage Current	I_{LKG}	DAC register loaded with all 0s	T_A = +25°C	All grades		±0.5	±5	nA
			T_A = T_{MIN} to T_{MAX}	MAX543AC/BC/AE/BE			±25	
				MAX543AM/BM			±100	
I_{OUT} Capacitance (Note 2)	C_{OUT}	DAC register loaded with all 0s				55	80	pF
		DAC register loaded with all 1s				85	110	
DIGITAL INPUTS								
Input High Voltage	V_{IH}	V_{DD} = 5V			2.4			V
		V_{DD} = 15V			13.5			
Input Low Voltage	V_{IL}	V_{DD} = 5V					0.8	V
		V_{DD} = 15V					1.5	
Input Leakage Current	I_{IN}	Digital inputs at 0V or V_{DD}					±1	µA
Input Capacitance (Note 2)	C_{IN}	Digital inputs at 0V or V_{DD}					8	pF
SWITCHING CHARACTERISTICS (Note 3)								
CLK Pulse Width HIgh	t_{CH}				90			ns
CLK Pulse Width Low	t_{CL}				120			ns
SRI Data to CLK Setup	t_{DS}				40			ns
SRI Data to CLK Hold	t_{DH}				80			ns
$\overline{LOAD}$ Pulse Width	t_{LD}				120			ns
LSB CLK to $\overline{LOAD}$	t_{SL}				0			ns
$\overline{LOAD}$ High to CLK	t_{LC}				0			ns
POWER SUPPLY								
V_{DD} Range	V_{DD}	V_{DD} = 12V or 15V			+11.40		+15.75	V
		V_{DD} = 5V			+4.75		+5.25	
I_{DD} Range	I_{DD}	All digital inputs at V_{IL} or V_{IH}					500	µA
		All digital inputs at 0V or V_{DD}				5	100	

Note 1: Tests are performed at V_{DD} = +5V and V_{DD} = +15V. Operation at +12V is guaranteed by power-supply rejection (PSR) tests.
Note 2: Guaranteed by design, not subject to test.
Note 3: Sample tested to 0.1% AQL.

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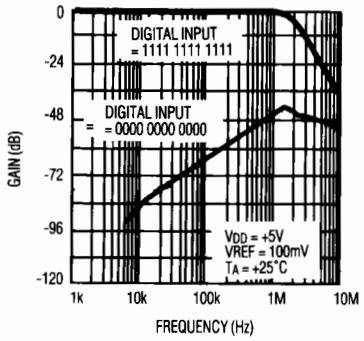
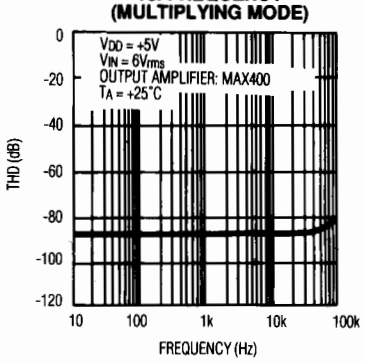
Typical Operating Characteristics

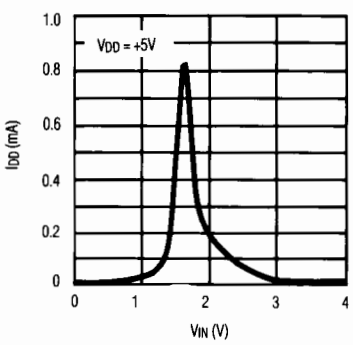
GAIN vs. FREQUENCY (OUTPUT AMPLIFIER: MAX400)



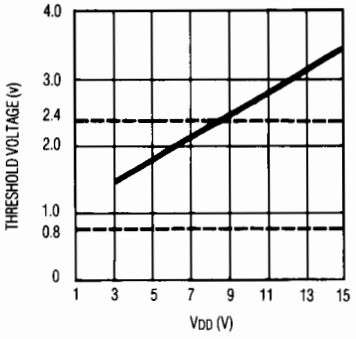
TOTAL HARMONIC DISTORTION vs. FREQUENCY (MULTIPLYING MODE)



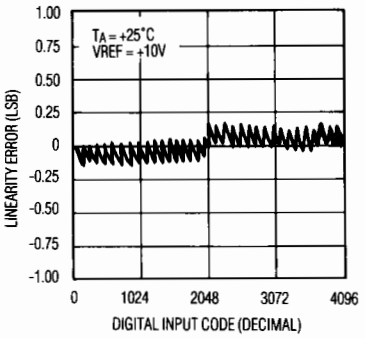
SUPPLY CURRENT vs. LOGIC INPUT VOLTAGE



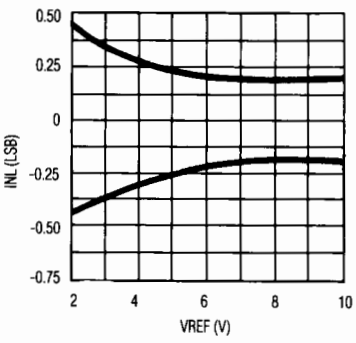
LOGIC THRESHOLD VOLTAGE vs. SUPPLY VOLTAGE



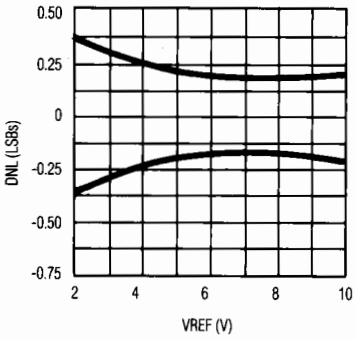
LINEARITY ERROR vs. DIGITAL CODE



INTEGRAL NONLINEARITY ERROR vs. REFERENCE VOLTAGE



DIFFERENTIAL NONLINEARITY ERROR vs. REFERENCE VOLTAGE



Detailed Description

D/A Converter

The MAX543 DAC circuit consists of a laser-trimmed, thin-film R-2R resistor array with NMOS current switches, as shown in Figure 1. Binary weighted currents are switched to either IOUT or GND depending on the status of each input data bit. Although the current at IOUT and GND depends on the digital input code, the sum of the two output currents is always equal to the input current at VREF.

The current output (IOUT) can be converted into a voltage by adding an external output amplifier (Figure 3). The VREF input accepts a wide range of signals, including fixed and time-varying voltage or current inputs. If a current source is used for the reference input, then a low-tempco external resistor should be used for RFB to minimize gain variation with temperature.

The internal feedback resistor (RFB) is compensated with an NMOS switch that matches the NMOS switches used in the R-2R array. This results in excellent supply rejection and gain-temperature coefficient.

The IOUT pin output capacitance (COUT) is code dependent and is typically 55pF with all switches to GND and 85pF with all switches to IOUT.

Digital Circuit

Figure 2 shows the MAX543 timing diagram. The most significant bit (MSB) is always loaded first on the rising edge of the clock. When all data is shifted into the MAX543, the DAC register is loaded by taking the $\overline{LOAD}$ signal low. The DAC register is transparent when $\overline{LOAD}$ is low and latched when $\overline{LOAD}$ is high. If the $\overline{LOAD}$ signal is taken low before the LSB bit is fully shifted into the shift register, the DAC output can produce a "glitch." If this is undesirable, the $\overline{LOAD}$ signal can be delayed 30ns after the rising edge of the LSB clock edge to avoid this condition.

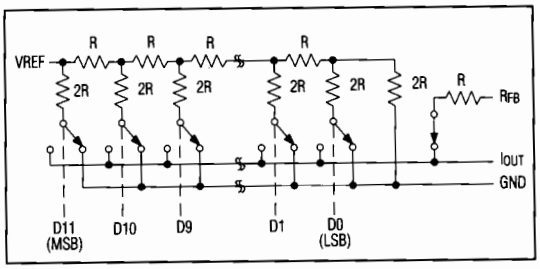


Figure 1. MAX543 Simplified Circuit

The MAX543's input buffer inverters act as level shifters, converting TTL levels into CMOS logic levels. These input buffers are TTL and 5V-CMOS compatible (0.8V and 2.4V) at VDD = 5V. For VDD = 15V the input buffers are CMOS compatible (1.5V and 13.5V). At this supply voltage, the input buffers are in their linear region when the input voltages are between 1V and 6V. Therefore, to minimize high supply currents, the digital input voltages should be kept as close to the supply and ground voltages (VDD and GND) as possible.

Circuit Configurations

Unipolar Operation

Figure 3 shows the MAX543's basic application. This circuit is used for unipolar operation or 2-quadrant multiplication. The code table for this mode is given in Table 1. Note that the polarity of the output is the inverse of the reference voltage, VREF.

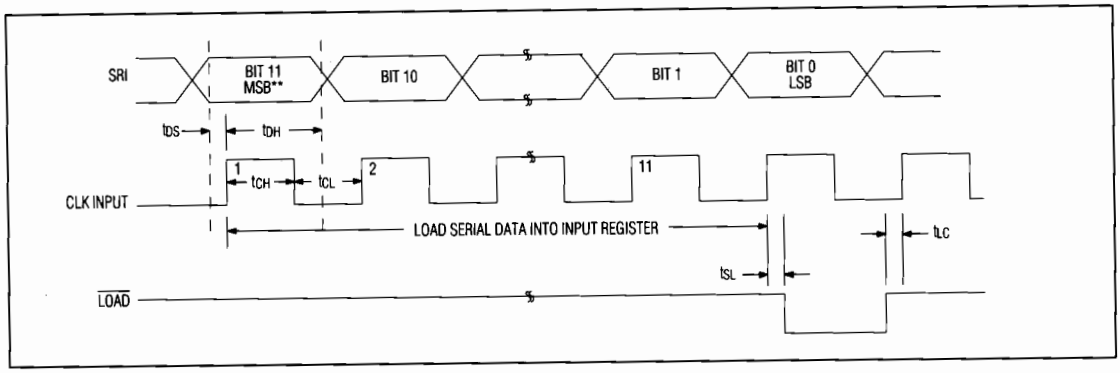


Figure 2. Write-Cycle Timing Diagram

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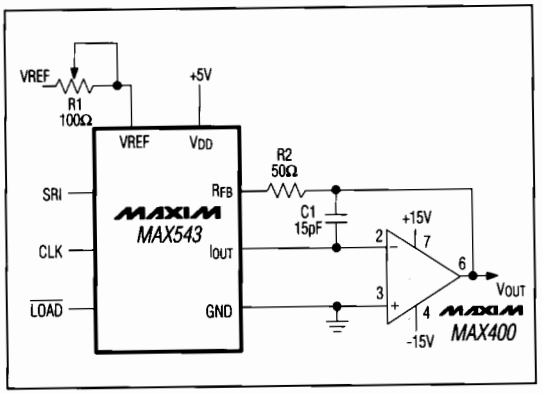

Figure 3. Unipolar Operation

Table 1. Unipolar Binary-Code Table for Circuit of Figure 3

DIGITAL INPUT			ANALOG OUTPUT
MSB		LSB	
1111	1111	1111	$-VREF\left(\frac{4095}{4096}\right)$
1000	0000	0000	$-VREF\left(\frac{2048}{4096}\right)=-\frac{VREF}{2}$
0000	0000	0001	$-VREF\left(\frac{1}{4096}\right)$
0000	0000	0000	0

In many applications, gain adjustment will not be necessary since the part's gain accuracy is sufficient, or is trimmed at the reference source. In these cases, resistors R1 and R2 in Figure 3 can be omitted. If the gain is trimmed and the DAC is operated over a wide temperature range, use low-tempco (<300ppm/°C) resistors for R1 and R2.

Capacitor C1 provides phase compensation and reduces overshoot and ringing when fast amplifiers are used at the output of the DAC.

Bipolar Operation

Figure 4 shows the MAX543 operating in bipolar (or 4-quadrant multiplying) mode. A second amplifier and three matched resistors (R3 , R4 and R5) are required. These resistors must be of the same material (preferably

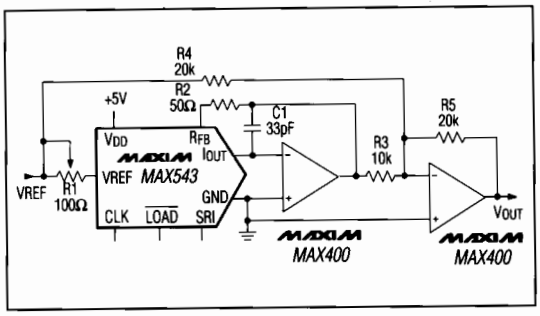

Figure 4. Bipolar Operation

Table 2. Offset Binary-Code Table for Circuit of Figure 4

DIGITAL INPUT			ANALOG OUTPUT
MSB		LSB	
1111	1111	1111	$+VREF\left(\frac{2047}{2048}\right)$
1000	0000	0001	$+VREF\left(\frac{1}{2048}\right)$
1000	0000	0000	0
0111	1111	1111	$-VREF\left(\frac{1}{2048}\right)$
0000	0000	0000	$-VREF\left(\frac{2048}{2048}\right)$

Table 3. Twos-Complement Code Table

DIGITAL INPUT			ANALOG OUTPUT
MSB		LSB	
0111	1111	1111	$+VREF\left(\frac{2047}{2048}\right)$
0000	0000	0001	$+VREF\left(\frac{1}{2048}\right)$
0000	0000	0000	0
1111	1111	1111	$-VREF\left(\frac{1}{2048}\right)$
1000	0000	0000	$-VREF\left(\frac{2048}{2048}\right)$

metal film or wire-wound) for good temperature tracking characteristics (<15ppm/°C), and should match to 0.01% for 12-bit performance. The output code is offset binary and is listed in Table 2. In multiplying applications, the MSB determines output polarity while the other 11 bits control the amplitude. The MSB can be inverted in software using an exclusive-OR instruction to make the MAX543 work with twos-complement coding. Table 3 shows the code relationships to output voltage for twos-complement operation.

To adjust the circuit, load the DAC with a code of 1000 0000 0000 and trim R1 for a 0V output. With R1 and R2 omitted, an alternative zero trim is needed to adjust the ratio of R3 and R4 for 0V out. Trim full scale by loading the DAC with all 0s or all 1s, and adjusting VREF's amplitude or varying R5 until the desired positive or negative output is obtained. In many applications, the gain adjustment will not be necessary, especially when using parts with a guaranteed maximum ±1LSB gain error. In these cases the gain can be trimmed at the reference source and resistors R1 and R2 in Figure 4 omitted. However, if the trims are desired and the DAC is operated over a wide temperature range, then low-tempco (<300ppm/°C) resistors should be used for R1 and R2.

Single-Supply Operation (Voltage Mode)

The MAX543 can be conveniently used in single-supply (voltage mode) operation with I_{OUT} biased at any voltage between GND and V_{DD}. I_{OUT} must not be allowed to go 0.3V lower than the GND or 0.3V higher than V_{DD}. Otherwise, internal diodes would turn on, causing a high current flow from the supply that could damage the device.

Figure 5 shows the MAX543 connected as a voltage-output DAC. I_{OUT} is connected to the reference-voltage source and GND is grounded. The DAC output now appears at the VREF pin, which has a constant impedance equal to the reference input resistance (typically 11kΩ). This output should be buffered with an op amp when a lower output impedance is required. R_{FB} pin is not used in this mode.

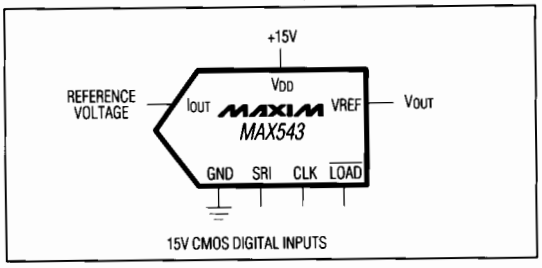

Figure 5. Single-Supply Operation Using Voltage-Switching Mode

The input impedance of the reference input (I_{OUT}) for this mode is code dependent, and the circuit's response time depends on the reference source's behavior with changing load conditions.

Two advantages of voltage-mode operation are single-supply operation and that a negative reference is not required for a positive output. Note that the reference input (I_{OUT}) must always be positive and is limited to no more than 2.5V when V_{DD} is 15V. If the reference voltage is greater than 2.5V or V_{DD} is reduced, resistance mismatches in the DAC's internal NMOS switches result in degraded integral (INL) and differential nonlinearity (DNL).

The unipolar and bipolar circuits in Figures 3 and 4 can all be converted to voltage-output mode.

MAX543 Opto-Isolated Application

Figure 6a shows the MAX543 interface to optocouplers for isolated barrier applications. Three optocouplers (OC1, OC2 and OC3) carry the serial data and clocking signals across the isolation barrier. Isolated power sources, V+ and V-, supply the MAX543, the output amplifier and optocouplers. If data word updates are infrequent and large analog output transitions can be tolerated while serial data is being clocked in, then parts count can be reduced by eliminating optocoupler OC3 and tying $\overline{LOAD}$ (pin 5) of the MAX543 low.

When using type 6N136 optocouplers, this circuit accepts serial data at a maximum clock rate of 100kHz, or 130µs per data word. The SERIAL DATA and $\overline{LOAD}$ signals should change coincident with the falling edge of CLOCK, as shown in the timing diagram (Figure 6b). A positive CLOCK cycle is masked during the time $\overline{LOAD}$ is low.

The MAX543 will also work with 5V isolated supplies using the optocoupler circuit of Figure 6a. Change the values of R1 through R3 to 3kΩ to maintain switching speed with the lower value of V+.

Current drawn from V- for the MAX543 and optocoupler is 3.5mA at a 100kHz clock rate when all data bits are set to 0. V+ current drops to 0 (excluding reference and op-amp current) when no new data is being loaded and CLOCK, SERIAL DATA, and $\overline{LOAD}$ are static high.

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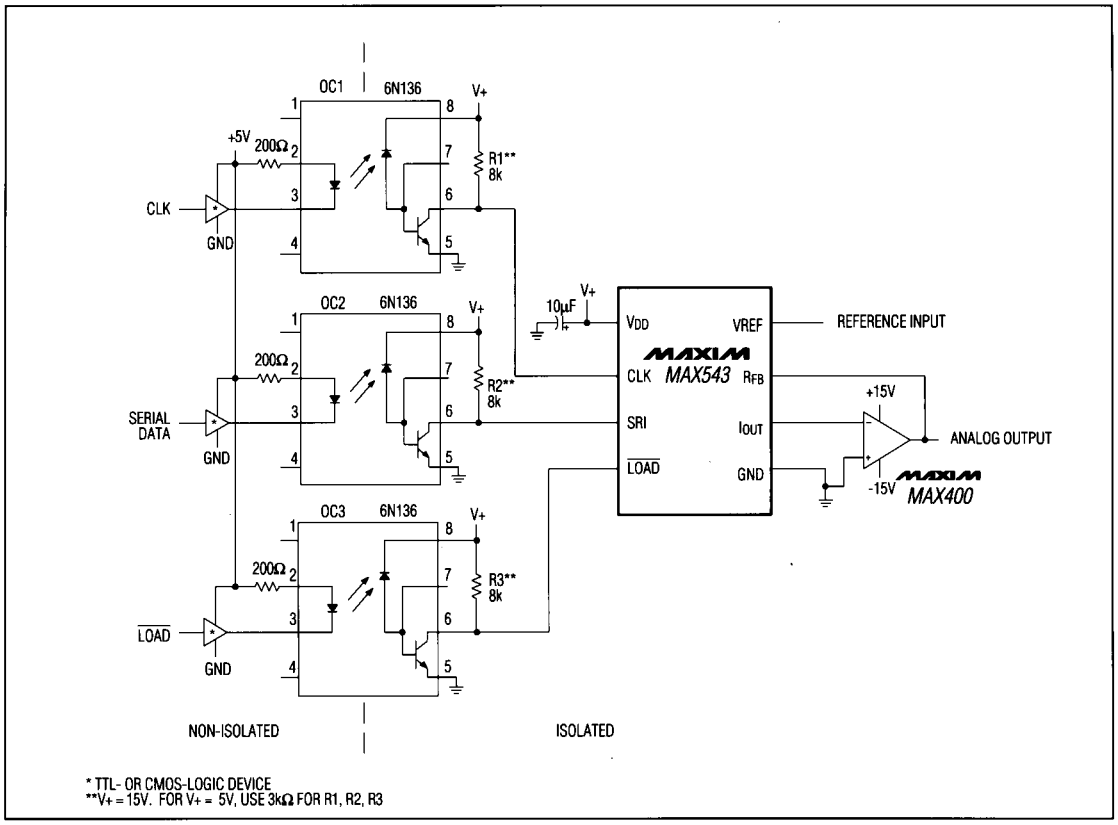

Figure 6a. MAX543 Opto-Coupled Application

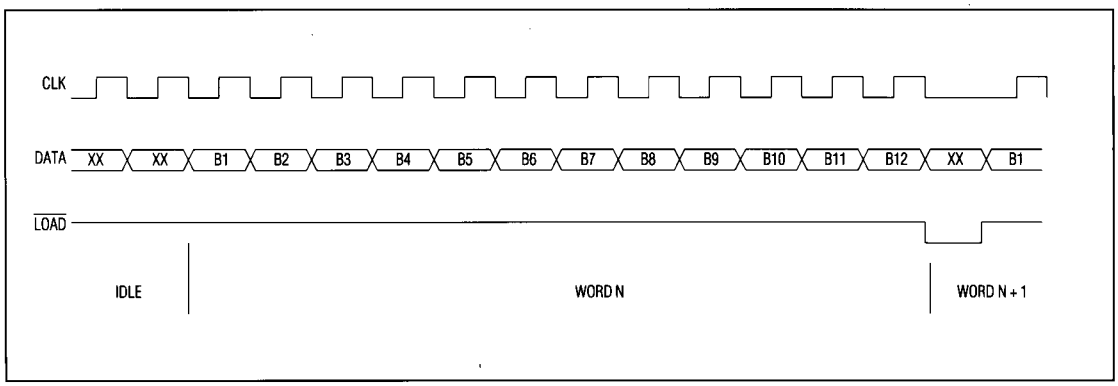

Figure 6b. MAX543 Opto-Isolated Timing

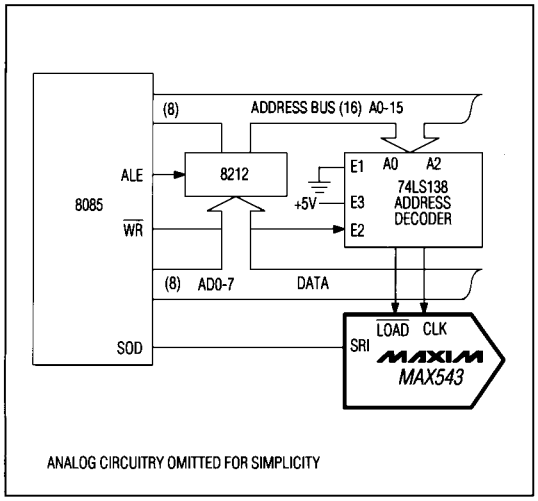

Figure 7. MAX543 8085 Interface

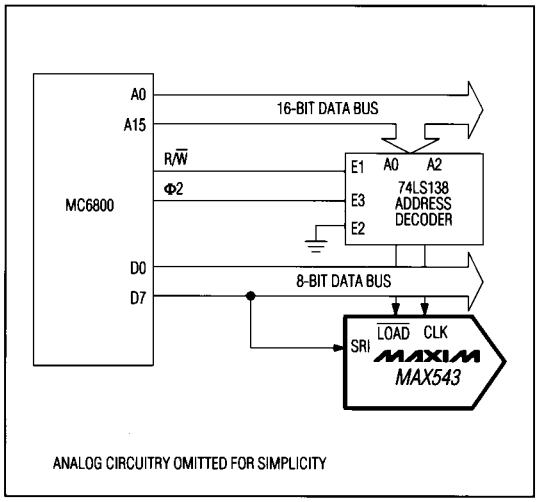

Figure 8. MAX543 MC6800 Interface

Microprocessor Interfacing

Interfacing to the 8085

Figure 7 shows the MAX543 interfacing to the 8085 µP. The SOD line from the 8085 sends serial data to the DAC. This data is clocked into the MAX543 by executing memory-write instructions. Generate the CLK input for the DAC by decoding address 8000 and $\overline{WR}$ signal. The data is transferred into the DAC register with a memeory-write instruction to address A000, which brings $\overline{LOAD}$ low. The data for the MAX543 is stored in right-justified format in registers H and L of the 8085.

Interfacing to the MC6800

Figure 8 shows the MAX543 interfacing to the MC6800 µP. Transfer the data into the MAX543 by executing successive memory-write instructions while changing the data between writes to construct the serial data to the DAC.

The D7 data line is used for the SRI signal. The lower half of the memory location 0000 holds the four MSB data bits, and the 0001 location holds the eight LSB data bits. The memory address 2000, R/$\overline{W}$, and 02 are decoded to genenrate the CLK signal for the DAC with each memory write. Similarly, a memory write to address 4000 transfers data into the DAC register by bringing the MAX543's $\overline{LOAD}$ input low.

Applications Information

Output Amplifier Offset

For best linearity, terminate I_{OUT} and GND at exactly 0V. In most applications, I_{OUT} is connected to the summing junction of an inverting op amp. The amplifiers's input offset voltage can degrade the DAC's linearity by causing I_{OUT} to be terminated to a non-zero voltage. The resulting error is:

$$\text{Error Voltage} = V_{OS}(1 + R_{FB}/R_O)$$

where V_{OS} is the op amp's offset and R_O is the DAC's output resistance. R_O is a function of the digital input code, and varies from approximately 11kΩ to 33kΩ. The error voltage range is then typically 4/3V_{OS} to 2V_{OS} – a change of 2/3V_{OS}. Therefore, an amplifier with 3mV of offset will degrade the linearity by 2mV – almost a full LSB with a 10V reference voltage. For best linearity, use a low-offset amplifier such as the MAX400, otherwise the amplifier offset must be trimmed to zero. A good guide rule is that V_{OS} should be no more than 1/10LSB.

The output-amplifer input bias current (I_B) can also limit performance since I_B X R_{FB} generates an offset error. Therefore, I_B should be much less than the DAC output current for 1LSB, typically 250nA with VREF = 10V. One tenth of this value, 25nA, is recommended. Offset and linearity can also be impaired if the output-amplifier non-

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inverting input is grounded through a "bias-current compensation resistor." This resistor adds to the offset at this pin and should not be used. Best performance is obtained when the noninverting input is directly connected to ground.

Dynamic Considerations

In static or DC applications, the output amplifier's AC characteristics are not critical. In higher-speed applications where either the reference input is an AC signal or the DAC output must quickly settle to a new programmmed value, the AC parameters of the output op amp must be considered.

Another error source in dynamic applications is parasitic coupling of the signal from the VREF pin to I_{OUT}. This is normally a function of board layout and lead-to-lead package capacitance. Noise signals can also be injected into the DAC outputs when the digital inputs are switched. This digital feedthrough is usually dependent on ciruit-board layout and on-chip capacitive coupling. Layout-induced feedthrough can be minimized with guard traces beween digital inputs, VREF, and I_{OUT} pins.

The DAC output follows the digital inputs when the $\overline{LOAD}$ pin is low. In this mode, invalid outputs and voltage glitches can appear at the DAC output. Keeping the $\overline{LOAD}$ input high until all the data is shifted into the MAX543 eliminates this problem.

Compensation

A compenation capacitor, C1, may be required when the DAC is used with a high-speed output amplifier. The purpose of the capacitor is to cancel the pole formed by the DAC output capacitance, C_{OUT}, and the internal feedback resistor, R_{FB}. Its value depends on the type of op amp used, but typically ranges from 10pF to 33pF. Too small a value causes output ringing, while excess capacitance overdamps the output. The size of C1 can be minimized and the output-voltage settling time improved by keeping the cirucit-boad trace and stray capacitance at I_{OUT} as low as possible.

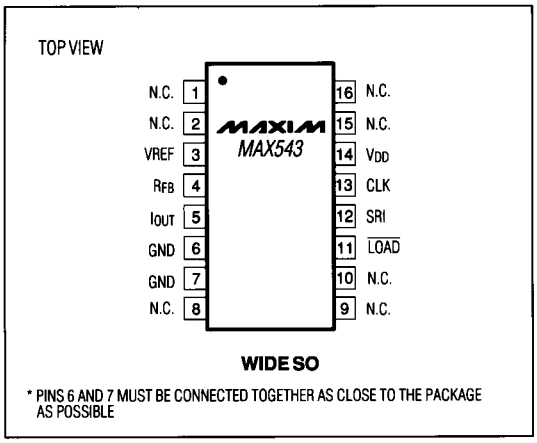
Grounding and Bypassing

Since I_{OUT} and the noninverting input of the output amplifier are sensitive to offset voltages, nodes that are to be grounded should be connected directly to "single point" ground through a separate, low-resistance (less than 0.2Ω) connection. The current at I_{OUT} and GND varies with input code, creating a code-dependent error if these terminals are connected to ground (or a "virtural ground") through a resistive path.

Connect a 1µF bypass capacitor in parallel with a 0.01µF ceramic capacitor across V_{DD} and GND, and as close to the pins as possible.

The MAX543 has high-impedance digital inputs. To minimize noise pick-up, tie them to either V_{DD} or GND when not in use. It is good practice to connect active inputs to V_{DD} or GND through high-value resistors (1MΩ) to prevent static charge accumulation if the pins are left floating, such as when a circuit card is left unconnected.

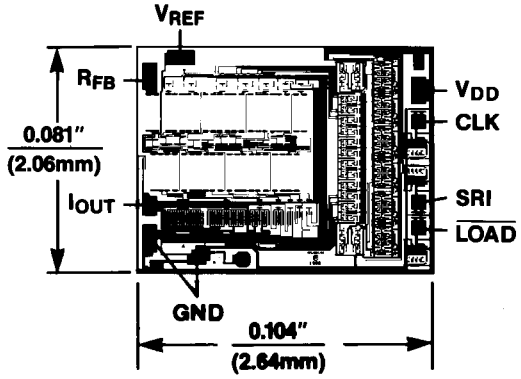
Pin Configurations (continued)



Ordering Information (continued)

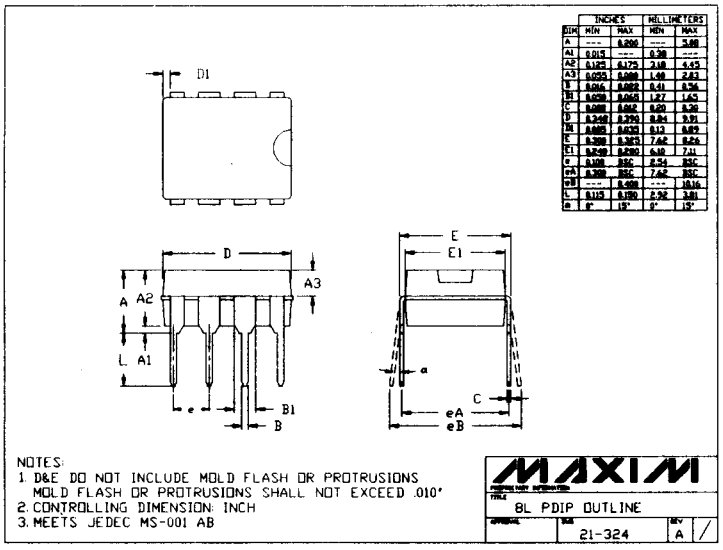
PART	TEMP. RANGE	PIN-PACKAGE	LINEARITY (LSBs)
MAX543AESA	-40°C to +85°C	8 SO	±1/2
MAX543BESA	-40°C to +85°C	8 SO	±1
MAX543AEWE	-40°C to +85°C	16 Wide SO	±1/2
MAX543BEWE	-40°C to +85°C	16 Wide SO	±1
MAX543AEJA	-40°C to +85°C	8 CERDIP	±1/2
MAX543BEJA	-40°C to +85°C	8 CERDIP	±1
MAX543AMJA	-55°C to +125°C	8 CERDIP	±1/2
MAX543BMJA	-55°C to +125°C	8 CERDIP	±1

Chip Topography

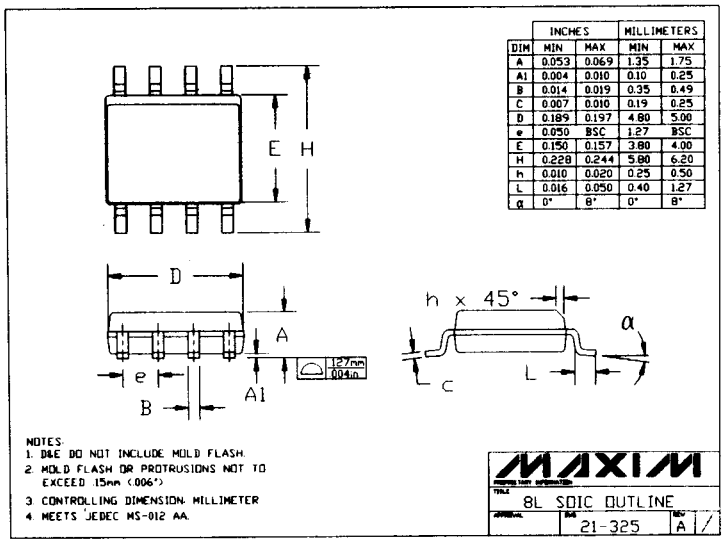


CMOS, 12-Bit, Serial-Input Multiplying DAC

Package Information



DIM	INCHES MIN	INCHES MAX	MILLIMETERS MIN	MILLIMETERS MAX
A	----	0.200	----	5.080
A1	0.015	----	0.38	----
A2	0.125	0.175	3.18	4.45
A3	0.055	0.080	1.40	2.03
B	0.016	0.022	0.41	0.56
B1	0.050	0.065	1.27	1.65
C	0.008	0.012	0.20	0.30
D	0.240	0.370	6.04	9.91
DE	0.005	0.013	0.13	0.89
E	0.290	0.325	7.62	8.26
E1	0.240	0.280	6.10	7.11
e	0.100	BSC	2.54	BSC
eA	0.300	BSC	7.62	BSC
eB	----	0.400	----	10.16
L	0.115	0.150	2.92	3.81
a	0°	15°	0°	15°



DIM	INCHES MIN	INCHES MAX	MILLIMETERS MIN	MILLIMETERS MAX
A	0.053	0.069	1.35	1.75
A1	0.004	0.010	0.10	0.25
B	0.014	0.019	0.35	0.49
C	0.007	0.010	0.19	0.25
D	0.189	0.197	4.80	5.00
e	0.050	BSC	1.27	BSC
E	0.150	0.157	3.80	4.00
H	0.228	0.244	5.80	6.20
h	0.010	0.020	0.25	0.50
L	0.016	0.050	0.40	1.27
α	0°	8°	0°	8°

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