

Low-Voltage, SPST, CMOS Analog Switches

ABSOLUTE MAXIMUM RATINGS

(Voltages Referenced to GND)

V+	-0.3V to +13V
Voltage into Any Terminal (Note 1)	-0.3V to (V+ + 0.3V) or ±10mA (whichever occurs first)
Continuous Current into Any Terminal	±10mA
Peak Current, NO or COM (pulsed at 1ms, 10% duty cycle)	±20mA
ESD per Method 3015.7	>2000V
Continuous Power Dissipation (T _A = +70°C)	
5-Pin SC70-5 (derate 2.5mW/°C above +70°C)	200mW
5-Pin SOT23-5 (derate 7.1mW/°C above +70°C)	571mW

8-Pin SO (derate 5.88mW/°C above +70°C)	471mW
8-Pin Plastic DIP (derate 9.09mW/°C above +70°C)	727mW
8-Pin CERDIP (derate 8.00mW/°C above +70°C)	640mW
Operating Temperature Ranges	
MAX4501C_/MAX4502C_	0°C to +70°C
MAX4501E_/MAX4502E_	-40°C to +85°C
MAX4501MJA/MAX4502MJA	-55°C to +125°C
Storage Temperature Range	-65°C to +150°C
Lead Temperature (soldering, 10s)	+300°C

Note 1: Voltages exceeding V+ or GND on any signal terminal are clamped by internal diodes. Limit forward-diode current to maximum current rating.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS—+5V Supply

(V+ = +4.5V to +5.5V, V_{INH} = 2.4V, V_{INL} = 0.8V, T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are at T_A = +25°C.) (Note 2)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
ANALOG SWITCH						
Analog Signal Range	V _{COM} , V _{NO} , V _{NC}		0		V+	V
COM to NO or NC On-Resistance	R _{ON}	V _{COM} = 3.5V, I _{COM} = 1mA	T _A = +25°C		90	250
			T _A = T _{MIN} to T _{MAX}		350	
NO or NC Off-Leakage Current (Notes 3, 4)	I _{NO(OFF)} , I _{NC(OFF)}	V+ = 5.5V, V _{COM} = 1V, V _{NO} or V _{NC} = 4.5V	T _A = +25°C		-1	0.01
			T _A = T _{MIN} to T _{MAX}	C, E	-10	10
				M	-100	100
COM Off-Leakage Current (Notes 3, 4)	I _{COM(OFF)}	V+ = 5.5V, V _{COM} = 1V, V _{NO} or V _{NC} = 4.5V	T _A = +25°C		-1	0.01
			T _A = T _{MIN} to T _{MAX}	C, E	-10	10
				M	-100	100
COM On-Leakage Current (Notes 3, 4)	I _{COM(ON)}	V+ = 5.5V, V _{COM} = 1V, 4.5V	T _A = +25°C		-2	0.01
			T _A = T _{MIN} to T _{MAX}	C, E	-20	20
				M	-200	200
DIGITAL I/O						
Input Logic High	V _{INH}		2.4		V+	V
Input Logic Low	V _{INL}		0		0.8	V
Input Current Logic High or Low	I _{INH} , I _{INL}	V _{IN} = V+, 0	-1	0.03	1	μA
SWITCH DYNAMIC CHARACTERISTICS						
Turn-On Time	t _{ON}	V _{NO} = V _{NC} = 1.5V, V _{IN} = 3V, R _L = 1kΩ, C _L = 35pF, Figure 1	T _A = +25°C		16	75
			T _A = T _{MIN} to T _{MAX}		150	
Turn-Off Time	t _{OFF}	V _{NO} = V _{NC} = 1.5V, V _{IN} = 3V, R _L = 1kΩ, C _L = 35pF, Figure 1	T _A = +25°C		10	50
			T _A = T _{MIN} to T _{MAX}		150	

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MAX4501/MAX4502

ELECTRICAL CHARACTERISTICS—+5V Supply (continued)

(V+ = +4.5V to +5.5V, VINH = 2.4V, VINL = 0.8V, TA = TMIN to TMAX, unless otherwise noted. Typical values are at TA = +25°C.) (Note 2)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
SWITCH DYNAMIC CHARACTERISTICS (continued)						
Charge Injection (Note 5)	Q	CL = 1nF, VNO = 0, RS = 0Ω, TA = +25°C, Figure 2		1	10	pC
Off-Isolation	VISO	RL = 50Ω, CL = 15pF, VNO = 1VRMS, f = 100kHz, TA = +25°C, Figure 3		< -100		dB
NO or NC Off-Capacitance	CNO(OFF), CNC(OFF)	f = 1MHz, Figure 4		3		pF
COM Off-Capacitance	CCOM(OFF)	f = 1MHz, Figure 4		3		pF
COM On-Capacitance	CCOM(ON)	f = 1MHz, Figure 4		8		pF
POWER SUPPLY						
V+ Supply Current	I+	VIN = 0 or V+	TA = +25°C	-1	1	μA
			TA = TMIN to TMAX	-10	10	

ELECTRICAL CHARACTERISTICS—+12V Supply

(V+ = +11.4V to +12.6V, VINH = 5.0V, VINL = 0.8V, TA = TMIN to TMAX, unless otherwise noted. Typical values are at TA = +25°C.) (Note 2)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS	
ANALOG SWITCH							
Analog Signal Range	VCOM, VNO, VNC		0		V+	V	
COM to NO or NC On-Resistance	RON	VCOM = 10V, ICOM = 1mA	TA = +25°C	40	160	Ω	
			TA = TMIN to TMAX		200		
NO or NC Off-Leakage Current (Notes 3, 4)	INO(OFF), INC(OFF)	VCOM = 10V, VNO or VNC = 1V, V+ = +12.6V	TA = +25°C	-5	5	nA	
			TA = TMIN to TMAX	C, E	-50		50
				M	-500		500
COM Off-Leakage Current (Notes 3, 4)	ICOM(OFF)	VCOM = 10V, VNO or VNC = 1V, V+ = +12.6V	TA = +25°C	-5	5	nA	
			TA = TMIN to TMAX	C, E	-50		50
				M	-500		500
COM On-Leakage Current (Notes 3, 4)	ICOM(ON)	VCOM = 10V, V+ = +12.6V	TA = +25°C	-10	10	nA	
			TA = TMIN to TMAX	C, E	-100		100
				M	-1000		1000
DIGITAL I/O							
Input Logic High	VINH		5.0		V+	V	
Input Logic Low	VINL		0		0.8	V	
Input Current Logic High or Low	IINH, IINL	VIN = 0 or V+	-1	0.03	1	μA	
POWER SUPPLY							
V+ Supply Current	I+	IN = 0 or V+	TA = +25°C	-1	1	μA	
			TA = TMIN to TMAX	-10	10		

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ELECTRICAL CHARACTERISTICS—+3V Supply

($V_+ = +3.0V$ to $+3.6V$, $V_{INH} = 2.4V$, $V_{INL} = 0.8V$, $T_A = T_{MIN}$ to T_{MAX} , unless otherwise noted. Typical values are at $T_A = +25^\circ C$.) (Note 2)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS	
ANALOG SWITCH							
Analog Signal Range	V_{COM} , V_{NO} , V_{NC}		0		V_+	V	
COM to NO or NC On-Resistance	R_{ON}	$V_{COM} = 1.5V$, $I_{COM} = 0.1mA$	$T_A = +25^\circ C$		175	600	Ω
			$T_A = T_{MIN}$ to T_{MAX}			800	
DIGITAL I/O							
Input Logic High	V_{INH}		2.4		V_+	V	
Input Logic Low	V_{INL}		0		0.8	V	
Input Current Logic High or Low	I_{INH} , I_{INL}	$V_{IN} = 0$ or V_+	-1.00	0.03	1.00	μA	
SWITCH DYNAMIC CHARACTERISTICS							
Turn-On Time (Note 5)	t_{ON}	$V_{NO} = V_{NC} = 1.5V$, $V_{IN} = 3V$, $R_L = 1k\Omega$, Figure 1	$T_A = +25^\circ C$		45	300	ns
			$T_A = T_{MIN}$ to T_{MAX}			500	
Turn-Off Time (Note 5)	t_{OFF}	$V_{NO} = V_{NC} = 1.5V$, $V_{IN} = 3V$, $R_L = 1k\Omega$, Figure 1	$T_A = +25^\circ C$		10	125	ns
			$T_A = T_{MIN}$ to T_{MAX}			175	
Charge Injection (Note 5)	Q	$C_L = 1nF$, $T_A = +25^\circ C$, Figure 2		0.5	10	pC	
POWER SUPPLY							
V_+ Supply Current	I_+	$I_N = 0$ or V_+	$T_A = +25^\circ C$		-1	1	μA
			$T_A = T_{MIN}$ to T_{MAX}		-10	10	

Note 2: Algebraic convention is used in this data sheet; the most negative value is shown in the minimum column.

Note 3: Leakage parameters are 100% tested at maximum-rated hot operating temperature, and are guaranteed by correlation at $+25^\circ C$.

Note 4: SOT and SC70 packaged parts are 100% tested at $+25^\circ C$. Limits at maximum and minimum rated temperature are guaranteed by design and correlation limits at $+25^\circ C$.

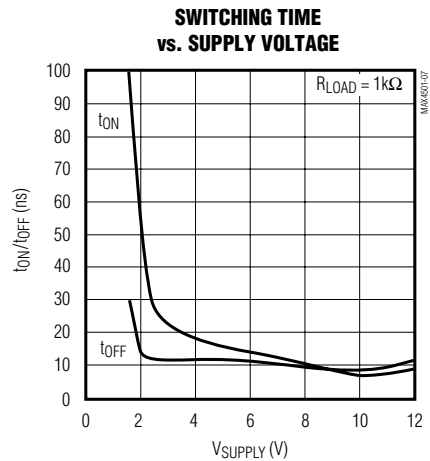
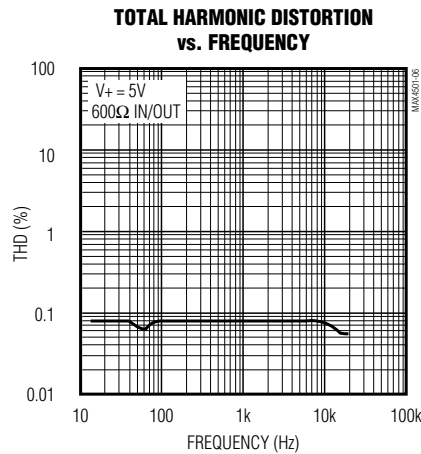
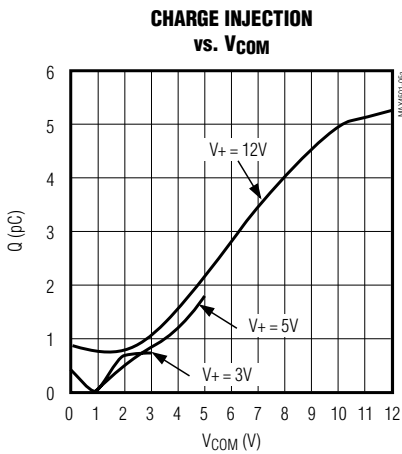
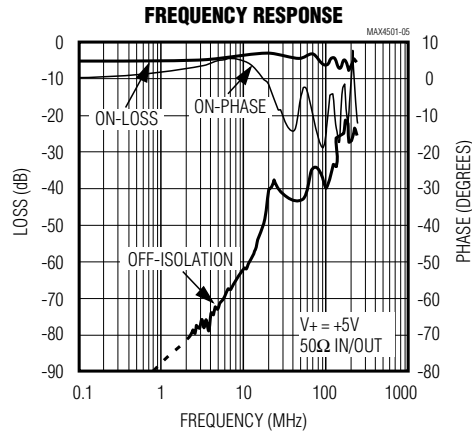
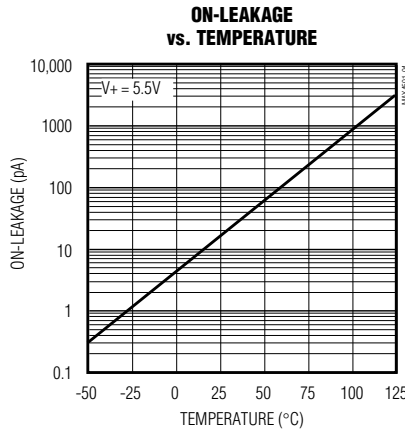
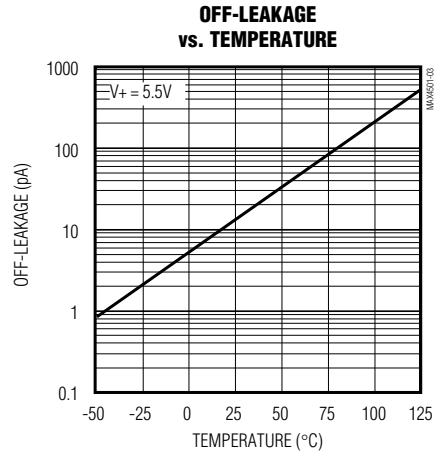
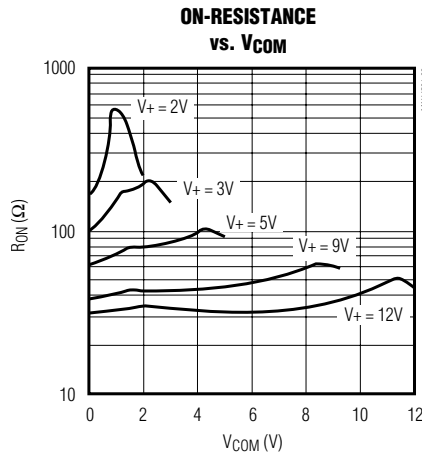
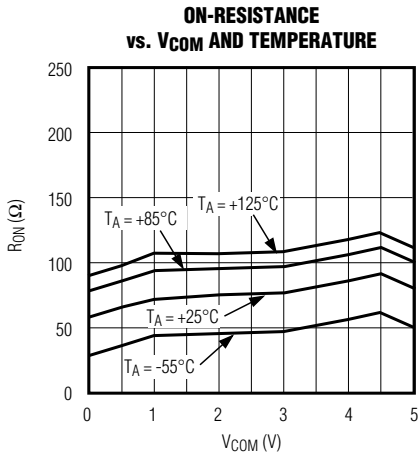
Note 5: Guaranteed, not production tested.

Low-Voltage, SPST, CMOS Analog Switches

Typical Operating Characteristics

($V_+ = +5V$, $GND = 0$, $T_A = +25^\circ C$, unless otherwise noted.)

MAX4501/MAX4502



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Pin Description

PIN				NAME	FUNCTION
MAX4501		MAX4502			
SO/DIP	SC70-5/SOT23-5	SO/DIP	SC70-5/SOT23-5		
1	1	1	1	COM	Analog Switch Common Terminal
2, 3, 5	—	2, 3, 5	—	N.C.	No Connection. Not internally connected.
4	5	4	5	V+	Positive Supply-Voltage Input (analog and digital)
6	4	6	4	IN	Digital Control Input
7	3	7	3	GND	Ground
8	2	—	—	NO	Analog Switch (normally open)
—	—	8	2	NC	Analog Switch (normally closed)

Note: NO, NC, and COM pins are identical and interchangeable. Any may be considered as an input or an output; signals pass equally well in both directions.

Applications Information

Power-Supply Considerations

The MAX4501/MAX4502 are constructed like most CMOS analog switches, except they have only two supply pins: V+ and GND. V+ and GND drive the internal CMOS switches and set the analog voltage limits of the switch. Reverse ESD-protection diodes are internally connected between each analog signal pin and both V+ and GND. One of these diodes conducts if any analog signal exceeds V+ or GND. During normal operation, these and other reverse-biased ESD diodes leak, forming the only current drawn from V+ or GND.

Virtually all the analog leakage current comes from the ESD diodes. Although the ESD diodes on a given signal pin are identical and therefore fairly well balanced, they are reverse biased differently. Each is biased by either V+ or GND and the analog signal. This means their leakages will vary as the signal varies. The *difference* in the two diode leakages to the V+ and GND pins constitutes the analog signal-path leakage current. All analog leakage current flows between each pin and one of the supply terminals, not to the other switch terminal. This is why both sides of a given switch can show leakage currents of the same or opposite polarity.

There is no connection between the analog-signal paths and V+ or GND.

V+ and GND also power the internal logic and logic-level translators, and set the input logic limits. The logic-level translators convert the logic levels to switched V+ and GND signals to drive the analog sig-

nal gates. This drive signal is the only connection between the logic supplies (and signals) and the analog supplies. COM, NO, and NC pins have ESD-protection diodes to V+ and GND.

The logic-level thresholds are CMOS/TTL compatible when V+ is +5V. As V+ rises, the threshold increases slightly. When V+ reaches +12V, the logic-level threshold is about 3V—above the TTL guaranteed high-level minimum of 2.8V, but still compatible with CMOS outputs.

Do not connect the MAX4501/MAX4502's V+ pin to +3V and then connect the logic-level pins to TTL logic-level signals. TTL levels can exceed +3V and violate the absolute maximum ratings, damaging the part and/or external circuits.

High-Frequency Performance

In 50Ω systems, signal response is reasonably flat up to 250MHz (see *Typical Operating Characteristics*). Above 20MHz, the on-response has several minor peaks that are highly layout dependent. The problem is not in turning the switch on; it's in turning it off. The off-state switch acts like a capacitor and passes higher frequencies with less attenuation. At 10MHz, off-isolation is about -60dB in 50Ω systems, decreasing approximately 20dB per decade as frequency increases. Higher circuit impedances also cause off-isolation to decrease. Adjacent channel attenuation is about 3dB above that of a bare IC socket, and is due entirely to capacitive coupling.

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Test Circuits/Timing Diagrams

MAX4501/MAX4502

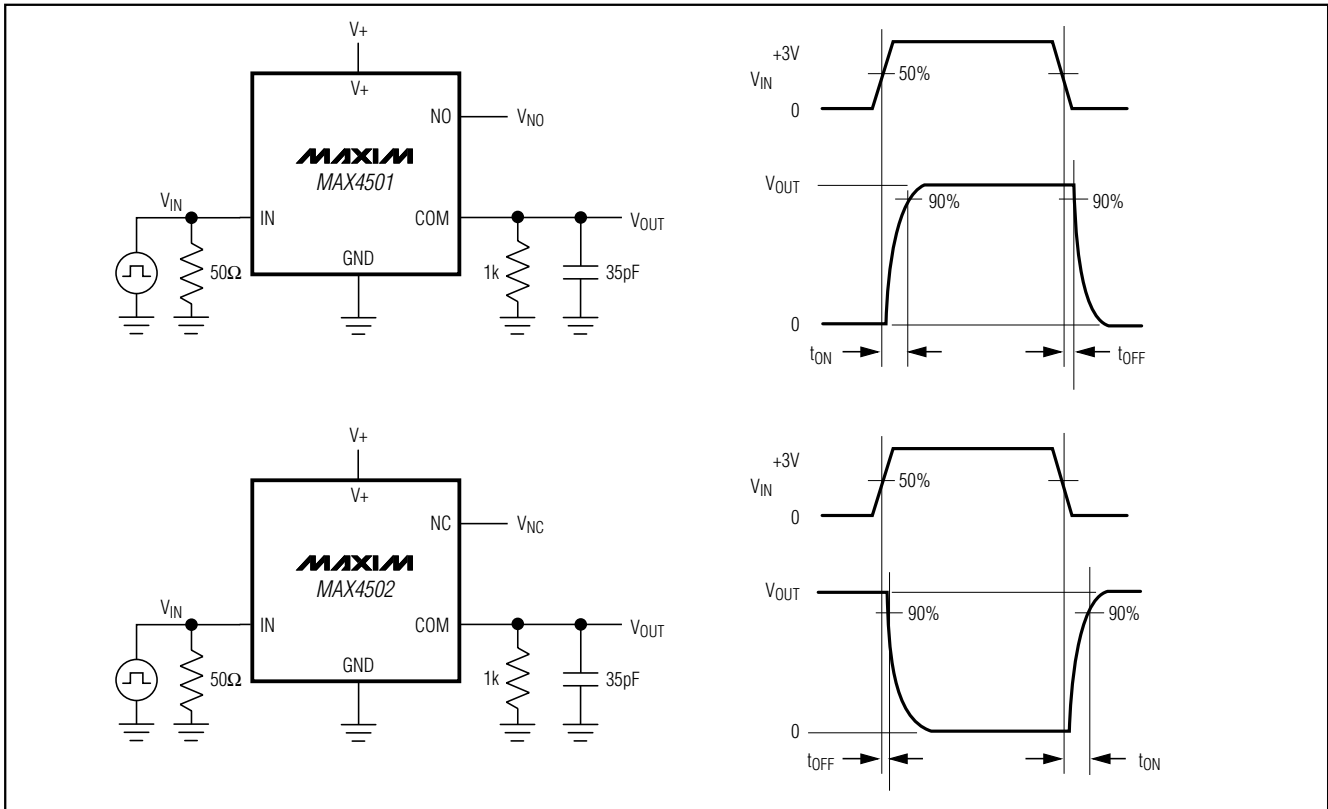


Figure 1. Switching Times

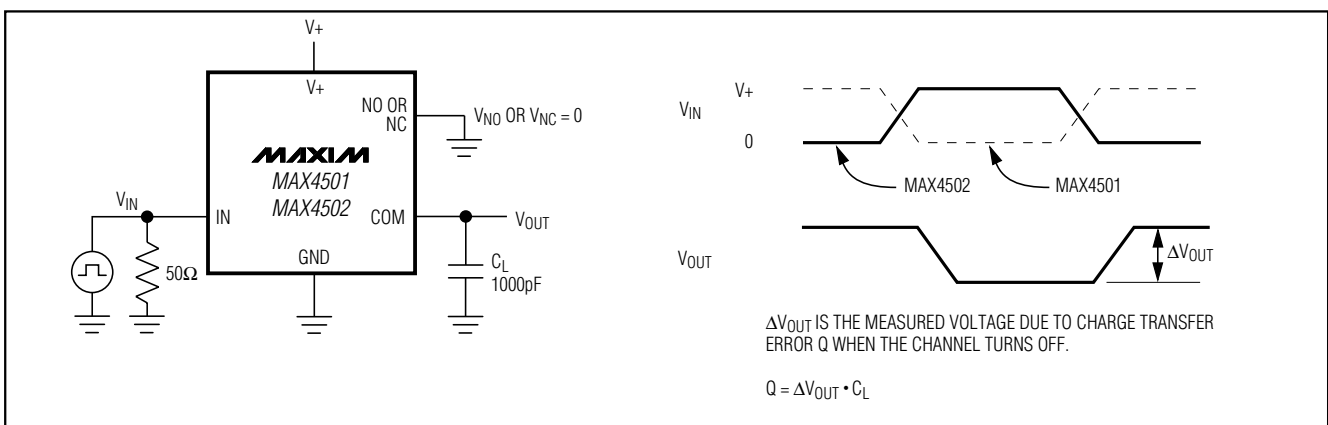


Figure 2. Charge Injection

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Test Circuits/Timing Diagrams (continued)

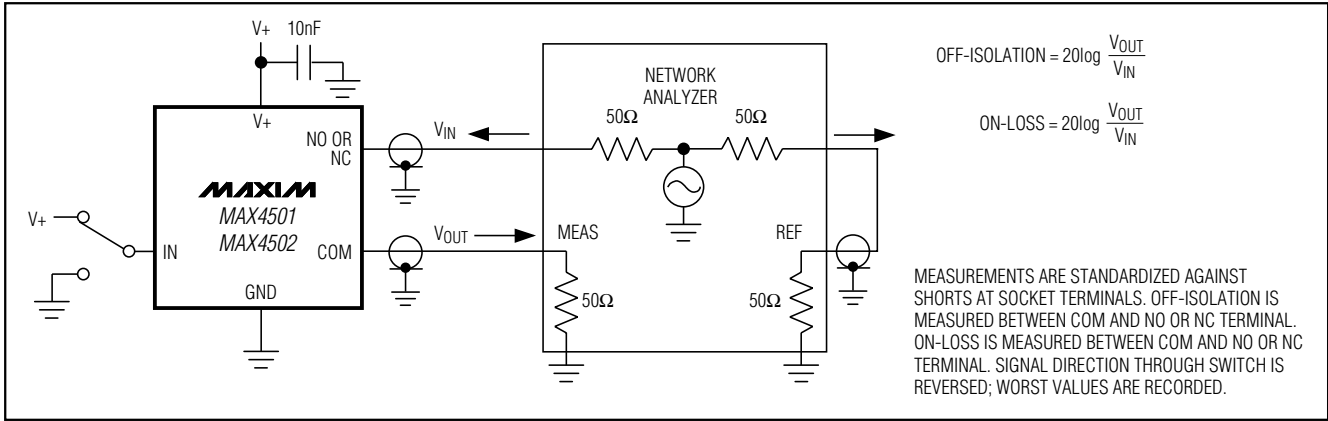


Figure 3. Off-Isolation and On-Loss

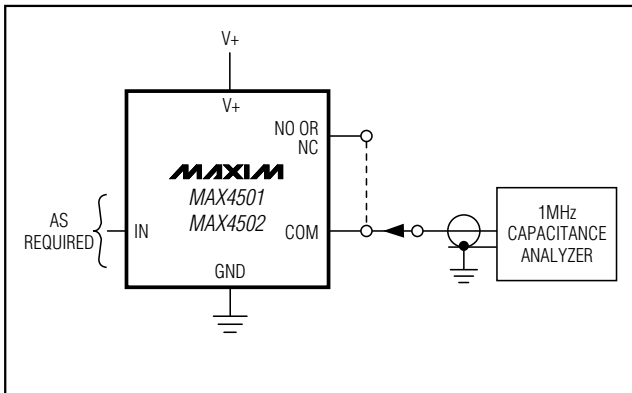
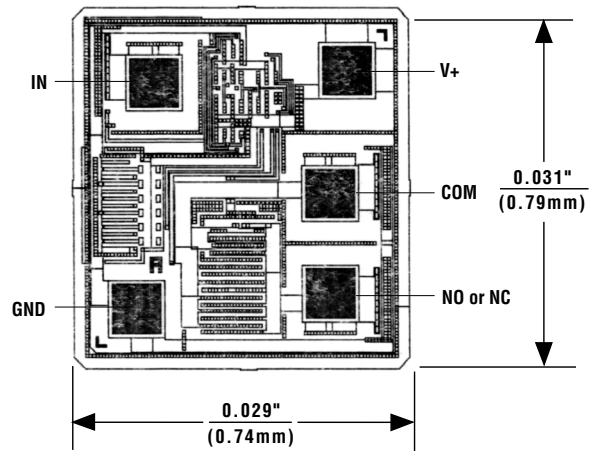


Figure 4. NO, NC, and COM Capacitance

Chip Topography



TRANSISTOR COUNT: 17
SUBSTRATE CONNECTED TO V+

Ordering Information (continued)

PART	TEMP. RANGE	PIN-PACKAGE	TOP MARK
MAX4502CUK-T	0°C to +70°C	5 SOT23-5	AAAB
MAX4502CSA	0°C to +70°C	8 SO	—
MAX4502CPA	0°C to +70°C	8 Plastic DIP	—
MAX4502C/D	0°C to +70°C	Dice*	—
MAX4502EXK-T	-40°C to +85°C	5 SC70-5	AAF
MAX4502EUK-T	-40°C to +85°C	5 SOT23-5	AAAB
MAX4502ESA	-40°C to +85°C	8 SO	—
MAX4502EPA	-40°C to +85°C	8 Plastic DIP	—
MAX4502MJA	-55°C to +125°C	8 CERDIP**	—

*Contact factory for dice specifications.

**Contact factory for availability.

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