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REVISION HISTORY

7/2016—Rev. B to Rev. C

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Deleted PCB Layout Section and Figure 50; Renumbered Sequentially ... 25
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9/2005—Rev. A to Rev. B

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11/2001—Rev. 0 to Rev. A

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10/1998—Revision 0: Initial Version

SPECIFICATIONS

V_S = ±5 V, T_A = +25°C, R_L = 1 kΩ, unless otherwise noted.

Table 1.

Parameter	Test Conditions/Comments	Min	Typ	Max	Unit
DYNAMIC PERFORMANCE					
−3 dB Bandwidth	200 mV p-p, R_L = 150 Ω	150/125	225/200		MHz
	2 V p-p, R_L = 150 Ω		100/125		MHz
Gain Flatness	0.1 dB, 200 mV p-p, R_L = 150 Ω		25/40		MHz
	0.1 dB, 2 V p-p, R_L = 150 Ω		20/40		MHz
Propagation Delay	2 V p-p, R_L = 150 Ω		5		ns
Settling Time	0.1%, 2 V step, R_L = 150 Ω		40		ns
Slew Rate	2 V step, R_L = 150 Ω		375/450		V/µs
NOISE/DISTORTION PERFORMANCE					
Differential Gain Error	NTSC or PAL, R_L = 1 kΩ		0.05		%
	NTSC or PAL, R_L = 150 Ω		0.05		%
Differential Phase Error	NTSC or PAL, R_L = 1 kΩ		0.05		Degrees
	NTSC or PAL, R_L = 150 Ω		0.05		Degrees
Crosstalk, All Hostile	f = 5 MHz		−70/−64		dB
	f = 10 MHz		−60/−52		dB
Off Isolation, Input-to-Output	f = 5 MHz, R_L = 150 Ω, one channel		−98		dB
Input Voltage Noise	0.01 MHz to 50 MHz		16/18		nV/$\sqrt{Hz}$
DC PERFORMANCE					
Gain Error	No load		0.05/0.2	0.08/0.6	%
	R_L = 1 kΩ		0.05/0.2		%
	R_L = 150 Ω		0.2/0.35		%
Gain Matching	No load, channel-to-channel		0.01/0.5	0.04/1	%
	R_L = 1 kΩ channel-to-channel		0.01/0.5		%
Gain Temperature Coefficient			0.75/1.5		ppm/°C
OUTPUT CHARACTERISTICS					
Output Impedance	DC, enabled		0.2		Ω
	Disabled		10		MΩ
Output Disable Capacitance	Disabled		5		pF
Output Leakage Current	Disabled		1		µA
Output Voltage Range	No load	±3.0	±3.3		V
Voltage Range	I_{OUT} = 20 mA	±2.5	±3		V
	Short-circuit current		65		mA
INPUT CHARACTERISTICS					
Input Offset Voltage	Worst case (all configurations)		3	15	mV
	Temperature coefficient		10		µV/°C
Input Voltage Range	No load	±3/±1.5	±3.5		V
Input Capacitance	Any switch configuration		5		pF
Input Resistance		1	10		MΩ
Input Bias Current	Per output selected		2	5	µA
SWITCHING CHARACTERISTICS					
Enable On Time			60		ns
Switching Time, 2 V Step	50% $\overline{\text{UPDATE}}$ to 1% settling		50		ns
Switching Transient (Glitch)			20/30		mV p-p

Parameter	Test Conditions/Comments	Min	Typ	Max	Unit
POWER SUPPLIES					
Supply Current	AVCC, outputs enabled, no load		70/80		mA
	AVCC, outputs disabled		27/30		mA
	AVEE, outputs enabled, no load		70/80		mA
	AVEE, outputs disabled		27/30		mA
	DVCC, outputs enabled, no load		16		mA
Supply Voltage Range			±4.5 to ±5.5		V
PSRR	DC	64	80		dB
	f = 100 kHz		66		dB
	f = 1 MHz		46		dB
OPERATING TEMPERATURE RANGE					
Temperature Range	Operating (still air)		−40 to +85		°C
θ_{JA}	Operating (still air)		40		°C/W

TIMING CHARACTERISTICS (SERIAL)

Table 2. Timing Characteristics

Parameter	Symbol	Min	Typ	Max	Unit
Serial Data Setup Time	t_1	20			ns
CLK Pulse Width	t_2	100			ns
Serial Data Hold Time	t_3	20			ns
CLK Pulse Separation, Serial Mode	t_4	100			ns
CLK to $\overline{\text{UPDATE}}$ Delay	t_5	0			ns
$\overline{\text{UPDATE}}$ Pulse Width	t_6	50			ns
CLK to DATA OUT Valid, Serial Mode	t_7			200	ns
Propagation Delay, $\overline{\text{UPDATE}}$ to Switch On or Off				50	ns
Data Load Time, CLK = 5 MHz, Serial Mode			16		μs
CLK, $\overline{\text{UPDATE}}$ Rise and Fall Times				100	ns
$\overline{\text{RESET}}$ Time				200	ns

Table 3. Logic Levels

V_{IH}	V_{IL}	V_{OH}	V_{OL}	I_{IH}	I_{IL}	I_{OH}	I_{OL}
$\overline{\text{RESET}}$, $\overline{\text{SER}}$/PAR CLK, DATA IN, $\overline{\text{CE}}$, $\overline{\text{UPDATE}}$	$\overline{\text{RESET}}$, $\overline{\text{SER}}$/PAR CLK, DATA IN, $\overline{\text{CE}}$, $\overline{\text{UPDATE}}$	DATA OUT	DATA OUT	$\overline{\text{RESET}}$, $\overline{\text{SER}}$/PAR CLK, DATA IN, $\overline{\text{CE}}$, $\overline{\text{UPDATE}}$	$\overline{\text{RESET}}$, $\overline{\text{SER}}$/PAR CLK, DATA IN, $\overline{\text{CE}}$, $\overline{\text{UPDATE}}$	DATA OUT	DATA OUT
2.0 V min	0.8 V max	2.7 V min	0.5 V max	20 μA max	−400 μA min	−400 μA max	3.0 mA min

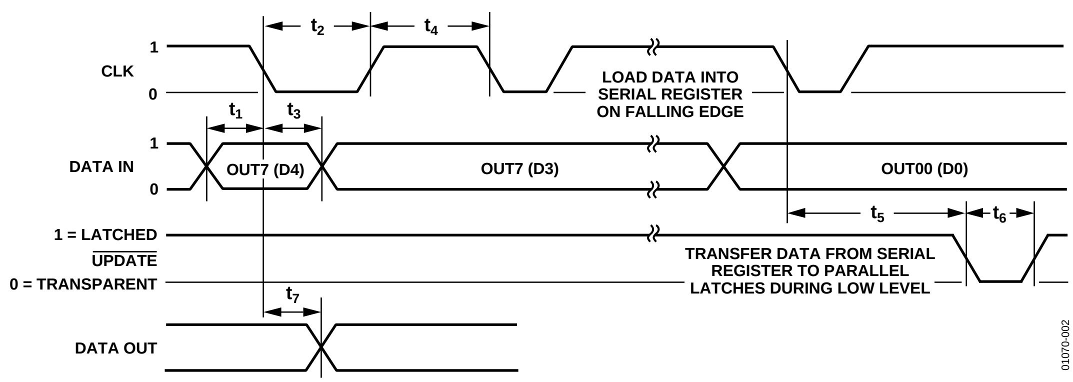


Figure 2. Timing Diagram, Serial Mode

TIMING CHARACTERISTICS (PARALLEL)

Table 4. Timing Characteristics

Parameter	Symbol	Min	Typ	Max	Unit
Data Setup Time	t_1	20			ns
CLK Pulse Width	t_2	100			ns
Data Hold Time	t_3	20			ns
CLK Pulse Separation	t_4	100			ns
CLK to $\overline{\text{UPDATE}}$ Delay	t_5	0			ns
$\overline{\text{UPDATE}}$ Pulse Width	t_6	50			ns
Propagation Delay, $\overline{\text{UPDATE}}$ to Switch On or Off				50	ns
CLK, $\overline{\text{UPDATE}}$ Rise and Fall Times				100	ns
$\overline{\text{RESET}}$ Time				200	ns

Table 5. Logic Levels

V_{IH}	V_{IL}	V_{OH}	V_{OL}	I_{IH}	I_{IL}	I_{OH}	I_{OL}
$\overline{\text{RESET}}$, $\overline{\text{SER}}$/PAR, CLK, D0, D1, D2, D3, D4, A0, A1, A2, A3, $\overline{\text{CE}}$, $\overline{\text{UPDATE}}$	$\overline{\text{RESET}}$, $\overline{\text{SER}}$/PAR, CLK, D0, D1, D2, D3, D4, A0, A1, A2, A3, $\overline{\text{CE}}$, $\overline{\text{UPDATE}}$	DATA OUT	DATA OUT	$\overline{\text{RESET}}$, $\overline{\text{SER}}$/PAR, CLK, D0, D1, D2, D3, D4, A0, A1, A2, A3, $\overline{\text{CE}}$, $\overline{\text{UPDATE}}$	$\overline{\text{RESET}}$, $\overline{\text{SER}}$/PAR, CLK, D0, D1, D2, D3, D4, A0, A1, A2, A3, $\overline{\text{CE}}$, $\overline{\text{UPDATE}}$	DATA OUT	DATA OUT
2.0 V min	0.8 V max	2.7 V min	0.5 V max	20 µA max	−400 µA min	−400 µA max	3.0 mA min

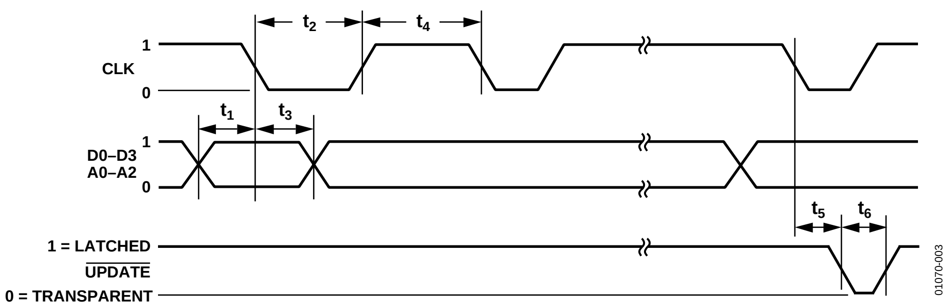


Figure 3. Timing Diagram, Parallel Mode

Table 6. Operation Truth Table

CE	UPDATE	CLK	DATA IN	DATA OUT	RESET	SER/ PAR	Operation/Comment
1	X	X	X	X	X	X	No change in logic.
0	1	f	$Data_i$	$Data_{i-80}$	1	0	The data on the serial DATA IN line is loaded into serial register. The first bit clocked into the serial register appears at DATA OUT 80 clocks later.
0	1	f	D0…D4, A0… A3	Not applicable in parallel mode	1	1	The data on the parallel data lines, D0 to D4, are loaded into the 80 bit serial shift register location addressed by A0 to A3.
0	0	X	X	X	1	X	Data in the 80-bit shift register transfers into the parallel latches that control the switch array. Latches are transparent.
X	X	X	X	X	0	X	Asynchronous operation. All outputs are disabled. Remainder of logic is unchanged.

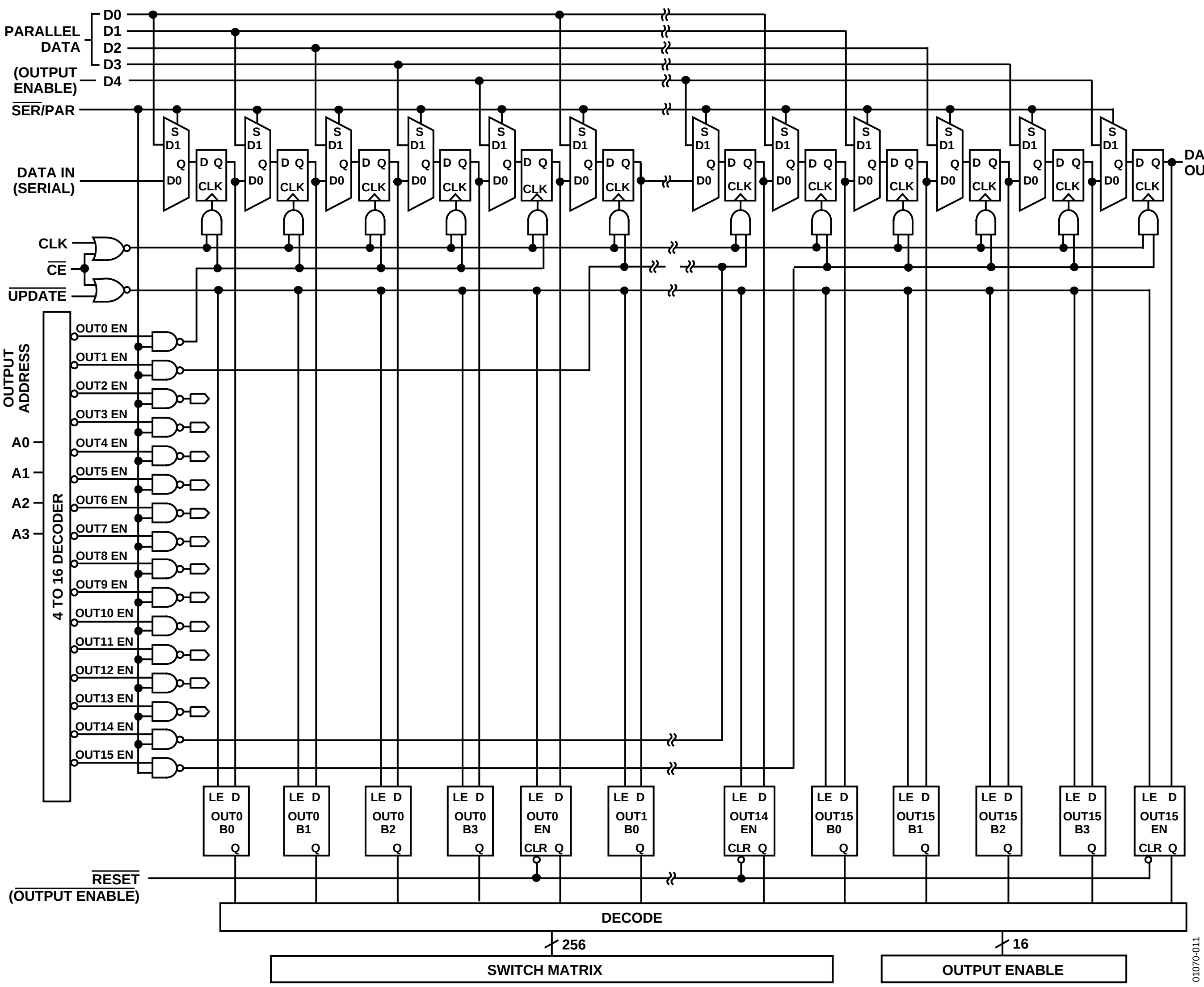


Figure 4. Logic Diagram

ABSOLUTE MAXIMUM RATINGS

Table 7.

Parameter	Rating
Supply Voltage	12.0 V
Internal Power Dissipation[1]	
AD8114/AD8115 100-Lead Plastic LQFP (ST)	2.6 W
Input Voltage	$\pm V_S$
Output Short-Circuit Duration	Observe power derating curves
Storage Temperature Range[2]	−65°C to +125°C

[1] Specification is for device in free air (T_A = 25°C). 100-lead plastic LQFP (ST): θ_{JA} = 40°C/W.
[2] Maximum reflow temperatures are to JEDEC industry standard J-STD-020.

Stresses at or above those listed under Absolute Maximum Ratings may cause permanent damage to the product. This is a stress rating only; functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

MAXIMUM POWER DISSIPATION

The maximum power that can be safely dissipated by the AD8114/AD8115 is limited by the associated rise in junction temperature. The maximum safe junction temperature for plastic encapsulated devices is determined by the glass transition temperature of the plastic, approximately 125°C. Temporarily exceeding this limit may cause a shift in parametric performance due to a change in the stresses exerted on the die by the package. Exceeding a junction temperature of 125°C for an extended period can result in device failure.

While the AD8114/AD8115 are internally short-circuit protected, this may not be sufficient to guarantee that the maximum junction temperature (125°C) is not exceeded under all conditions. To ensure proper operation, it is necessary to observe the maximum power derating curves shown in Figure 5.

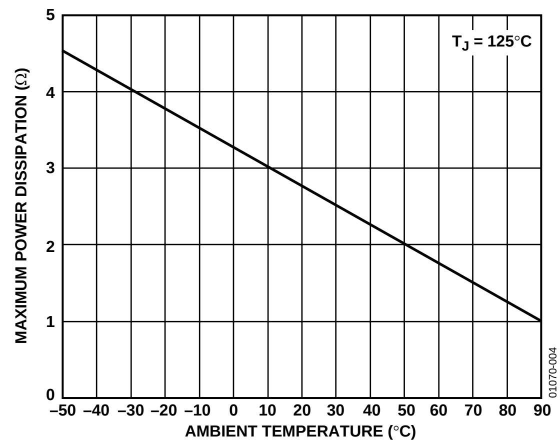
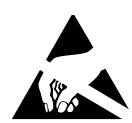


Figure 5. Maximum Power Dissipation vs. Temperature

ESD CAUTION



ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

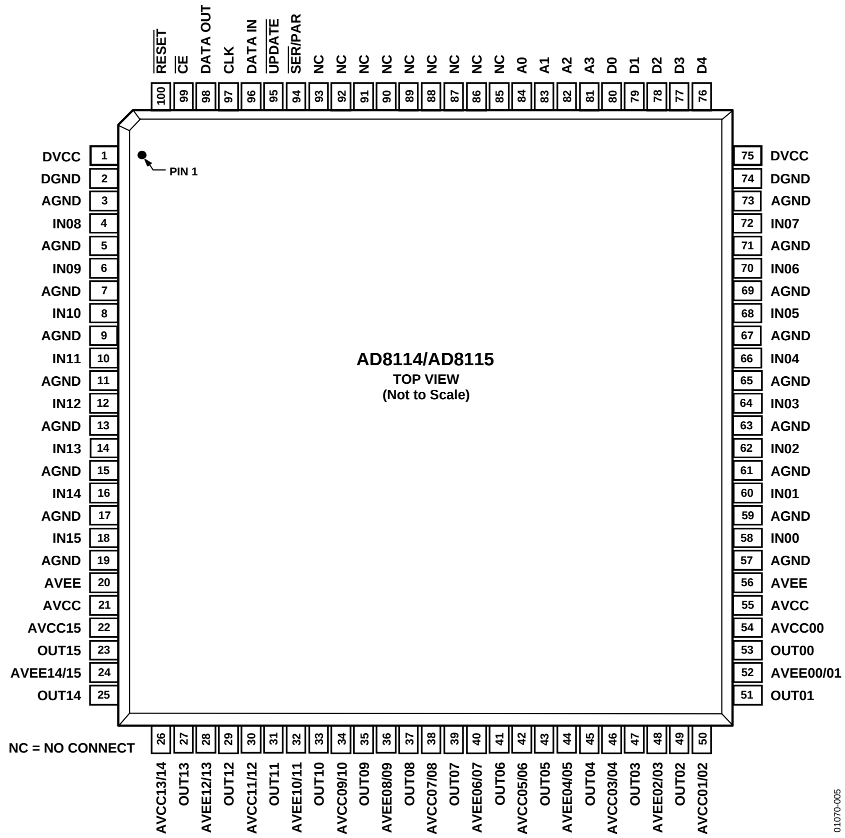


Figure 6. Pin Configuration

Table 8. Pin Function Descriptions

Pin No.	Mnemonic	Description
58, 60, 62, 64, 66, 68, 70, 72, 4, 6, 8, 10, 12, 14, 16, 18	INxx	Analog Inputs. xx = Channel 00 through Channel 15.
96	DATA IN	Serial Data Input, TTL Compatible.
97	CLK	Clock, TTL Compatible. Falling edge triggered.
98	DATA OUT	Serial Data Out, TTL Compatible.
95	$\overline{\text{UPDATE}}$	Enable (Transparent) Low. Allows serial register to connect directly to switch matrix. Data latched when high.
100	$\overline{\text{RESET}}$	Disable Outputs, Active Low.
99	$\overline{\text{CE}}$	Chip Enable, Enable Low. Must be low to clock in and latch data.
94	$\overline{\text{SER}}$/PAR	Selects Serial Data Mode, Low or Parallel Data Mode, High. Must be connected.
53, 51, 49, 47, 45, 43, 41, 39, 37, 35, 33, 31, 29, 27, 25, 23	OUTyy	Analog Outputs. yy = Channel 00 through Channel 15.
3, 5, 7, 9, 11, 13, 15, 17, 19, 57, 59, 61, 63, 65, 67, 69, 71, 73	AGND	Analog Ground for Inputs and Switch Matrix. Must be connected.
1, 75	DVCC	+5 V for Digital Circuitry.
2, 74	DGND	Ground for Digital Circuitry.
20, 56	AVEE	−5 V for Inputs and Switch Matrix.
21, 55	AVCC	+5 V for Inputs and Switch Matrix.
54, 50, 46, 42, 38, 34, 30, 26, 22	AVCCxx/yy	+5 V for Output Amplifier that is Shared by Channels xx and yy. Must be connected.
52, 48, 44, 40, 36, 32, 28, 24	AVEExx/yy	−5 V for Output Amplifier that is Shared by Channels xx and yy. Must be connected.
84	A0	Parallel Data Input, TTL Compatible (output select LSB).
83	A1	Parallel Data Input, TTL Compatible (output select).
82	A2	Parallel Data Input, TTL Compatible (output select).

Pin No.	Mnemonic	Description
81	A3	Parallel Data Input, TTL Compatible (output select MSB).
80	D0	Parallel Data Input, TTL Compatible (input select LSB)
79	D1	Parallel Data Input, TTL Compatible (input select).
78	D2	Parallel Data Input, TTL Compatible (input select).
77	D3	Parallel Data Input, TTL Compatible (input select MSB).
76	D4	Parallel Data Input, TTL Compatible (output enable).
85 to 93	NC	No Connect.

TYPICAL PERFORMANCE CHARACTERISTICS

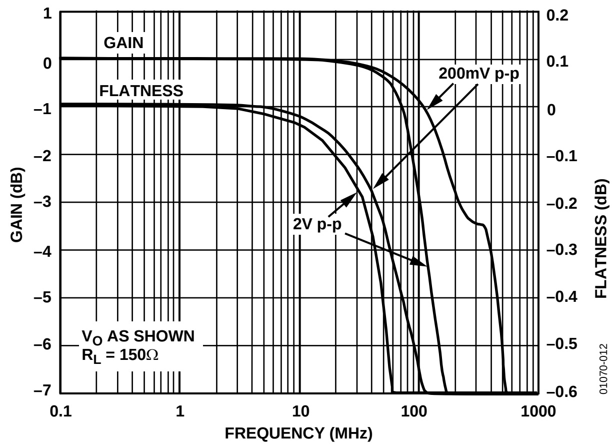


Figure 7. AD8114 Frequency Response, R_L = 150 Ω

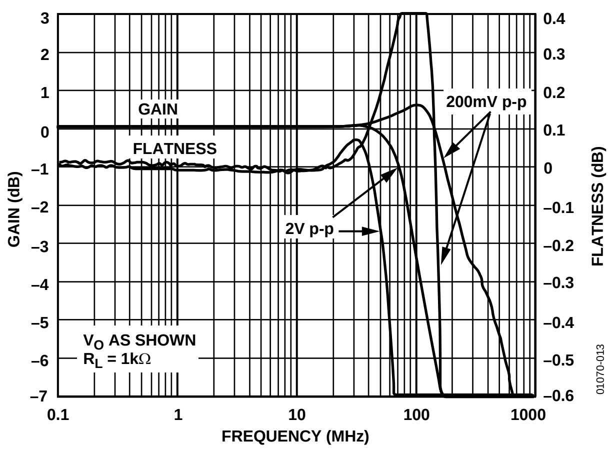


Figure 8. AD8114 Frequency Response, R_L = 1 kΩ

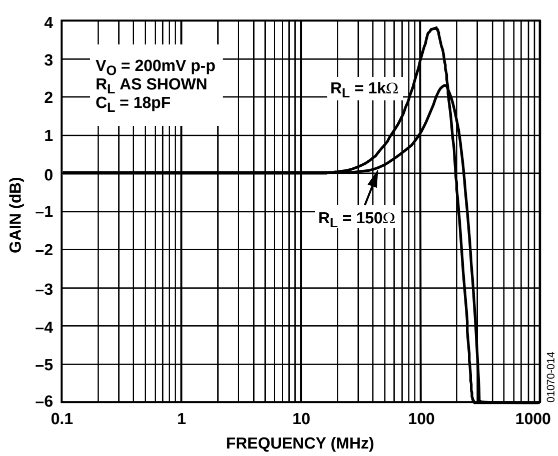


Figure 9. AD8114 Frequency Response vs. Load Impedance

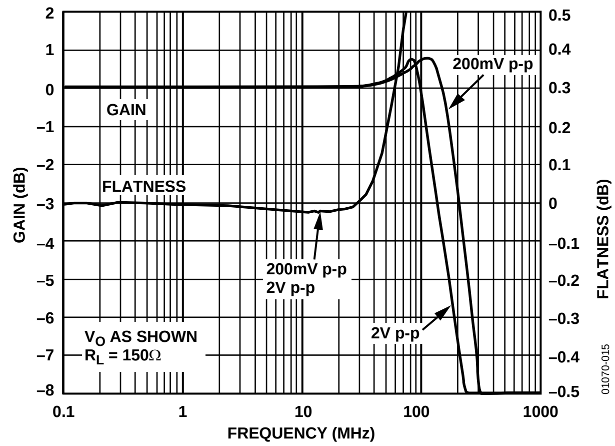


Figure 10. AD8115 Frequency Response, R_L = 150 Ω

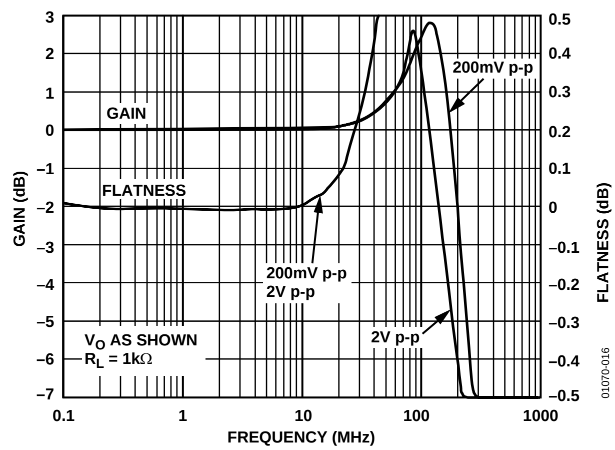


Figure 11. AD8115 Frequency Response, R_L = 1 kΩ

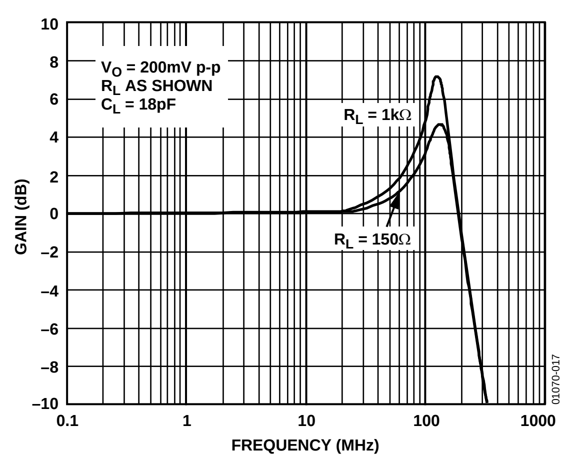


Figure 12. AD8115 Frequency Response vs. Load Impedance

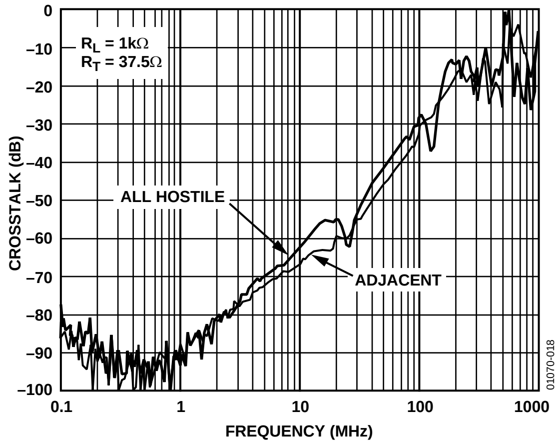


Figure 13. AD8114 Crosstalk vs. Frequency

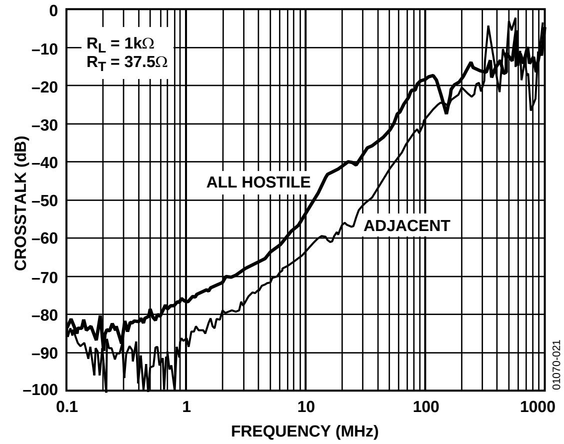


Figure 16. AD8115 Crosstalk vs. Frequency

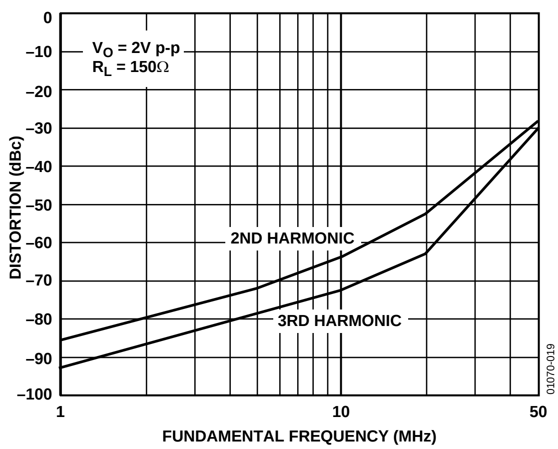


Figure 14. AD8114 Distortion vs. Frequency

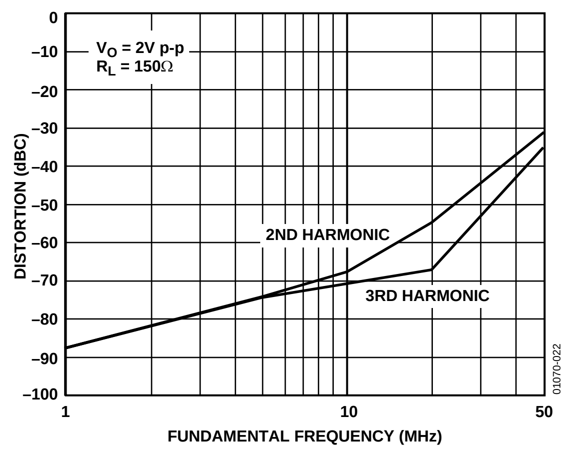


Figure 17. AD8115 Distortion vs. Frequency

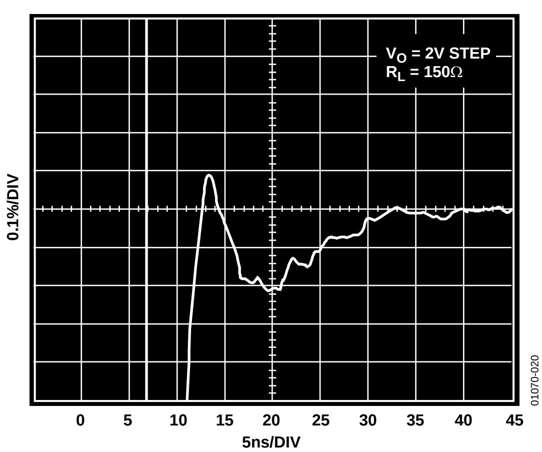


Figure 15. AD8114 Settling Time

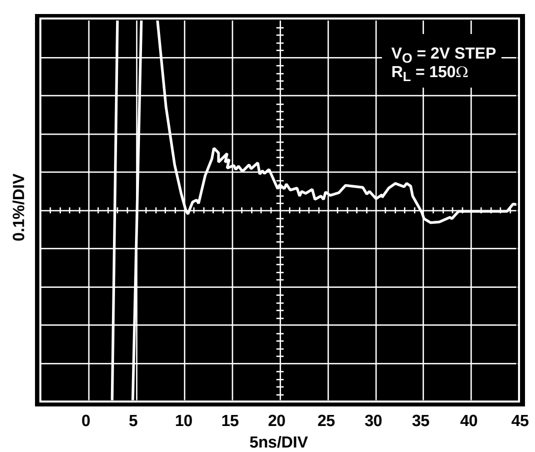


Figure 18. AD8115 Settling Time

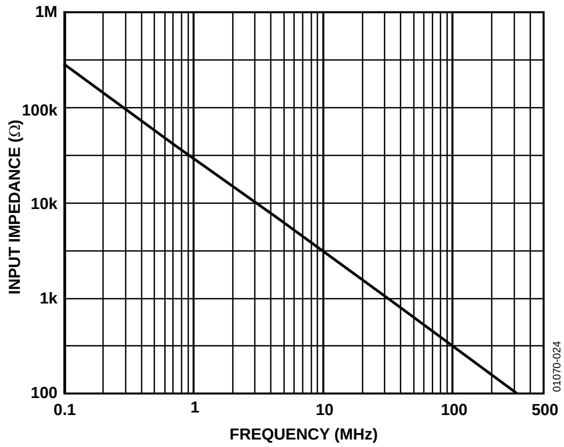


Figure 19. AD8114 Input Impedance vs. Frequency

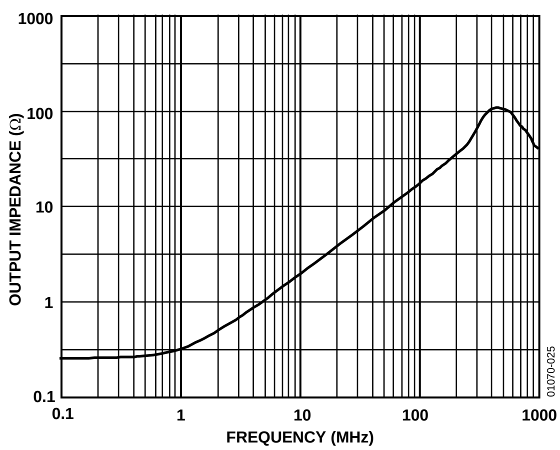


Figure 20. AD8114 Output Impedance, Enabled vs. Frequency

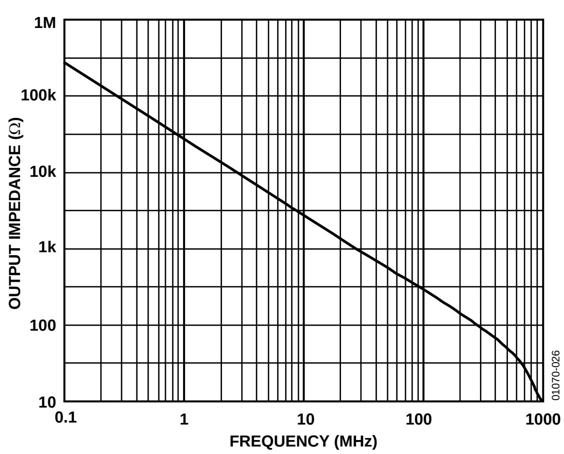


Figure 21. AD8114 Output Impedance, Disabled vs. Frequency

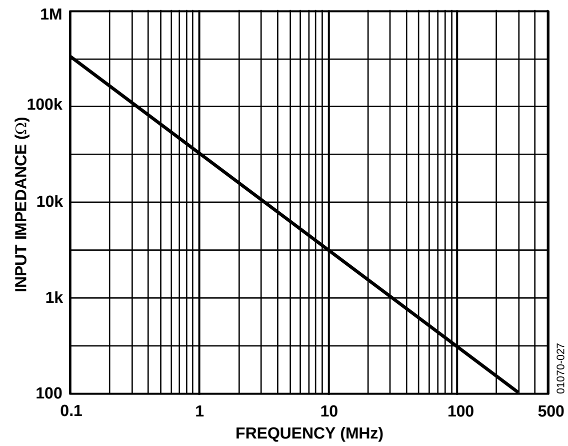


Figure 22. AD8115 Input Impedance vs. Frequency

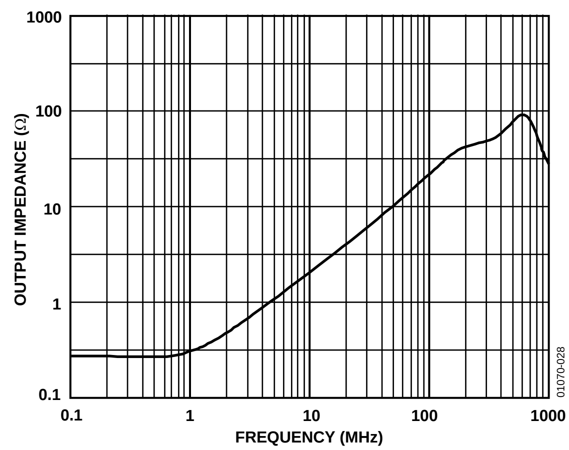


Figure 23. AD8115 Output Impedance, Enabled vs. Frequency

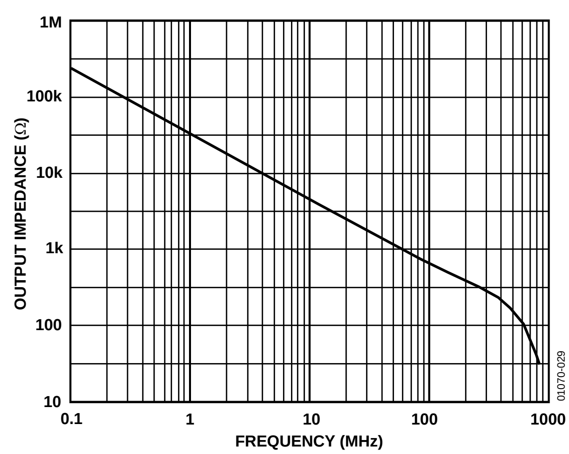


Figure 24. AD8115 Output Impedance, Disabled vs. Frequency

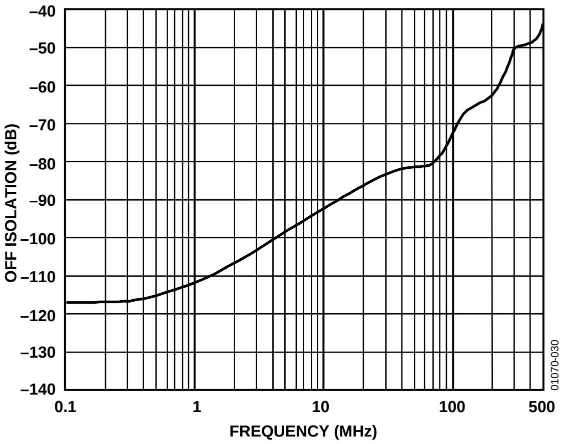


Figure 25. AD8114 Off Isolation, Input-to-Output

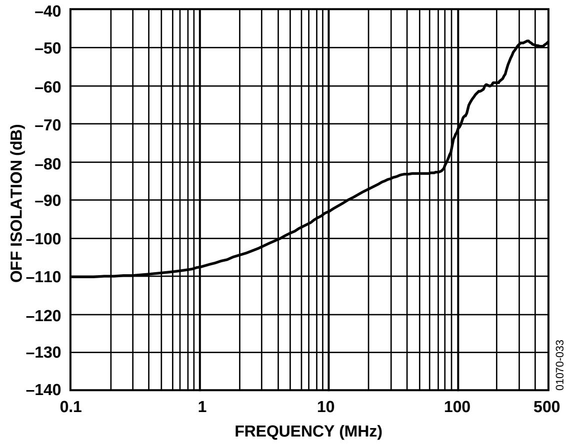


Figure 28. AD8115 Off Isolation, Input-to-Output

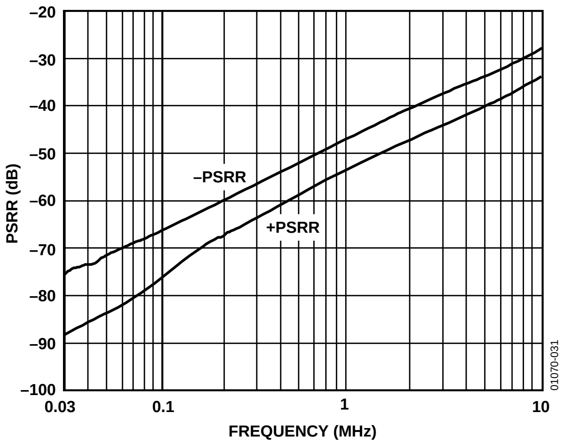


Figure 26. AD8114 PSRR vs. Frequency

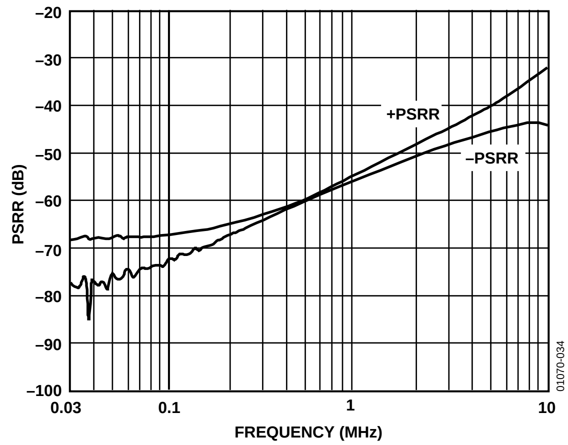


Figure 29. AD8115 PSRR vs. Frequency

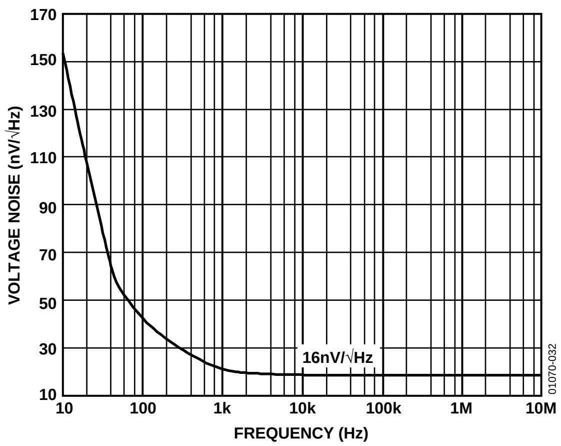


Figure 27. AD8114 Voltage Noise vs. Frequency

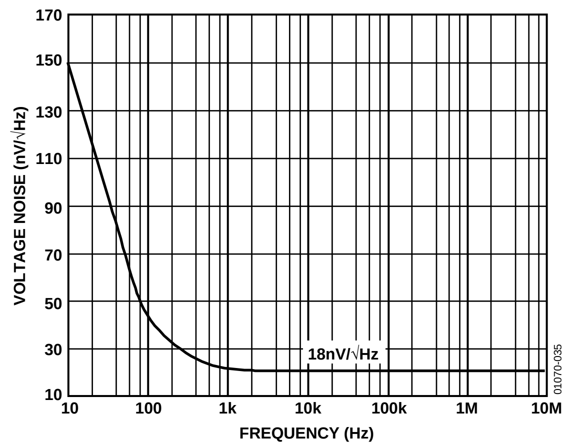


Figure 30. AD8115 Voltage Noise vs. Frequency

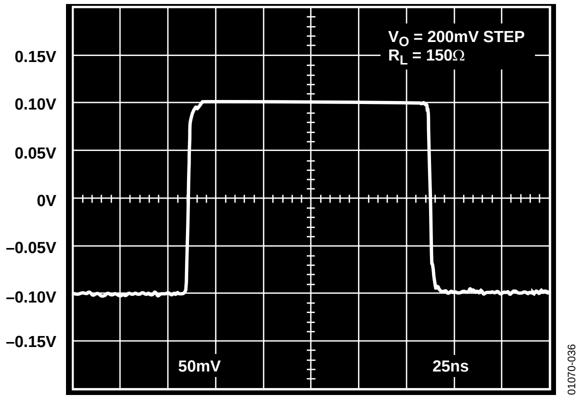


Figure 31. AD8114 Pulse Response, Small Signal

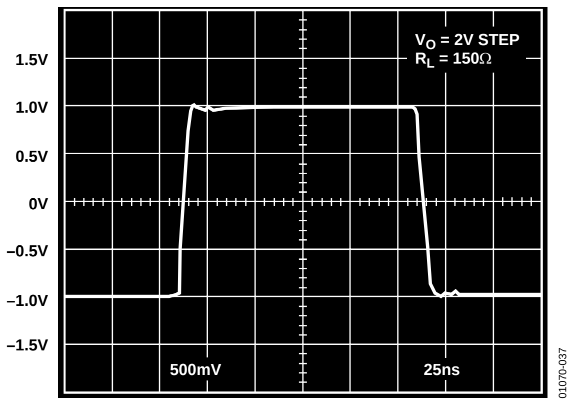


Figure 32. AD8114 Pulse Response, Large Signal

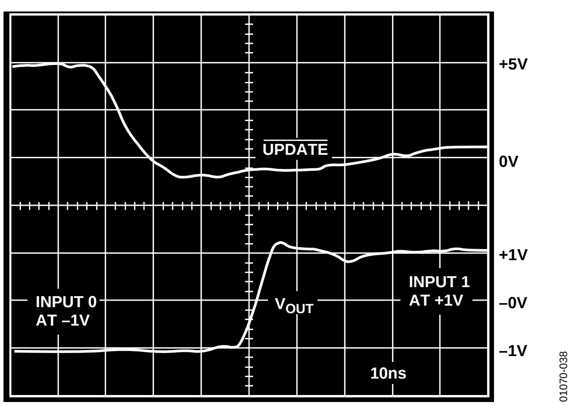


Figure 33. AD8114 Switching Time

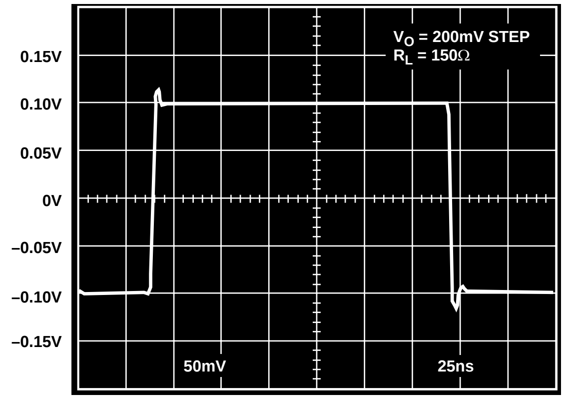


Figure 34. AD8115 Pulse Response, Small Signal

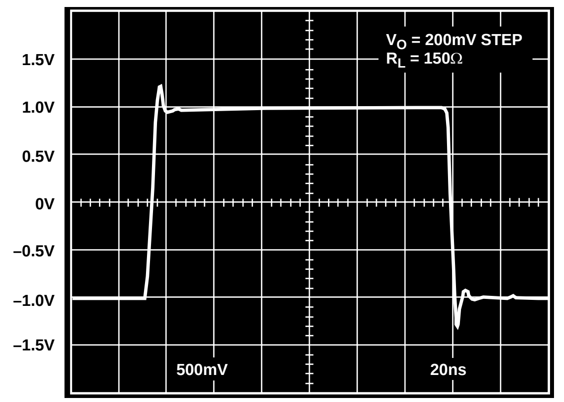


Figure 35. AD8115 Pulse Response, Large Signal

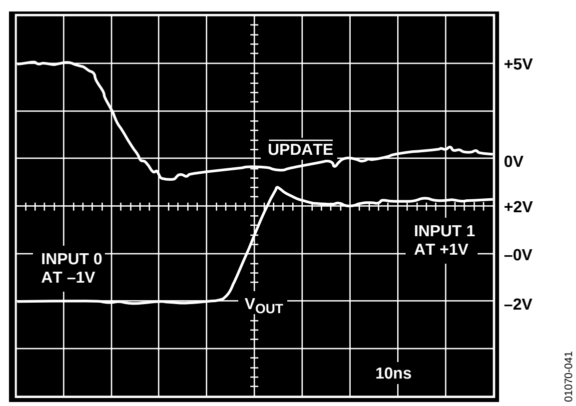


Figure 36. AD8115 Switching Time

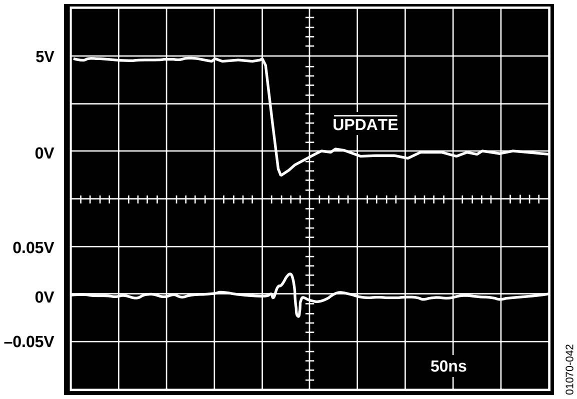


Figure 37. AD8114 Switching Transient (Glitch)

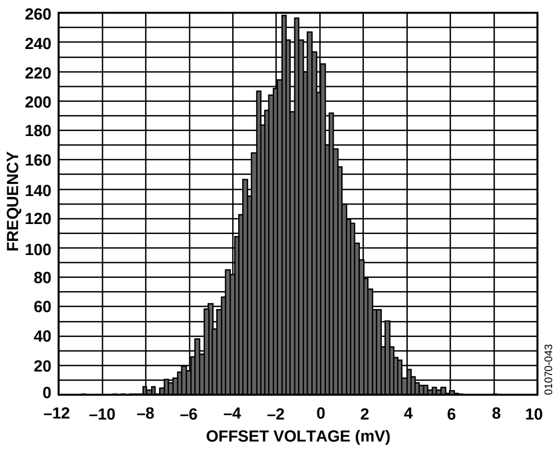


Figure 38. AD8114 Offset Voltage Distribution

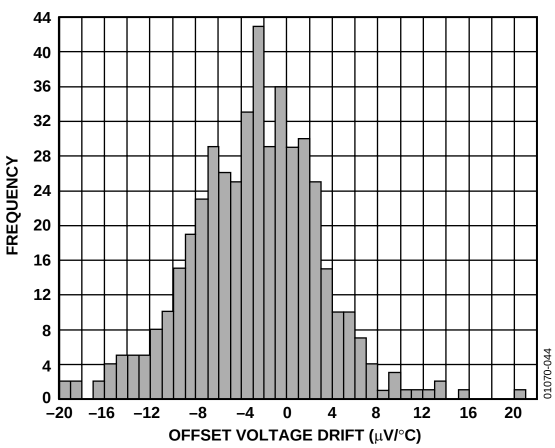


Figure 39. AD8114 Offset Voltage Drift Distribution (–40°C to +85°C)

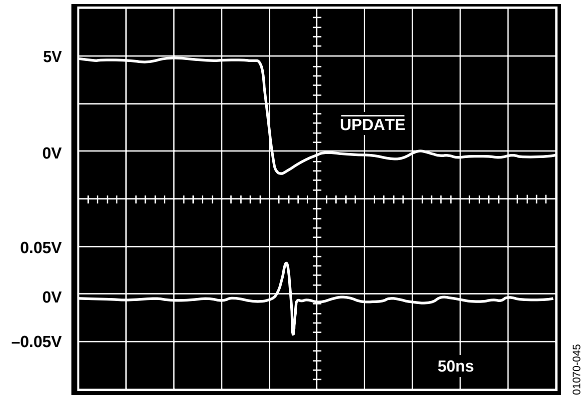


Figure 40. AD8115 Switching Transient (Glitch)

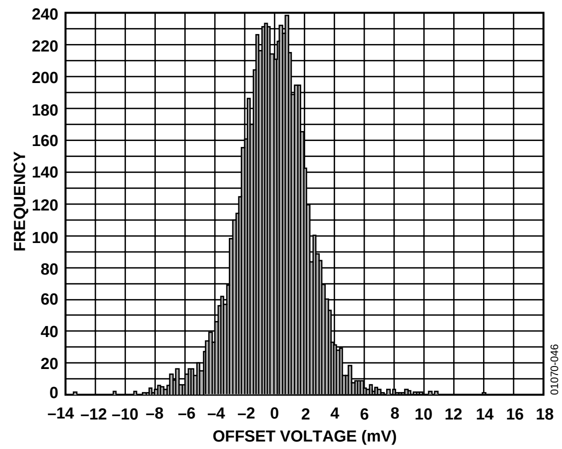


Figure 41. AD8115 Offset Voltage Distribution

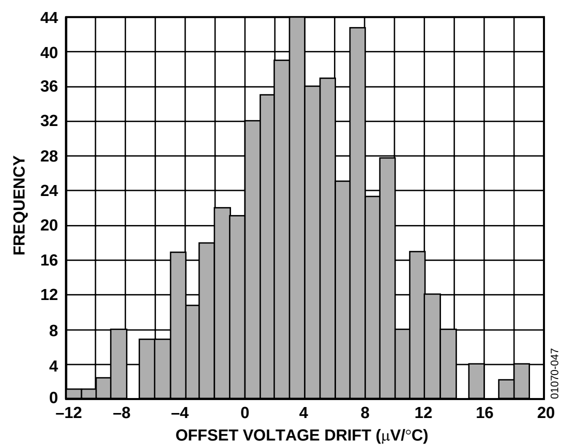


Figure 42. AD8115 Offset Voltage Drift Distribution (–40°C to +85°C)

INPUT/OUTPUT SCHEMATICS

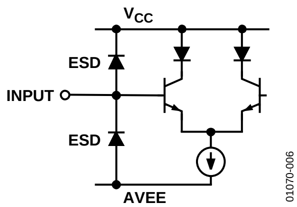


Figure 43. Analog Input

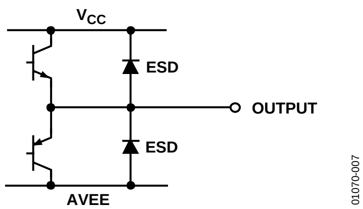


Figure 44. Analog Output

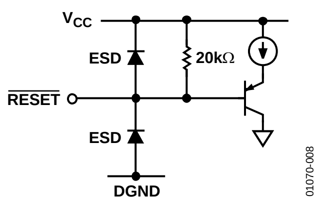


Figure 45. Reset Input

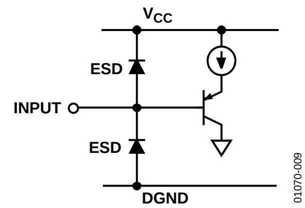


Figure 46. Logic Input

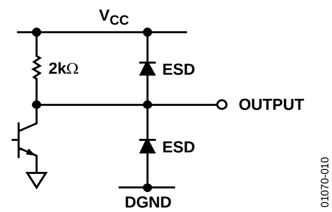


Figure 47. Logic Output

THEORY OF OPERATION

The AD8114 (G = 1) and AD8115 (G = 2) are crosspoint arrays with 16 outputs, each of which can be connected to any one of 16 inputs. Organized by output row, 16 switchable transconductance stages are connected to each output buffer in the form of a 16-to-1 multiplexer. Each of the 16 rows of transconductance stages are wired in parallel to the 16 input pins, for a total array of 256 transconductance stages. Decoding logic for each output selects one (or none) of the transconductance stages to drive the output stage. The transconductance stages are NPN-input differential pairs, sourcing current into the folded cascode output stage. The compensation network and emitter follower output buffer are in the output stage. Voltage feedback sets the gain, with the AD8114 configured as a unity gain follower, and the AD8115 configured as a gain-of-2 amplifier with a feedback network.

This architecture provides drive for a reverse-terminated video load (150 Ω), with low differential gain and phase error for relatively low power consumption. Power consumption is further reduced by disabling outputs and transconductance stages that are not in use. The user notices a small increase in input bias current as each transconductance stage is enabled.

Features of the AD8114 and AD8115 simplify the construction of larger switch matrices. The unused outputs of both devices can be disabled to a high impedance state, allowing the outputs of multiple ICs to be bused together. In the case of the AD8115, a feedback isolation scheme is used so that the impedance of the gain-of-2 feedback network does not load the output. Because no additional input buffering is necessary, high input resistance and low input capacitance are easily achieved without additional signal degradation. To control enable glitches, it is recommended that the disabled output voltage be maintained within its normal enabled voltage range (±3.3 V). If necessary, the disabled output can be kept from drifting out of range by applying an output load resistor to ground.

A flexible TTL-compatible logic interface simplifies the programming of the matrix. Both parallel and serial loading into a first rank of latches programs each output. A global latch simultaneously updates all outputs. A power-on reset pin is available to avoid bus conflicts by disabling all outputs.

APPLICATIONS

The AD8114/AD8115 have two options for changing the programming of the crosspoint matrix. In the first option a serial word of 80 bits can be provided that updates the entire matrix each time. The second option allows for changing the programming of a single output via a parallel interface. The serial option requires fewer signals, but more time (clock cycles) for changing the programming, while the parallel programming technique requires more signals, but can change a single output at a time and requires fewer clock cycles to complete programming.

Serial Programming

The serial programming mode uses the $\overline{\text{CE}}$, CLK, DATA IN, $\overline{\text{UPDATE}}$, and $\overline{\text{SER}}$/PAR device pins. The first step is to assert a low on $\overline{\text{SER}}$/PAR to enable the serial programming mode. $\overline{\text{CE}}$ for the chip must be low to allow data to be clocked into the device. The $\overline{\text{CE}}$ signal can be used to address an individual device when devices are connected in parallel.

The $\overline{\text{UPDATE}}$ signal should be high during the time that data is shifted into the serial port of the device. Although the data still shifts in when $\overline{\text{UPDATE}}$ is low, the transparent, asynchronous latches allow the shifting data to reach the matrix. This causes the matrix to try to update to every intermediate state as defined by the shifting data.

The data at DATA IN is clocked in at every down edge of CLK. A total of 80 bits must be shifted in to complete the programming. For each of the 16 outputs, there are four bits (D0 to D3) that determine the source of its input followed by one bit (D4) that determines the enabled state of the output. If D4 is low (output disabled), the four associated bits (D0 to D3) do not matter because no input is switched to that output.

The most significant output address data is shifted in first, and then following in sequence until the least significant output address data is shifted in. At this point $\overline{\text{UPDATE}}$ can be taken low, which causes the programming of the device according to the data that was just shifted in. The $\overline{\text{UPDATE}}$ registers are asynchronous, and when $\overline{\text{UPDATE}}$ is low (and $\overline{\text{CE}}$ is low), they are transparent.

If more than one AD8114/AD8115 device is to be serially programmed in a system, the DATA OUT signal from one device can be connected to the DATA IN of the next device to form a serial chain. All of the CLK, $\overline{\text{CE}}$, $\overline{\text{UPDATE}}$, and $\overline{\text{SER}}$/PAR pins should be connected in parallel and operated as described above. The serial data is input to the DATA IN pin of the first device of the chain, and it ripples on through to the last. Therefore, the data for the last device in the chain should come at the beginning of the programming sequence. The length of the programming sequence (80 bits) is multiplied by the number of devices in the chain.

Parallel Programming

While using the parallel programming mode, it is not necessary to reprogram the entire device when making changes to the matrix. In fact, parallel programming allows the modification of a single output at a time. Since this takes only one CLK/$\overline{\text{UPDATE}}$ cycle, significant time savings can be realized by using parallel programming.

One important consideration in using parallel programming is that the $\overline{\text{RESET}}$ signal does not reset all registers in the AD8114/AD8115. When taken low, the $\overline{\text{RESET}}$ signal only sets each output to the disabled state. This is helpful during power-up to ensure that two parallel outputs are not active at the same time.

After initial power-up, the internal registers in the device generally have random data, even though the $\overline{\text{RESET}}$ signal was asserted. If parallel programming is used to program one output, then that output is properly programmed, but the rest of the device has a random program state depending on the internal register content at power-up. Therefore, when using parallel programming, it is essential that all outputs be programmed to a desired state after power-up. This ensures that the programming matrix is always in a known state. From then on, parallel programming can be used to modify a single output or more at a time.

In similar fashion, if both $\overline{\text{CE}}$ and $\overline{\text{UPDATE}}$ are taken low after initial power-up, the random power-up data in the shift register is programmed into the matrix. Therefore, to prevent the crosspoint from being programmed into an unknown state, do not apply low logic levels to both $\overline{\text{CE}}$ and $\overline{\text{UPDATE}}$ after power is initially applied. Programming the full shift register one time to a desired state by either serial or parallel programming after initial power-up eliminates the possibility of programming the matrix to an unknown state.

To change the programming of an output via parallel programming, $\overline{\text{SER}}$/PAR and $\overline{\text{UPDATE}}$ should be taken high and $\overline{\text{CE}}$ should be taken low. The CLK signal should be in the high state. The 4-bit address of the output to be programmed should be put on A0 to A3. The first four data bits (D0 to D3) should contain the information that identifies the input that gets programmed to the output that is addressed. The fourth data bit (D4) determines the enabled state of the output. If D4 is low (output disabled), then the data on D0 to D3 does not matter.

After the desired address and data signals have been established, they can be latched into the shift register by a high to low transition of the CLK signal. The matrix is not programmed, however, until the $\overline{\text{UPDATE}}$ signal is taken low. It is thus possible to latch in new data for several or all of the outputs first via successive negative transitions of CLK while $\overline{\text{UPDATE}}$ is held high, and then have all the new data take effect when UPDATE goes low. This technique should be used when programming the device for the first time after power-up when using parallel programming.

POWER-ON RESET

When powering up the AD8114/AD8115, it is usually desirable to have the outputs come up in the disabled state. When taken low, the $\overline{\text{RESET}}$ pin causes all outputs to be in the disabled state. However, the $\overline{\text{RESET}}$ signal does not reset all registers in the AD8114/AD8115. This is important when operating in the parallel programming mode. Please refer to that section for information about programming internal registers after power-up. Serial programming programs the entire matrix each time, so no special considerations apply.

Since the data in the shift register is random after power-up, it should not be used to program the matrix, or the matrix can enter unknown states. To prevent this, do not apply logic low signals to both $\overline{\text{CE}}$ and $\overline{\text{UPDATE}}$ initially after power-up. The shift register should first be loaded with the desired data, and then $\overline{\text{UPDATE}}$ can be taken low to program the device.

The $\overline{\text{RESET}}$ pin has a 20 kΩ pull-up resistor to DVDD that can be used to create a simple power-up reset circuit. A capacitor from $\overline{\text{RESET}}$ to ground holds $\overline{\text{RESET}}$ low for some time while the rest of the device stabilizes. The low condition causes all the outputs to be disabled. The capacitor then charges through the pull-up resistor to the high state, thus allowing full programming capability of the device.

GAIN SELECTION

The 16 × 16 crosspoints come in two versions, depending on the gain of the analog circuit paths that is desired. The AD8114 device is unity gain and can be used for analog logic switching and other applications where unity gain is desired. The AD8114 can also be used for the input and interior sections of larger crosspoint arrays where termination of output signals is not usually used. The AD8114 outputs have very high impedance when their outputs are disabled.

The AD8115 can be used for devices that are used to drive a terminated cable with its outputs. This device has a built-in gain of 2 that eliminates the need for a gain-of-2 buffer to drive a video line. Its high output disabled impedance minimizes signal degradation when paralleling additional outputs.

CREATING LARGER CROSSPOINT ARRAYS

The AD8114/AD8115 are high density building blocks for creating crosspoint arrays of dimensions larger than 16 × 16. Various features, such as output disable, chip enable, and gain-of-1 and gain-of-2 options, are useful for creating larger arrays. When required for customizing a crosspoint array size, they can be used with the AD8108 and AD8109, a pair of (unity gain and gain-of-2) 8 × 8 video crosspoint switches, or with the AD8110 and AD8111, a pair of (unity gain and gain-of-2) 16 × 8 video crosspoint switches.

The first consideration in constructing a larger crosspoint is to determine the minimum number of devices required. The 16 × 16 architecture of the AD8114/AD8115 contains 256 points, which is a factor of 64 greater than a 4 × 1 crosspoint (or multiplexer). The printed circuit board area, power consumption, and design effort savings are readily apparent when compared to using these smaller devices.

For a nonblocking crosspoint, the number of points required is the product of the number of inputs multiplied by the number of outputs. Nonblocking requires that the programming of a given input to one or more outputs does not restrict the availability of that input to be a source for any other outputs.

Some nonblocking crosspoint architectures require more than this minimum as calculated above. Also, there are blocking architectures that can be constructed with fewer devices than this minimum. These systems have connectivity available on a statistical basis that is determined when designing the overall system.

The basic concept in constructing larger crosspoint arrays is to connect inputs in parallel in a horizontal direction and to wire-OR the outputs together in the vertical direction. The meaning of horizontal and vertical can best be understood by looking at a diagram. Figure 48 illustrates this concept for a 32 × 32 crosspoint array that uses four AD8114 or AD8115 devices.

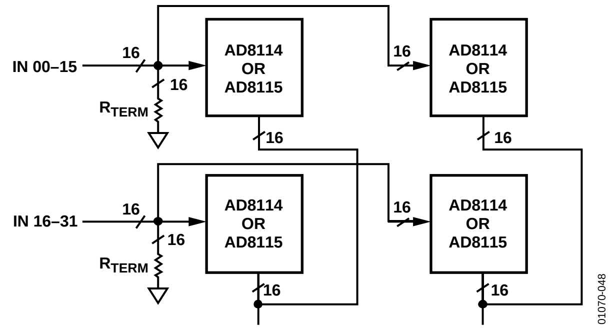


Figure 48. 32 × 32 Crosspoint Array Using Four AD8114 or AD8115 Devices

The inputs are each uniquely assigned to each of the 32 inputs of the two devices and terminated appropriately. The outputs are wired-OR'ed together in pairs. The output from only one of a wire-OR'ed pair should be enabled at any given time. The device programming software must be properly written to cause this to happen.

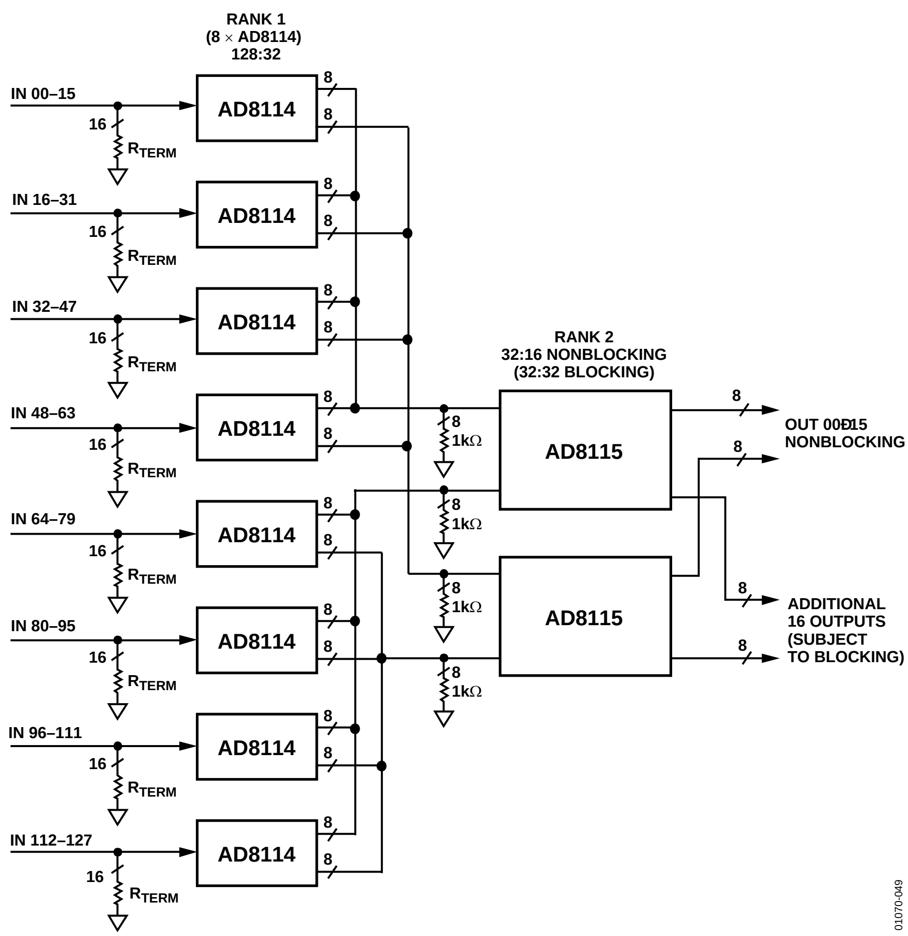


Figure 49. Nonblocking 128 × 16 Array (128 × 32 Blocking)

Using additional crosspoint devices in the design can lower the number of outputs that must be wire-OR'ed together. Figure 49 shows a block diagram of a system using eight AD8114 devices and two AD8115 devices to create a nonblocking, gain-of-2, 128 × 16 crosspoint that restricts the wire-OR'ing at the output to only four outputs.

Additionally, by using the lower eight outputs from each of the two Rank 2 AD8115 devices, a blocking 128 × 32 crosspoint array can be realized. There are, however, some drawbacks to this technique. The offset voltages of the various cascaded devices accumulates, and the bandwidth limitations of the devices compound. In addition, the extra devices consume more current and take up more board space. Once again, the overall system design specifications determine how to make the various tradeoffs.

MULTICHANNEL VIDEO

The excellent video specifications of the AD8114/AD8115 make them ideal candidates for creating composite video crosspoint switches. These can be made quite dense by taking advantage of the high level of integration of the AD8114/AD8115 and the fact that composite video requires only one crosspoint channel per system video channel. There are, however, other video formats that can be routed with the AD8114/AD8115 requiring more than one crosspoint channel per video channel.

Some systems use twisted-pair wiring to carry video signals. These systems utilize differential signals and can lower costs because they use lower cost cables, connectors and termination methods. They also have the ability to lower crosstalk and reject common-mode signals, which can be important for equipment that operates in noisy environments or where common-mode voltages are present between transmitting and receiving equipment.

In such systems, the video signals are differential; there is a positive and negative (or inverted) version of the signals. These complementary signals are transmitted onto each of the two wires of the twisted pair, yielding a first-order zero common-mode voltage. At the receive end, the signals are differentially received and converted back into a single-ended signal.

When switching these differential signals, two channels are required in the switching element to handle the two differential signals that make up the video channel. Thus, one differential video channel is assigned to a pair of crosspoint channels, both input and output. For a single AD8114/AD8115, eight differential video channels can be assigned to the 16 inputs and 16 outputs. This effectively forms an 8 × 8 differential crosspoint switch.

Programming such a device requires that inputs and outputs be programmed in pairs. This information can be deduced by inspection of the programming format of the AD8114/AD8115 and the requirements of the system.

There are other analog video formats requiring more than one analog circuit per video channel. One 2-circuit format that is commonly being used in systems such as satellite TV, digital cable boxes, and higher quality VCRs is called S-video or Y/C video. This format carries the brightness (luminance or Y) portion of the video signal on one channel and the color (chrominance, chroma, or C) on a second channel.

Since S-video also uses two separate circuits for one video channel, creating a crosspoint system requires assigning one video channel to two crosspoint channels, as in the case of a differential video system. Aside from the nature of the video format, other aspects of these two systems are the same.

There are yet other video formats using three channels to carry the video information. Video cameras produce RGB (red, green, blue) directly from the image sensors. RGB is also the usual format used by computers internally for graphics. RGB can be converted to Y, R-Y, B-Y format, sometimes called YUV format. These 3-circuit video standards are referred to as component analog video.

The component video standards require three crosspoint channels per video channel to handle the switching function. In a fashion similar to the 2-circuit video formats, the inputs and outputs are assigned in groups of three, and the appropriate logic programming is performed to route the video signals.

CROSSTALK

Many systems, such as broadcast video, that handle numerous analog signal channels have strict requirements for keeping the various signals from influencing any of the others in the system. Crosstalk is the term used to describe the coupling of the signals of other nearby channels to a given channel.

When there are many signals in close proximity in a system, as is undoubtedly the case in a system that uses the AD8114/AD8115, the crosstalk issues can be quite complex. A good understanding of the nature of crosstalk and some definition of terms is required to specify a system that uses one or more AD8114/AD8115 devices.

Types of Crosstalk

Crosstalk can be propagated by means of any of three methods. These fall into the categories of electric field, magnetic field, and sharing of common impedances. This section explains these effects.

Every conductor can be both a radiator of electric fields and a receiver of electric fields. The electric field crosstalk mechanism occurs when the electric field created by the transmitter propagates across a stray capacitance (for example, free space) and couples with the receiver and induces a voltage. This voltage is an unwanted crosstalk signal in any channel that receives it.

Currents flowing in conductors create magnetic fields that circulate around the currents. These magnetic fields then generate voltages in any other conductors whose paths they link. The undesired induced voltages in these other channels are crosstalk signals. The channels that crosstalk can be said to have a mutual inductance that couples signals from one channel to another.

The power supplies, grounds, and other signal return paths of a multichannel system are generally shared by the various channels. When a current from one channel flows in one of these paths, a voltage that is developed across the impedance becomes an input crosstalk signal for other channels that share the common impedance.

All these sources of crosstalk are vector quantities, so the magnitudes cannot simply be added together to obtain the total crosstalk. In fact, there are conditions where driving additional circuits in parallel in a given configuration can actually reduce the crosstalk.

Areas of Crosstalk

For a practical AD8114/AD8115 circuit, it is required that the device be mounted to some sort of circuit board to connect it to the power supplies and the measurement equipment. This requirement, however, raises the issue that the crosstalk of a system is a combination of the intrinsic crosstalk of the devices in addition to the circuit board to which they are mounted. It is important to try to separate these two areas of crosstalk when attempting to minimize its effect.

In addition, crosstalk can occur among the inputs to a crosspoint and among the output. It can also occur from input to output. Techniques are discussed for diagnosing which part of a system is contributing to crosstalk.

Measuring Crosstalk

Crosstalk is measured by applying a signal to one or more channels and measuring the relative strength of that signal on a desired selected channel. The measurement is usually expressed as dB down from the magnitude of the test signal. The crosstalk is expressed by

$$|XT| = 20 \log_{10} \left(Asel(s)/Atest(s) \right)$$

where:
$s = j\omega$ is the Laplace transform variable.
Asel(s) is the amplitude of the crosstalk-induced signal in the selected channel.
Atest(s) is the amplitude of the test signal.

It can be seen that crosstalk is a function of frequency, but not a function of the magnitude of the test signal (to first order). In addition, the crosstalk signal has a phase relative to the test signal associated with it.

A network analyzer is most commonly used to measure crosstalk over a frequency range of interest. It can provide both magnitude and phase information about the crosstalk signal.

As a crosspoint system or device grows larger, the number of theoretical crosstalk combinations and permutations can become extremely large. For example, in the case of the 16 × 16 matrix of the AD8114/AD8115, we can examine the number of crosstalk terms that can be considered for a single channel, say IN00 input. IN00 is programmed to connect to one of the AD8114/AD8115 outputs where the measurement can be made.

First, we can measure the crosstalk terms associated with driving a test signal into each of the other 15 inputs one at a time while applying no signal to IN00. We can then measure the crosstalk terms associated with driving a parallel test signal into all 15 other inputs taken two at a time in all possible combinations, then three at a time, and so on, until there is only one way to drive a test signal into all 15 other inputs in parallel.

Each of these cases is legitimately different from the others and might yield a unique value depending on the resolution of the measurement system, but it is hardly practical to measure all these terms and then to specify them. In addition, this describes the crosstalk matrix for just one input channel. A similar crosstalk matrix can be proposed for every other input. In addition, if the possible combinations and permutations for connecting inputs to the other (not used for measurement) outputs are taken into consideration, the numbers rather quickly grow to astronomical proportions. If a larger crosspoint array of multiple AD8114/AD8115 devices is constructed, the numbers grow larger still.

Some subset of all these cases must be selected to be used as a guide for a practical measure of crosstalk. One common method is to measure all hostile crosstalk. This term means that the crosstalk to the selected channel is measured while all other system channels are driven in parallel. In general, this yields the worst crosstalk number, but this is not always the case due to the vector nature of the crosstalk signal.

Other useful crosstalk measurements are those created by one nearest neighbor or by the two nearest neighbors on either side. These crosstalk measurements are generally higher than those of more distant channels, so they can serve as a worst-case measure for any other 1-channel or 2-channel crosstalk measurements.

Input and Output Crosstalk

The flexible programming capability of the AD8114/AD8115 can be used to diagnose whether crosstalk is occurring more on the input side or the output side. Some examples are illustrative. A given input channel (IN07 in the middle for this example) can be programmed to drive OUT07 (also in the middle). The input to IN07 is just terminated to ground (via 50 Ω or 75 Ω) and no signal is applied.

All the other inputs are driven in parallel with the same test signal (practically that is provided by a distribution amplifier), with all other outputs except OUT07 disabled. Since grounded IN07 is programmed to drive OUT07, no signal should be present. Any signal that is present can be attributed to the other 15 hostile input signals because no other outputs are driven. (They are all disabled.) Thus, this method measures the all-hostile input contribution to crosstalk into IN07. Of course, the method can be used for other input channels and combinations of hostile inputs.

For output crosstalk measurement, a single input channel is driven (IN00, for example) and all outputs other than a given output (IN07 in the middle) are programmed to connect to IN00. OUT07 is programmed to connect to IN15 (far away from IN00), which is terminated to ground.

Thus OUT07 should not have a signal present since it is listening to a quiet input. Any signal measured at the OUT07 can be attributed to the output crosstalk of the other 16 hostile outputs. Again, this method can be modified to measure other channels and other crosspoint matrix combinations.

Effect of Impedances on Crosstalk

The input side crosstalk can be influenced by the output impedance of the sources that drive the inputs. The lower the impedance of the drive source, the lower the magnitude of the crosstalk. The dominant crosstalk mechanism on the input side is capacitive coupling. The high impedance inputs do not have significant current flow to create magnetically induced crosstalk. However, significant current can flow through the input termination resistors and the loops that drive them. Thus, the printed circuit board on the input side can contribute to magnetically coupled crosstalk.

From a circuit standpoint, the input crosstalk mechanism looks like a capacitor coupling to a resistive load. For low frequencies, the magnitude of the crosstalk is given by

$$|XT| = 20\log_{10}\left((R_S\ C_M)\times s\right)$$

where:
R_S is the source resistance.
C_M is the mutual capacitance between the test signal circuit and the selected circuit.
s is the Laplace transform variable.

From the equation, it can be observed that this crosstalk mechanism has a high-pass nature; it can be minimized by reducing the coupling capacitance of the input circuits and lowering the output impedance of the drivers. If the input is driven from a 75 Ω terminated cable, the input crosstalk can be reduced by buffering this signal with a low output impedance buffer.

On the output side, the crosstalk can be reduced by driving a lighter load. Although the AD8114/AD8115 is specified with excellent differential gain and phase when driving a standard 150 Ω video load, the crosstalk is higher than the minimum obtainable due to the high output currents. These currents induce crosstalk via the mutual inductance of the output pins and bond wires of the AD8114/AD8115.

From a circuit standpoint, this output crosstalk mechanism looks like a transformer, with a mutual inductance between the windings, that drives a load resistor. For low frequencies, the magnitude of the crosstalk is given by

$$|XT| = 20\log_{10}(Mxy \times s / R_L)$$

where:
Mxy is the mutual inductance of Output X to Output Y.
R_L is the load resistance on the measured output.

This crosstalk mechanism can be minimized by keeping the mutual inductance low and increasing R_L. The mutual inductance can be kept low by increasing the spacing of the conductors and minimizing their parallel length.

OUTLINE DIMENSIONS

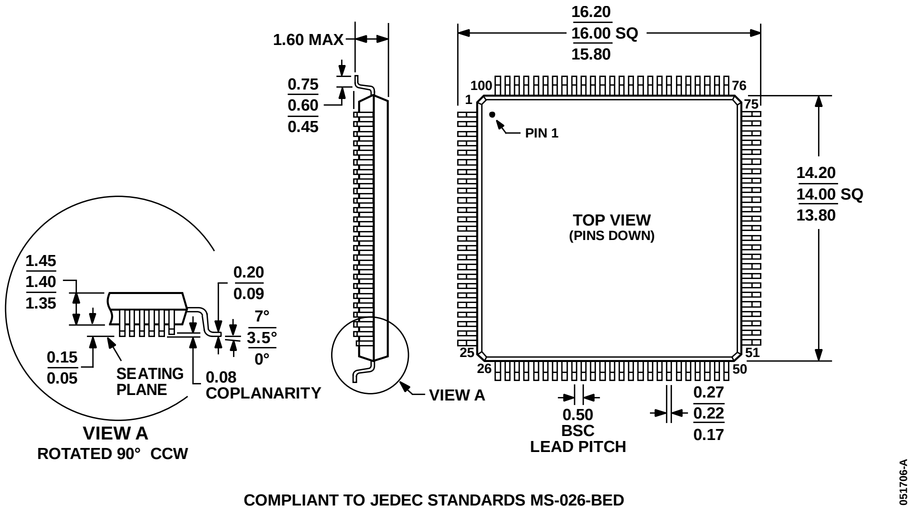


Figure 50. 100-Lead Low Profile Quad Flat Package [LQFP]
(ST-100-1)
Dimension shown in millimeters

ORDERING GUIDE

Model[1, 2]	Temperature Range	Package Description	Package Option
AD8114ASTZ	−40°C to +85°C	100-Lead Low Profile Quad Flat Package [LQFP]	ST-100-1
AD8115ASTZ	−40°C to +85°C	100-Lead Low Profile Quad Flat Package [LQFP]	ST-100-1

[1] Details of the lead finish composition can be found on the Analog Devices website at www.analog.com by reviewing the Material Description of each relevant package.
[2] Z = RoHS Compliant Part.

NOTES