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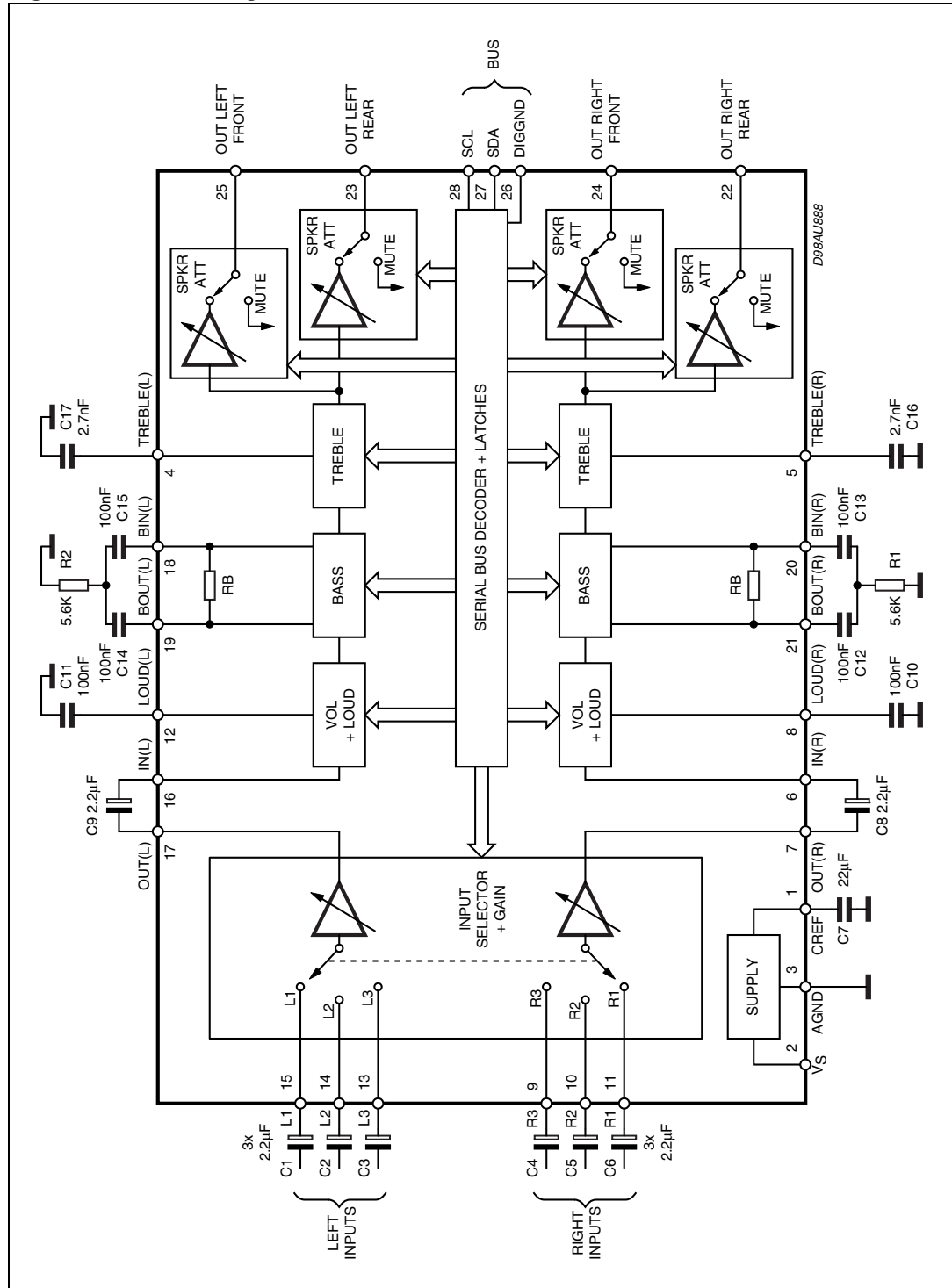
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# 1 Block, test and pin diagrams

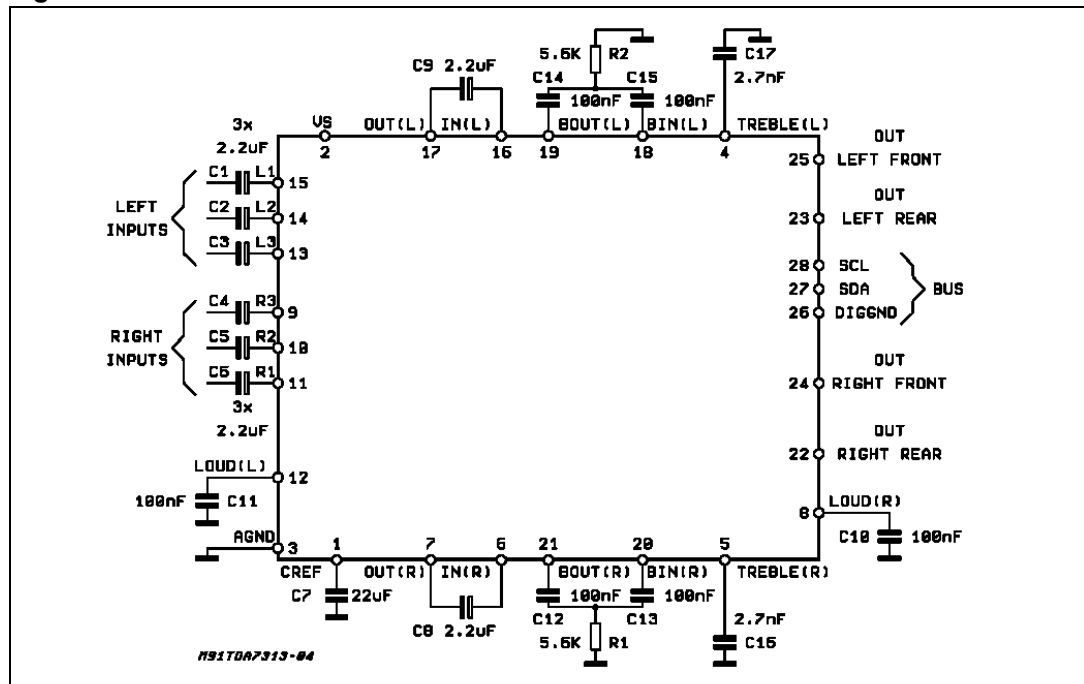
## 1.1 Block diagram

Figure 1. Block diagram



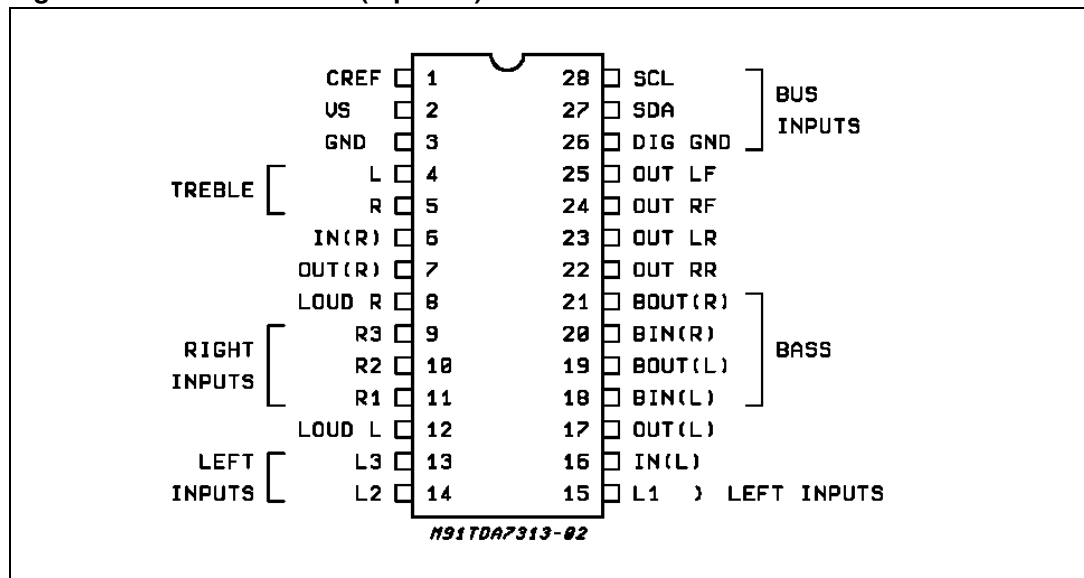
## 1.2 Test circuit

Figure 2. Test circuit



## 1.3 Pin connection

Figure 3. Pin connection (top view)



## 2 Electrical specifications

### 2.1 Absolute maximum ratings

Table 2. Absolute maximum ratings

Symbol	Parameter	Value	Unit
$V_S$	Operating supply voltage	10.0	V
$T_{amb}$	Ambient temperature	-40 to 85	°C
$T_{stg}$	Storage temperature range	-55 to +150	°C

### 2.2 Quick reference data

Table 3. Quick reference data

Symbol	Parameter	Min.	Typ.	Max.	Unit
$V_S$	Supply voltage	6	9	10	V
$V_{CL}$	Max. input signal handling	2			Vrms
THD	Total harmonic distortion $V = 1$ Vrms; $f = 1$ kHz		0.01		%
S/N	Signal to noise ratio		106		dB
$S_C$	Channel separation $f = 1$ kHz		103		dB
	Volume control 1.25d B step	-78.75		0	dB
	Bass and treble control 2 dB step	-14		+14	dB
	Fader and balance control 1.25 dB step	-38.75		0	dB
	Input gain 3.75 dB step 1.25 dB step	0		11.25	dB
	Mute attenuation		100		dB

### 2.3 Thermal data

Table 4. Thermal data

Symbol	Parameter	Value	Unit
$R_{th\ j-pins}$	Thermal resistance junction to pins	Max. 85	°C/W

## 2.4 Electrical characteristics

**Table 5. Electrical characteristics**

( $T_{amb} = 25\text{ °C}$ ,  $V_S = 9\text{ V}$ ,  $R_L = 10\text{ k}\Omega$ ,  $R_G = 600\ \Omega$ , all control flat ( $G = 0$ ),  $f = 1\text{ kHz}$  unless otherwise specified)

Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit
<b>Supply</b>						
$V_S$	Supply voltage		6	9	10	V
$I_S$	Supply current			8	11	mA
SVR	Ripple rejection		60	80		dB
<b>Input selectors</b>						
$R_{II}$	Input resistance	Input 1, 2, 3, 4		50		k $\Omega$
$V_{CL}$	Clipping level		2	2.5		Vrms
$S_{IN}$	Input separation <sup>(2)</sup>		80	100		dB
$R_L$	Output load resistance	pin 7, 17	2			k $\Omega$
$G_{INmin}$	Min. input gain		-1	0	1	dB
$G_{INmax}$	Max. input gain			11.25		dB
$G_{STEP}$	Step resolution			3.75		dB
$e_{IN}$	Input noise	$G = 11.25\text{ dB}$		2		$\mu\text{V}$
<b>Volume control</b>						
$R_{IN}$	Input resistance			33		k $\Omega$
$C_{RANGE}$	Control range		70	75	80	dB
$A_{VMIN}$	Min. attenuation		-1	0	1	dB
$A_{VMAX}$	Max. attenuation		70	75	80	dB
$A_{STEP}$	Step resolution		0.5	1.25	1.75	dB
$E_A$	Attenuation set error	$A_V = 0\text{ to }-20\text{ dB}$	-1.25	0	1.25	dB
		$A_V = -20\text{ to }-60\text{ dB}$	-3		2	dB
$E_T$	Tracking error				2	dB
<b>Speaker attenuators</b>						
$C_{range}$	Control range		35	37.5	40	dB
$S_{STEP}$	Step resolution		0.5	1.25	1.75	dB
$E_A$	Attenuation set error				1.5	dB
$A_{MUTE}$	Output mute attenuation		80	100		dB
<b>Bass control<sup>(1)</sup></b>						
$G_b$	Control range	Max. Boost/cut	$\pm 12$	$\pm 14$	$\pm 16$	dB
$B_{STEP}$	Step resolution		1	2	3	dB

**Table 5. Electrical characteristics (continued)**

( $T_{amb} = 25\text{ °C}$ ,  $V_S = 9\text{ V}$ ,  $R_L = 10\text{ k}\Omega$ ,  $R_G = 600\ \Omega$ , all control flat ( $G = 0$ ),  $f = 1\text{ kHz}$  unless otherwise specified)

Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit
$R_B$	Internal feedback resistance			44		$\text{k}\Omega$
<b>Treble control (1)</b>						
$G_t$	Control range	Max. Boost/cut	$\pm 13$	$\pm 14$	$\pm 15$	dB
$T_{STEP}$	Step Resolution		1	2	3	dB
<b>Audio outputs</b>						
$V_{OCL}$	Clipping level	$d = 0.3\%$	2	2.5		Vrms
$R_L$	Output load resistance		2			$\text{k}\Omega$
$C_L$	Output load capacitance				10	nF
$R_{OUT}$	Output resistance			75		$\Omega$
$V_{OUT}$	DC voltage level		4.2	4.5	4.8	V
<b>General</b>						
$e_{NO}$	Output noise <sup>(2)</sup>	BW = 20-20 kHz, flat output muted all gains = 0 dB		2.5 5		$\mu\text{V}$ $\mu\text{V}$
		A curve all gains = 0 dB		3		$\mu\text{V}$
S/N	Signal to noise ratio	all gains = 0 dB; $V_O = 1\text{ Vrms}$		106		dB
d	Distortion	$A_V = 0$ ; $V_{IN} = 1\text{ Vrms}$		0.01		%
		$A_V = -20\text{ dB}$ , $V_{IN} = 1\text{ Vrms}$		0.09	0.3	%
		$A_V = -20\text{ dB}$ , $V_{IN} = 0.3\text{ Vrms}$		0.04		%
$Sc$	Channel separation left/right		80	103		dB
	Total tracking error	$A_V = 0\text{ to }-20\text{ dB}$		0	1	dB
		-20 to -60 dB		0	2	dB
<b>Bus inputs</b>						
$V_{IL}$	Input low voltage				1	V
$V_{IH}$	Input high voltage		3			V
$I_{IN}$	Input current		-5		+5	$\mu\text{A}$
$V_O$	Output voltage SDA acknowledge	$I_O = 1.6\text{ mA}$			0.4	V

1. Bass and treble response see attached diagram (Figure 19). The center frequency and quality of the resonance behavior can be chosen by the external circuitry. A standard first order bass response can be realized by a standard feedback network
2. The selected input is grounded through the 2.2  $\mu\text{F}$  capacitor.



## 2.5 Electrical characteristics curves

Figure 4. Loudness vs. volume attenuation

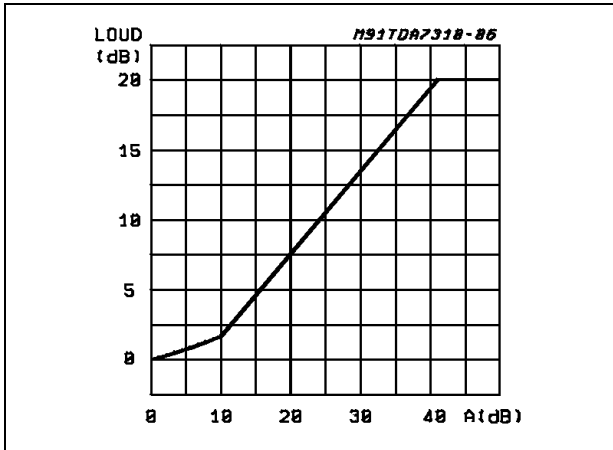


Figure 5. Loudness vs. frequency ( $C_{LOUD} = 100\text{ nF}$ ) vs. volume attenuation

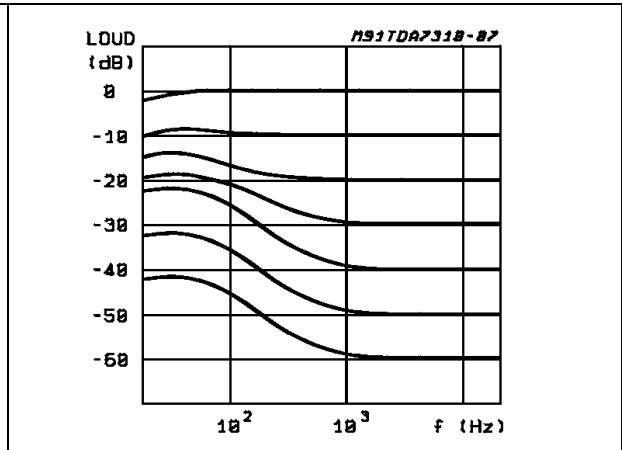


Figure 6. Loudness vs. external capacitors

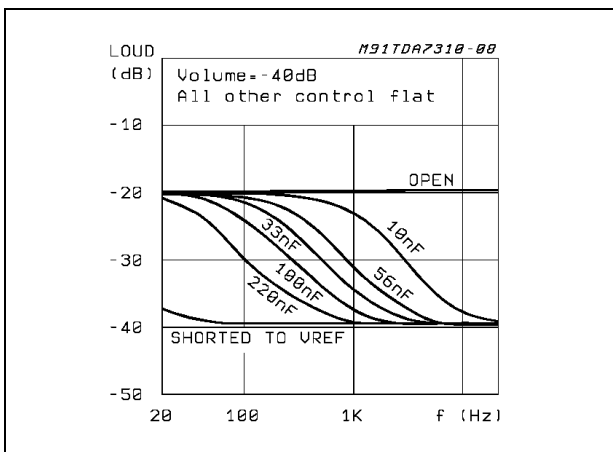


Figure 7. Noise vs. volume/gain setting

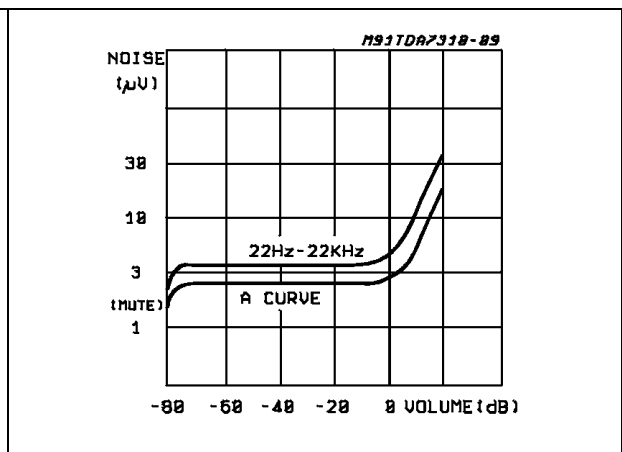


Figure 8. Signal to noise ratio vs. volume setting

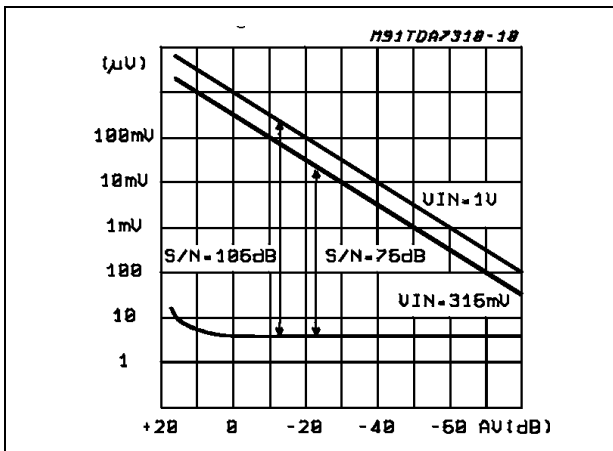


Figure 9. Distortion and noise vs. frequency ( $V_{IN} = 1\text{ V}$ )

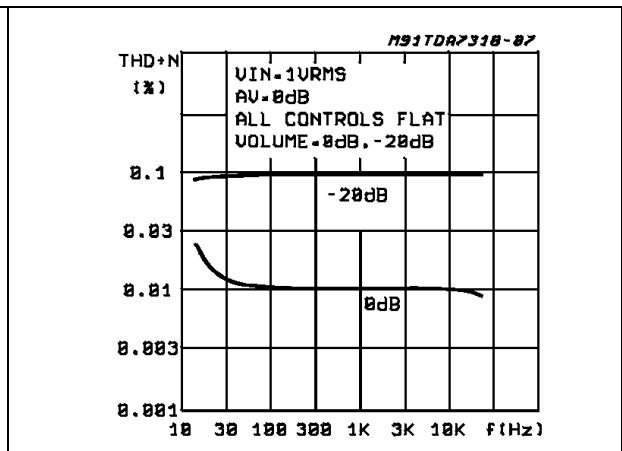


Figure 10. Distortion and noise vs. frequency ( $V_{IN} = 250\text{ mV}$ )

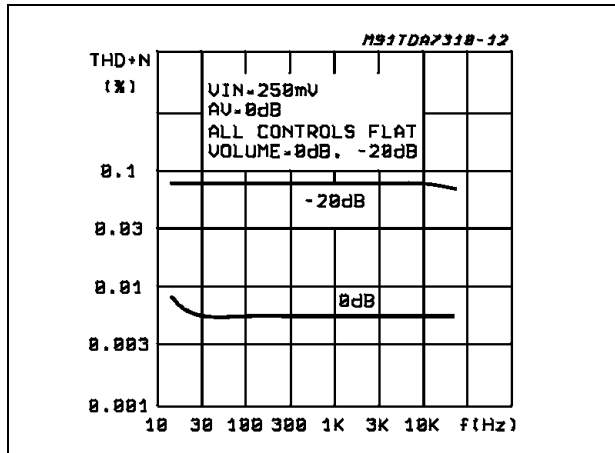


Figure 11. Distortion vs. load resistance

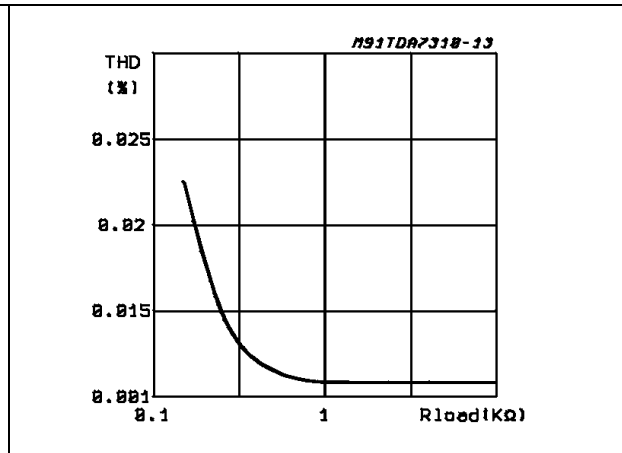


Figure 12. Channel separation (L → R) vs. frequency

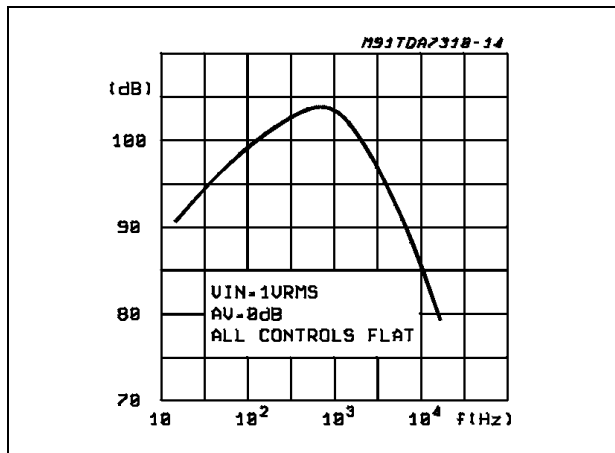


Figure 13. Input separation (L1 → L2, L3) vs. frequency

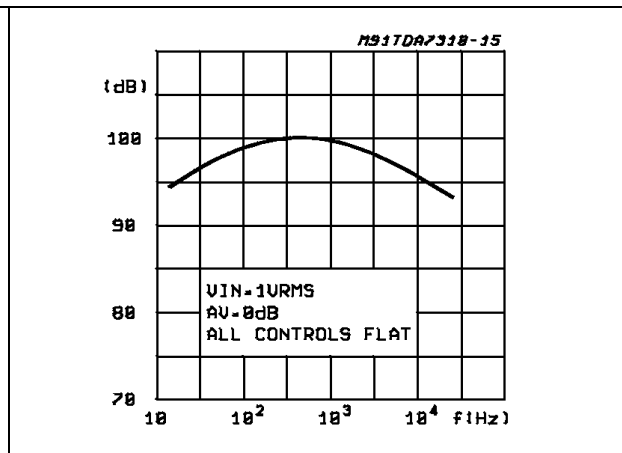


Figure 14. Supply voltage rejection vs. frequency

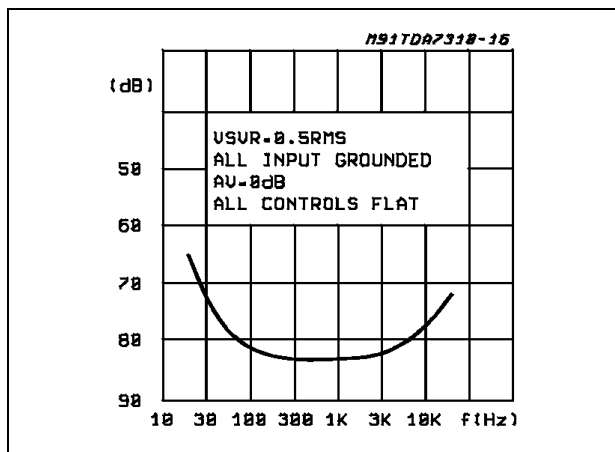


Figure 15. Output clipping level vs. supply voltage

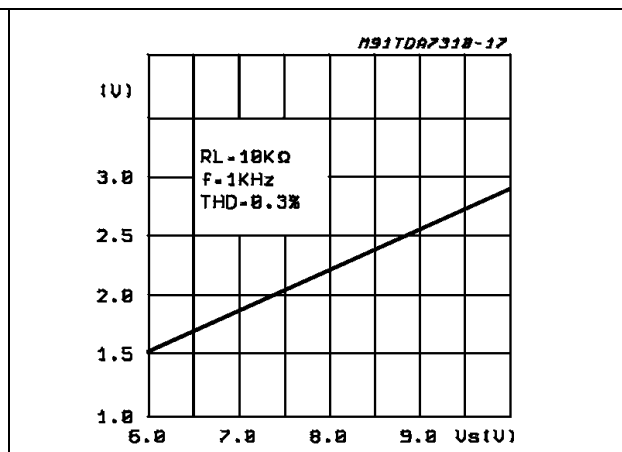


Figure 16. Quiescent current vs. supply voltage

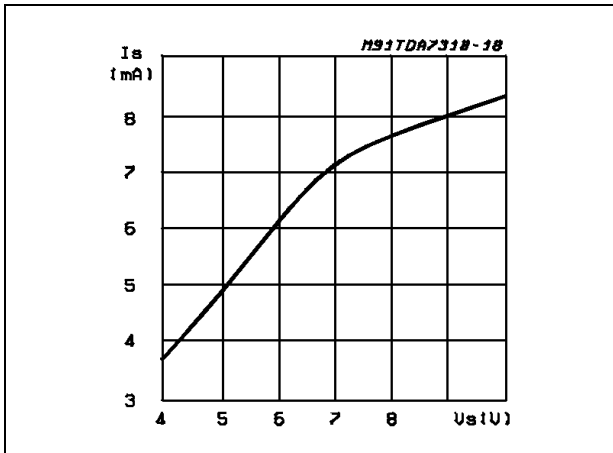


Figure 17. Supply current vs. temperature

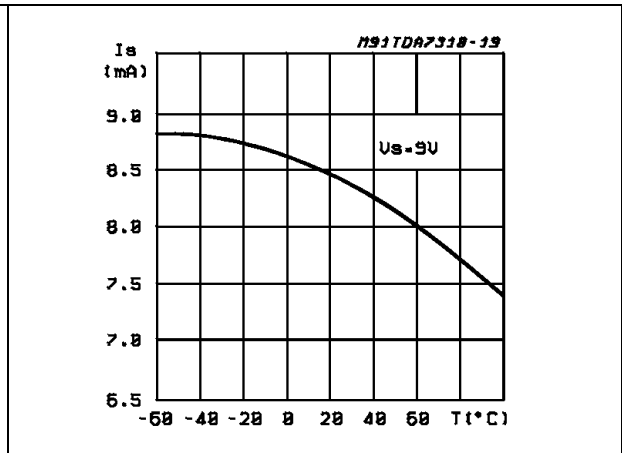


Figure 18. Bass resistance vs. temperature

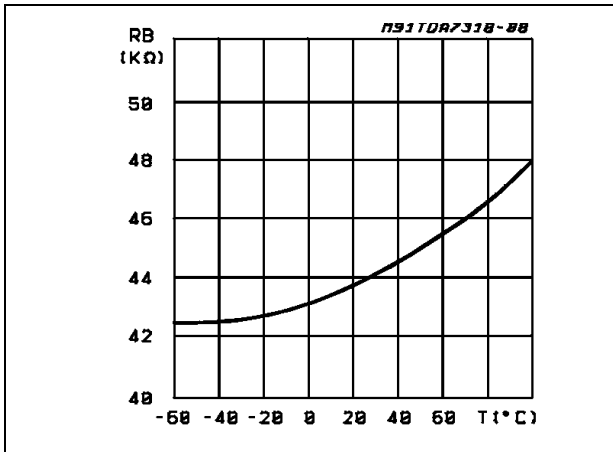
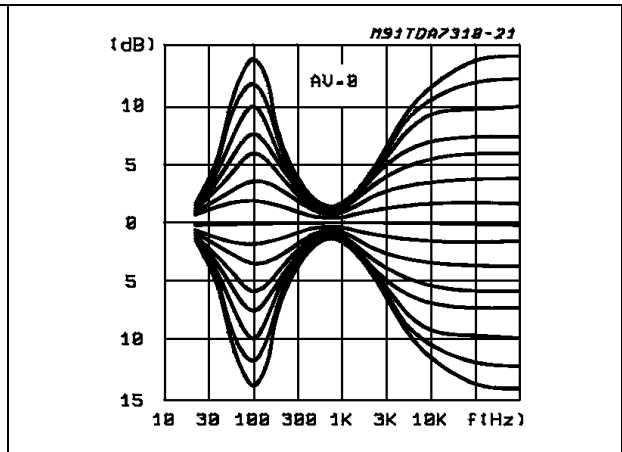


Figure 19. Typical tone response (with the external components indicated in the test circuit)



## 3 I<sup>2</sup>C bus interface

Data transmission from microprocessor to the TDA7303 and viceversa takes place through the 2 wires I<sup>2</sup>C bus interface, consisting of the two lines SDA and SCL (pull-up resistors to positive supply voltage must be connected).

### 3.1 Data validity

As shown in [Figure 20](#), the data on the SDA line must be stable during the high period of the clock. The high and low state of the data line can only change when the clock signal on the SCL line is IOW.

### 3.2 Start and stop conditions

As shown in [Figure 21](#) a start condition is a high to low transition of the SDA line while SCL is high. The stop condition is a low to high transition of the SDA line while SCL is high.

### 3.3 Byte format

Every byte transferred on the SDA line must contain 8 bits. Each byte must be followed by an acknowledge bit. The MSB is transferred first.

### 3.4 Acknowledge

The master ( $\mu$ P) puts a resistive HIGH level on the SDA line during the acknowledge clock pulse (see [Figure 22](#)). The peripheral (audioprocessor) that acknowledges has to pull-down (low) the SDA line during the acknowledge clock pulse, so that the SDA line is stable low during this clock pulse.

The audioprocessor which has been addressed has to generate an acknowledge after the reception of each byte, otherwise the SDA line remains at the high level during the ninth clock pulse time. In this case the master transmitter can generate the stop information in order to abort the transfer.

### 3.5 Transmission without acknowledge

Avoiding to detect the acknowledge of the audioprocessor, the  $\mu$ P can use a simpler transmission: simply it waits one clock without checking the slave acknowledging, and sends the new data.

This approach of course is less protected from misreading and decreases the noise immunity.

Figure 20. Data validity on the I<sup>2</sup>C bus

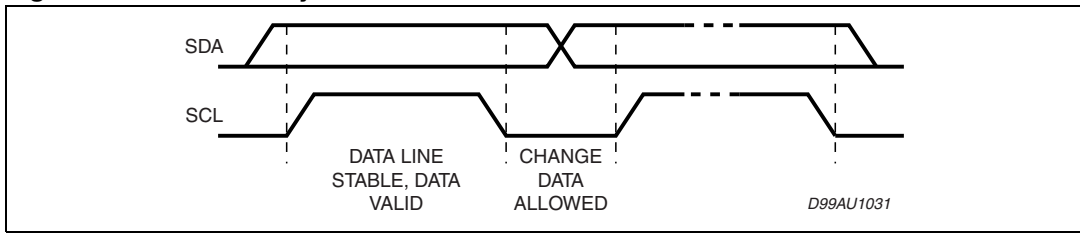


Figure 21. Timing diagram of S-bus and I<sup>2</sup>C bus

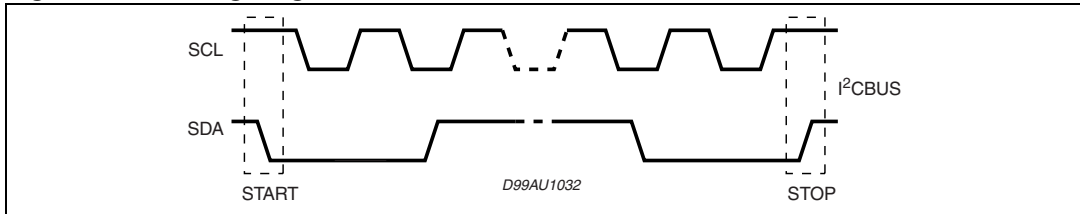
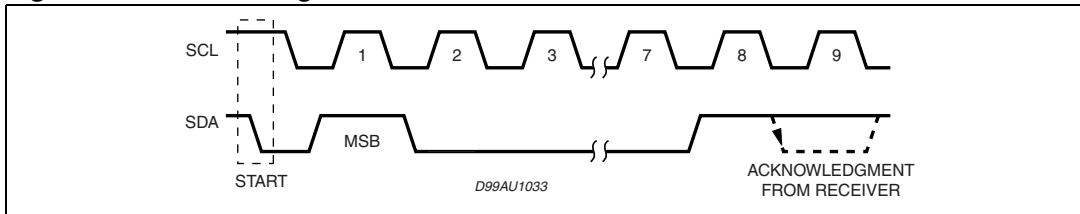


Figure 22. Acknowledge on the I<sup>2</sup>C bus



**Patent note:** Purchase of I<sup>2</sup>C Components of STMicroelectronics, conveys a license under the Philips I<sup>2</sup>C Patent Rights to use these components in an I<sup>2</sup>C system, provided that the system conforms to the I<sup>2</sup>C Standard Specifications as defined by Philips.

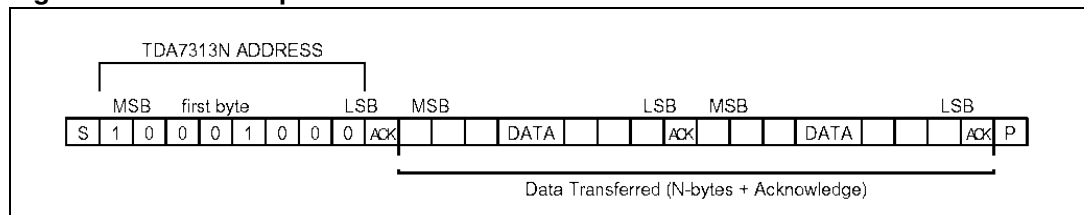
## 4 Software specification

### 4.1 Interface protocol

The interface protocol comprises:

- A start condition (s)
- A chip address byte, containing the TDA7303 address (the 8th bit of the byte must be 0).  
The TDA7303 must always acknowledge at the end of each transmitted byte.
- A sequence of data (N-bytes + acknowledge)
- A stop condition (P)

**Figure 23. Interface protocol**



ACK = Acknowledge

S = Start

P = Stop

Max. clock speed 400 kbits/s

### 4.2 Subaddress (receive mode)

**Table 6. Chip address**

MSB							LSB
1	0	0	0	1	0	0	0

**Table 7. Data bytes**

MSB					LSB			Function
0	0	B2	B1	B0	A2	A1	A0	Volume control
1	1	0	B1	B0	A2	A1	A0	Speaker ATT LR
1	1	1	B1	B0	A2	A1	A0	Speaker ATT RR
1	0	0	B1	B0	A2	A1	A0	Speaker ATT LF
1	0	1	B1	B0	A2	A1	A0	Speaker ATT RF
0	1	0	G1	G0	S2	S1	S0	Audio switch
0	1	1	0	C3	C2	C1	C0	Bass control
0	1	1	1	C3	C2	C1	C0	Treble control

Ax = 1.25dB steps; Bx = 10dB steps; Cx = 2dB steps; Gx = 3.75dB steps

### 4.3 Data bytes (detailed description)

Table 8. Volume

MSB					LSB			Function
0	0	B2	B1	B0	A2	A1	A0	Volume 1.25 dB steps
					0	0	0	0
					0	0	1	-1.25
					0	1	0	-2.5
					0	1	1	-3.75
					1	0	0	-5
					1	0	1	-6.25
					1	1	0	-7.5
					1	1	1	-8.75
								<b>Volume 10 dB steps</b>
		0	0	0				0
		0	0	1				-10
		0	1	0				-20
		0	1	1				-30
		1	0	0				-40
		1	0	1				-50
		1	1	0				-60
		1	1	1				-70

For example a volume of -45 dB is given by: 0 0 1 0 0 1 0 0

Table 9. Speaker attenuators

MSB					LSB			Function
1	0	0	B1	B0	A2	A1	A0	Speaker LF
1	0	1	B1	B0	A2	A1	A0	Speaker RF
1	1	0	B1	B0	A2	A1	A0	Speaker LR
1	1	1	B1	B0	A2	A1	A0	Speaker RR
					0	0	0	0
					0	0	1	-1.25
					0	1	0	-2.5
					0	1	1	-3.75
					1	0	0	-5
					1	0	1	-6.25
					1	1	0	-7.5
					1	1	1	-8.75
			0	0				0
			0	1				-10
			1	0				-20
			1	1				-30
			1	1	1	1	1	Mute

For example attenuation of 25 dB on speaker RF is given by: 1 0 1 1 0 1 0 0

Table 10. Audio switch

MSB				LSB				Function
0	1	0	G1	G0	S2	S1	S0	Audio Switch
						0	0	Stereo 1
						0	1	Stereo 2
						1	0	Stereo 3
						1	1	Not allowed
					0			Loudness ON
					1			Loudness OFF
			0	0				+11.25 dB
			0	1				+7.5 dB
			1	0				+3.75d B
			1	1				0 dB

For example to select the stereo 2 input with a gain of +7.5dB LOUDNESS ON the 8bit string is: 0 1 0 0 1 0 0 1

Table 11. Bass and treble

MSB				LSB				Function
0	1	1	0	C3	C2	C1	C0	Bass
0	1	1	1	C3	C2	C1	C0	Treble
				0	0	0	0	-14
				0	0	0	1	-12
				0	0	1	0	-10
				0	0	1	1	-8
				0	1	0	0	-6
				0	1	0	1	-4
				0	1	1	0	-2
				0	1	1	1	0
				1	1	1	1	0
				1	1	1	0	2
				1	1	0	1	4
				1	1	0	0	6
				1	0	1	1	8
				1	0	1	0	10
				1	0	0	1	12
				1	0	0	0	14

C3 = Sign

For example Bass at -10dB is obtained by the following 8 bit string: 0 1 1 0 0 0 1 0

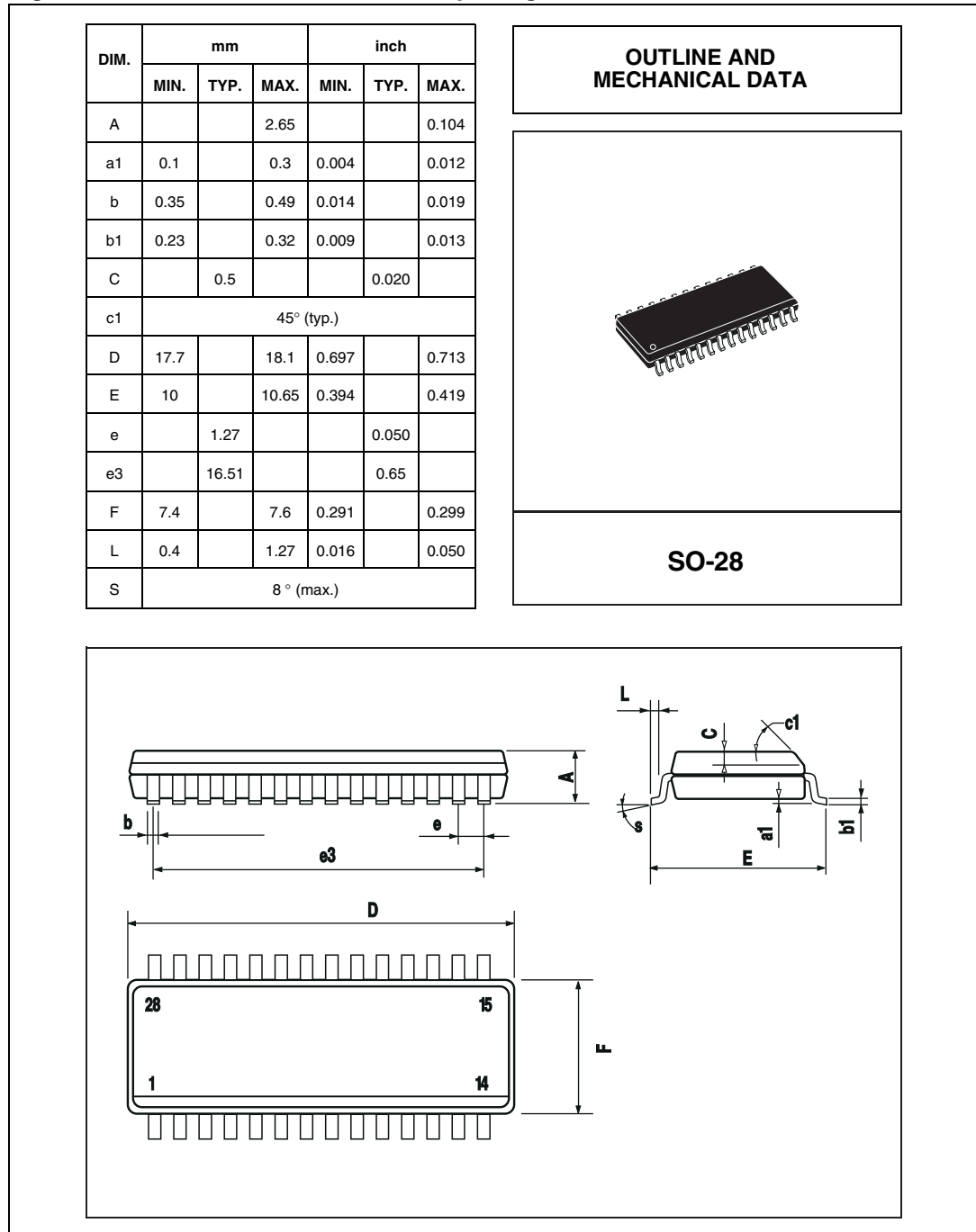


## 5 Package information

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: [www.st.com](http://www.st.com).

ECOPACK® is an ST trademark.

**Figure 24. SO-28 mechanical data and package dimensions**



## 6 Revision history

**Table 12. Document revision history**

Date	Revision	Changes
04-Aug-2006	1	Initial release.
13-Mar-2009	2	Updated “distortion” parameter in the <a href="#">Table 5: Electrical characteristics</a> on the page 9. Modified the max. clock speed value in <a href="#">Section 4.1: Interface protocol on page 15</a> . Updated <a href="#">Section 5: Package information on page 18</a> .
18-Mar-2009	3	Modified the test condition of the parameter “distortion” in the <a href="#">Table 5: Electrical characteristics</a> on the page 9.
17-Sep-2013	4	Updated Disclaimer

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