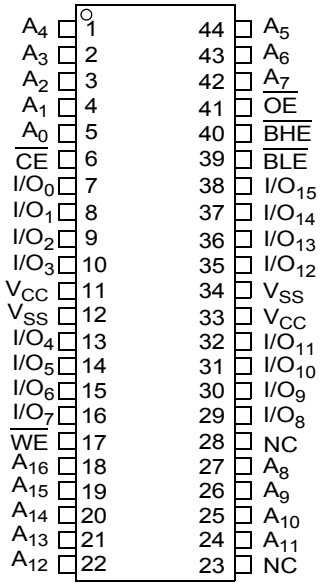
## Contents

## Product Portfolio

| Product | Range | $V_{CC}$ Range (V) | | | Speed (ns) | Power Dissipation | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | | | | Operating $I_{CC}$ (mA) | | | | Standby $I_{SB2}$ (µA) | |
| | | | | | | f = 1MHz | | f = $f_{max}$ | | | |
| | | Min | Typ [1] | Max | | Typ [1] | Max | Typ [1] | Max | Typ [1] | Max |
| CY62137FV30LL | Automotive-A | 2.2 V | 3.0 V | 3.6 V | 45 | 1.6 | 2.5 | 13 | 18 | 1 | 5 |
| | Automotive-E | 2.2 V | 3.0 V | 3.6 V | 55 | 2 | 3 | 15 | 25 | 1 | 20 |

## Pin Configuration

**Figure 1. 44-pin TSOP II pinout [2]**




**Notes**
1. Typical values are included for reference only and are not guaranteed or tested. Typical values are measured at $V_{CC} = V_{CC(typ)}$, $T_A = 25$ °C.
2. NC pins are not connected on the die.

## Maximum Ratings

Exceeding the maximum ratings may impair the useful life of the device. These user guidelines are not tested.

Storage temperature ..... –65 °C to + 150 °C

Ambient temperature with power applied ..... –55 °C to + 125 °C

Supply voltage to ground potential .....–0.3 V to 3.9 V

DC voltage applied to outputs in High Z state [3, 4] .....–0.3 V to 3.9 V

DC input voltage [4] .....–0.3 V to 3.9 V

Output current into outputs (LOW) ..... 20 mA

Static discharge voltage (MIL-STD-883, method 3015) ..... > 2001 V

Latch up current .....> 200 mA

## Operating Range

| Device | Range | Ambient Temperature | $V_{CC}$[5] |
|---|---|---|---|
| CY62137FV30LL | Automotive-A | –40 °C to +85 °C | 2.2 V to 3.6 V |
| | Automotive-E | –40 °C to +125 °C | |

## Electrical Characteristics

Over the Operating Range

| Parameter | Description | Test Conditions | | 45 ns (Automotive-A) | | | 55 ns (Automotive-E) | | | Unit |
|---|---|---|---|---|---|---|---|---|---|---|
| | | | | Min | Typ [6] | Max | Min | Typ [6] | Max | |
| $V_{OH}$ | Output high voltage | $2.2 \le V_{CC} \le 2.7$ | $I_{OH}$ = –0.1 mA | 2.0 | – | – | 2.0 | – | – | V |
| | | $2.7 \le V_{CC} \le 3.6$ | $I_{OH}$ = –1.0 mA | 2.4 | – | – | 2.4 | – | – | V |
| $V_{OL}$ | Output low voltage | $2.2 \le V_{CC} \le 2.7$ | $I_{OL}$ = 0.1 mA | – | – | 0.4 | – | – | 0.4 | V |
| | | $2.7 \le V_{CC} \le 3.6$ | $I_{OL}$ = 2.1 mA | – | – | 0.4 | – | – | 0.4 | V |
| $V_{IH}$ | Input high voltage | $2.2 \le V_{CC} \le 2.7$ | | 1.8 | – | $V_{CC}$ + 0.3 | 1.8 | – | $V_{CC}$ + 0.3 | V |
| | | $2.7 \le V_{CC} \le 3.6$ | | 2.2 | – | $V_{CC}$ + 0.3 | 2.2 | – | $V_{CC}$ + 0.3 | V |
| $V_{IL}$ | Input low voltage | $2.2 \le V_{CC} \le 2.7$ | | –0.3 | – | 0.6 | –0.3 | – | 0.6 | V |
| | | $2.7 \le V_{CC} \le 3.6$ | | –0.3 | – | 0.8 | –0.3 | – | 0.8 | V |
| $I_{IX}$ | Input leakage current | $GND \le V_I \le V_{CC}$ | | –1 | – | +1 | –4 | – | +4 | µA |
| $I_{OZ}$ | Output leakage current | $GND \le V_O \le V_{CC}$, Output disabled | | –1 | – | +1 | –4 | – | +4 | µA |
| $I_{CC}$ | $V_{CC}$ operating supply current | $f = f_{max} = 1/t_{RC}$ | $V_{CC} = V_{CC(max)}$, $I_{OUT}$ = 0 mA CMOS levels | – | 13 | 18 | – | 15 | 25 | mA |
| | | f = 1 MHz | | – | 1.6 | 2.5 | – | 2 | 3 | |
| $I_{SB1}$[7] | Automatic power down current – CMOS inputs | $\overline{CE} \ge V_{CC} - 0.2$ V or ($\overline{BHE}$ and $\overline{BLE}$) $\ge V_{CC} - 0.2$ V, $V_{IN} \ge V_{CC} - 0.2$ V, $V_{IN} \le 0.2$ V, f = $f_{max}$ (address and data only), f = 0 ($\overline{OE}$ and $\overline{WE}$), $V_{CC} = V_{CC(max)}$ | | – | 1 | 5 | – | 1 | 20 | µA |
| $I_{SB2}$[7] | Automatic power down current – CMOS inputs | $\overline{CE} \ge V_{CC} - 0.2$ V or ($\overline{BHE}$ and $\overline{BLE}$) $\ge V_{CC} - 0.2$ V, $V_{IN} \ge V_{CC} - 0.2$ V or $V_{IN} \le 0.2$ V, f = 0, $V_{CC} = V_{CC(max)}$ | | – | 1 | 5 | – | 1 | 20 | µA |

**Notes**

3. $V_{IL(min)}$ = –2.0 V for pulse durations less than 20 ns.
4. $V_{IH(max)} = V_{CC}$ + 0.75 V for pulse durations less than 20 ns.
5. Full device AC operation assumes a minimum of 100 µs ramp time from 0 to $V_{CC(min)}$ and 200 µs wait time after $V_{CC}$ stabilization.
6. Typical values are included for reference only and are not guaranteed or tested. Typical values are measured at $V_{CC} = V_{CC(typ)}$, $T_A$ = 25 °C.
7. Chip enable ($\overline{CE}$) and byte enables ($\overline{BHE}$ and $\overline{BLE}$) need to be tied to CMOS levels to meet the $I_{SB1}$ / $I_{SB2}$ / $I_{CCDR}$ specification. Other inputs can be left floating.

## Capacitance

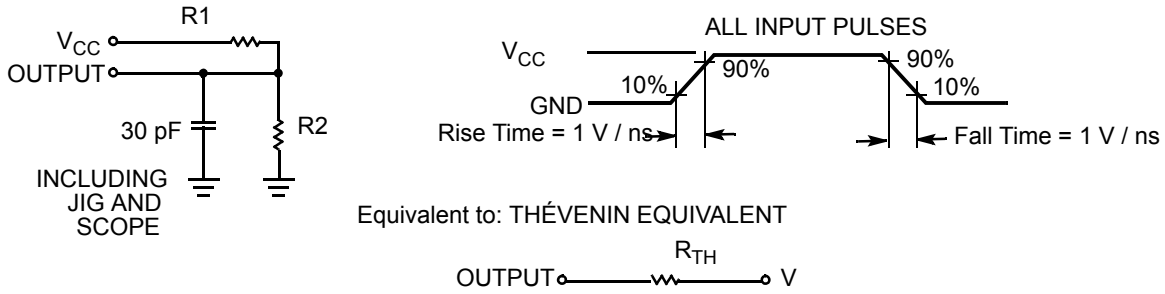
| Parameter [8] | Description | Test Conditions | Max | Unit |
|---|---|---|---|---|
| $C_{IN}$ | Input capacitance | $T_A$ = 25 °C, f = 1 MHz, $V_{CC}$ = $V_{CC(typ)}$ | 10 | pF |
| $C_{OUT}$ | Output capacitance | | 10 | pF |

## Thermal Resistance

| Parameter [8] | Description | Test Conditions | TSOP II | Unit |
|---|---|---|---|---|
| $\Theta_{JA}$ | Thermal resistance (junction to ambient) | Still air, soldered on a 3 × 4.5 inch, two layer printed circuit board | 77 | °C/W |
| $\Theta_{JC}$ | Thermal resistance (junction to case) | | 13 | °C/W |

## AC Test Loads and Waveforms

**Figure 2. AC Test Loads and Waveforms**




| Parameters | 2.5 V (2.2 V to 2.7 V) | 3.0 V (2.7 V to 3.6 V) | Unit |
|---|---|---|---|
| R1 | 16667 | 1103 | Ω |
| R2 | 15385 | 1554 | Ω |
| $R_{TH}$ | 8000 | 645 | Ω |
| $V_{TH}$ | 1.20 | 1.75 | V |

**Note**
8. Tested initially and after any design or process changes that may affect these parameters.

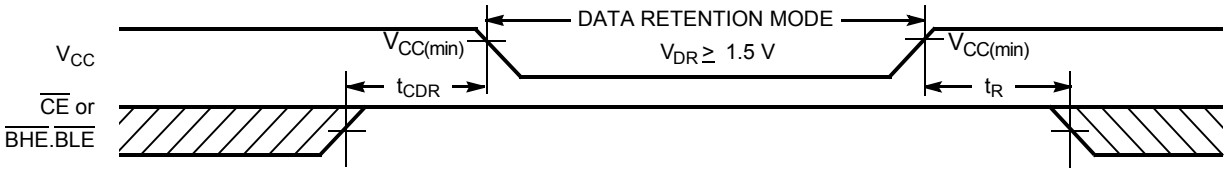
## Data Retention Characteristics

Over the Operating Range

| Parameter | Description | Conditions | | Min | Typ [9] | Max | Unit |
|---|---|---|---|---|---|---|---|
| $V_{DR}$ | $V_{CC}$ for data retention | | | 1.5 | – | – | V |
| $I_{CCDR}$ [10] | Data retention current | $V_{CC}$ = 1.5 V, $\overline{CE} \geq V_{CC} - 0.2$ V or ($\overline{BHE}$ and $\overline{BLE}$) $\geq V_{CC} - 0.2$ V $V_{IN} \geq V_{CC} - 0.2$ V or $V_{IN} \leq 0.2$ V | Automotive-A | – | – | 4 | µA |
| | | | Automotive-E | – | – | 12 | – |
| $t_{CDR}$ [11] | Chip deselect to data retention time | | | 0 | – | – | ns |
| $t_R$ [12] | Operation recovery time | | CY62137FV30LL-45 | 45 | – | – | ns |
| | | | CY62137FV30LL-55 | 55 | | | |

## Data Retention Waveform

**Figure 3. Data Retention Waveform** [13]




**Notes**
9. Typical values are included for reference only and are not guaranteed or tested. Typical values are measured at $V_{CC} = V_{CC(typ)}$, $T_A$ = 25 °C
10. Chip enable ($\overline{CE}$) and byte enables ($\overline{BHE}$ and $\overline{BLE}$) need to be tied to CMOS levels to meet the $I_{SB1}$ / $I_{SB2}$ / $I_{CCDR}$ specification. Other inputs can be left floating.
11. Tested initially and after any design or process changes that may affect these parameters.
12. Full device operation requires linear $V_{CC}$ ramp from $V_{DR}$ to $V_{CC(min)} \geq 100$ µs or stable at $V_{CC(min)} \geq 100$ µs.
13. $\overline{BHE}.\overline{BLE}$ is the AND of both $\overline{BHE}$ and $\overline{BLE}$. Deselect the chip by either disabling chip enable signals or by disabling both $\overline{BHE}$ and $\overline{BLE}$.

## Switching Characteristics

| Parameter [14, 15] | Description | 45 ns (Automotive-A) | | 55 ns (Automotive-E) | | Unit |
|---|---|---|---|---|---|---|
| | | Min | Max | Min | Max | |
| **Read Cycle** | | | | | | |
| $t_{RC}$ | Read cycle time | 45 | – | 55 | – | ns |
| $t_{AA}$ | Address to data valid | – | 45 | – | 55 | ns |
| $t_{OHA}$ | Data hold from address change | 10 | – | 10 | – | ns |
| $t_{ACE}$ | $\overline{CE}$ LOW to data valid | – | 45 | – | 55 | ns |
| $t_{DOE}$ | $\overline{OE}$ LOW to data valid | – | 22 | – | 25 | ns |
| $t_{LZOE}$ | $\overline{OE}$ LOW to low Z [16] | 5 | – | 5 | – | ns |
| $t_{HZOE}$ | $\overline{OE}$ HIGH to high Z [16, 17] | – | 18 | – | 20 | ns |
| $t_{LZCE}$ | $\overline{CE}$ LOW to low Z [16] | 10 | – | 10 | – | ns |
| $t_{HZCE}$ | $\overline{CE}$ HIGH to high Z [16, 17] | – | 18 | – | 20 | ns |
| $t_{PU}$ | $\overline{CE}$ LOW to power-up | 0 | – | 0 | – | ns |
| $t_{PD}$ | $\overline{CE}$ HIGH to power-down | – | 45 | – | 55 | ns |
| $t_{DBE}$ | $\overline{BLE}$/$\overline{BHE}$ LOW to data valid | – | 45 | – | 55 | ns |
| $t_{LZBE}$ | $\overline{BLE}$/$\overline{BHE}$ LOW to low Z [16, 18] | 5 | – | 10 | – | ns |
| $t_{HZBE}$ | $\overline{BLE}$/$\overline{BHE}$ HIGH to high Z [16, 17] | – | 18 | – | 20 | ns |
| **Write Cycle** [19] | | | | | | |
| $t_{WC}$ | Write cycle time | 45 | – | 55 | – | ns |
| $t_{SCE}$ | $\overline{CE}$ LOW to write end | 35 | – | 40 | – | ns |
| $t_{AW}$ | Address setup to write end | 35 | – | 40 | – | ns |
| $t_{HA}$ | Address hold from write end | 0 | – | 0 | – | ns |
| $t_{SA}$ | Address setup to write start | 0 | – | 0 | – | ns |
| $t_{PWE}$ | $\overline{WE}$ pulse width | 35 | – | 40 | – | ns |
| $t_{BW}$ | $\overline{BLE}$/$\overline{BHE}$ LOW to write end | 35 | – | 40 | – | ns |
| $t_{SD}$ | Data setup to write end | 25 | – | 25 | – | ns |
| $t_{HD}$ | Data hold from write end | 0 | – | 0 | – | ns |
| $t_{HZWE}$ | $\overline{WE}$ LOW to high Z [16, 17] | – | 18 | – | 20 | ns |
| $t_{LZWE}$ | $\overline{WE}$ HIGH to low Z [16] | 10 | – | 10 | – | ns |

**Notes**
14. Test conditions for all parameters, other than tristate parameters, assume signal transition time of 3 ns (1 V/ns) or less, timing reference levels of $V_{CC(typ)}/2$, input pulse levels of 0 to $V_{CC(typ)}$, and output loading of the specified $I_{OL}/I_{OH}$ as shown in Figure 2 on page 5.
15. AC timing parameters are subject to byte enable signals ($\overline{BHE}$ or $\overline{BLE}$) not switching when chip is disabled. Please see application note AN13842 for further clarification.
16. At any temperature and voltage condition, $t_{HZCE}$ is less than $t_{LZCE}$, $t_{HZBE}$ is less than $t_{LZBE}$, $t_{HZOE}$ is less than $t_{LZOE}$, and $t_{HZWE}$ is less than $t_{LZWE}$ for any device.
17. $t_{HZOE}$, $t_{HZCE}$, $t_{HZBE}$, and $t_{HZWE}$ transitions are measured when the outputs enter a high impedance state.
18. If both byte enables are toggled together, this value is 10 ns.
19. The internal write time of the memory is defined by the overlap of $\overline{WE}$, $\overline{CE}$ = $V_{IL}$, $\overline{BHE}$ and/or $\overline{BLE}$ = $V_{IL}$. All signals are ACTIVE to initiate a write and any of these signals terminate a write by going INACTIVE. The data input setup and hold timing are referenced to the edge of the signal that terminates the write.

## Switching Waveforms

**Figure 4. Read Cycle 1: Address Transition Controlled** [20, 21]

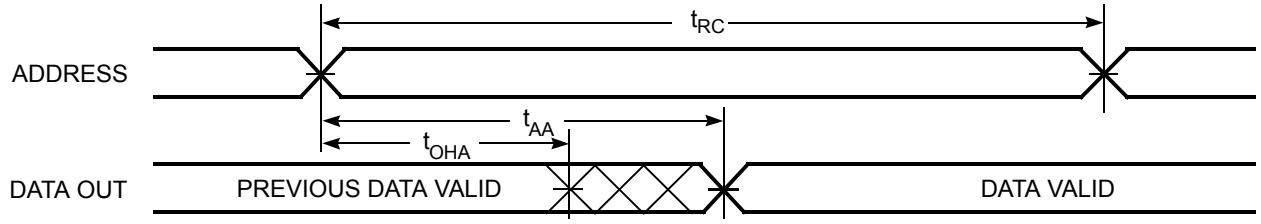
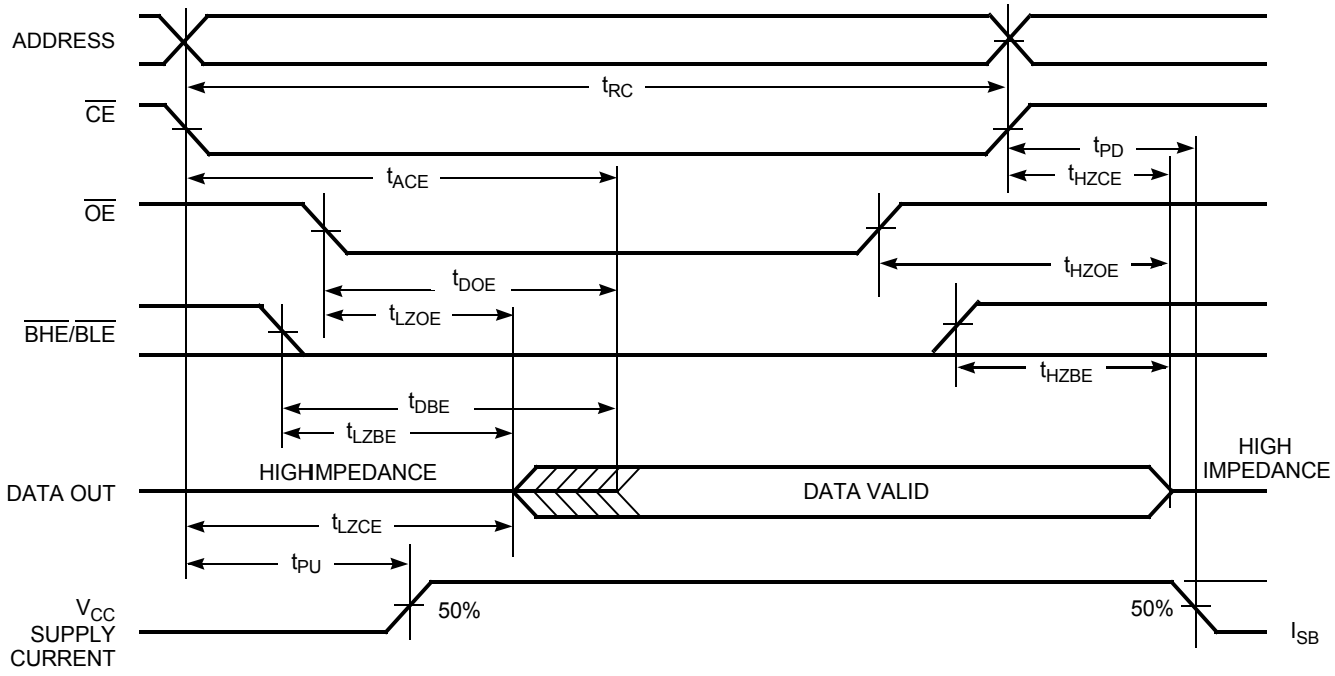



**Figure 5. Read Cycle 2: $\overline{OE}$ Controlled** [21, 22]




**Notes**
20. The device is continuously selected. $\overline{OE}$, $\overline{CE}$ = $V_{IL}$, $\overline{BHE}$ and/or $\overline{BLE}$ = $V_{IL}$.
21. $\overline{WE}$ is HIGH for read cycle.
22. Address valid before or similar to $\overline{CE}$ and $\overline{BHE}$, $\overline{BLE}$ transition LOW.

## Switching Waveforms (continued)

**Figure 6. Write Cycle 1: $\overline{WE}$ Controlled** [23, 24, 25]

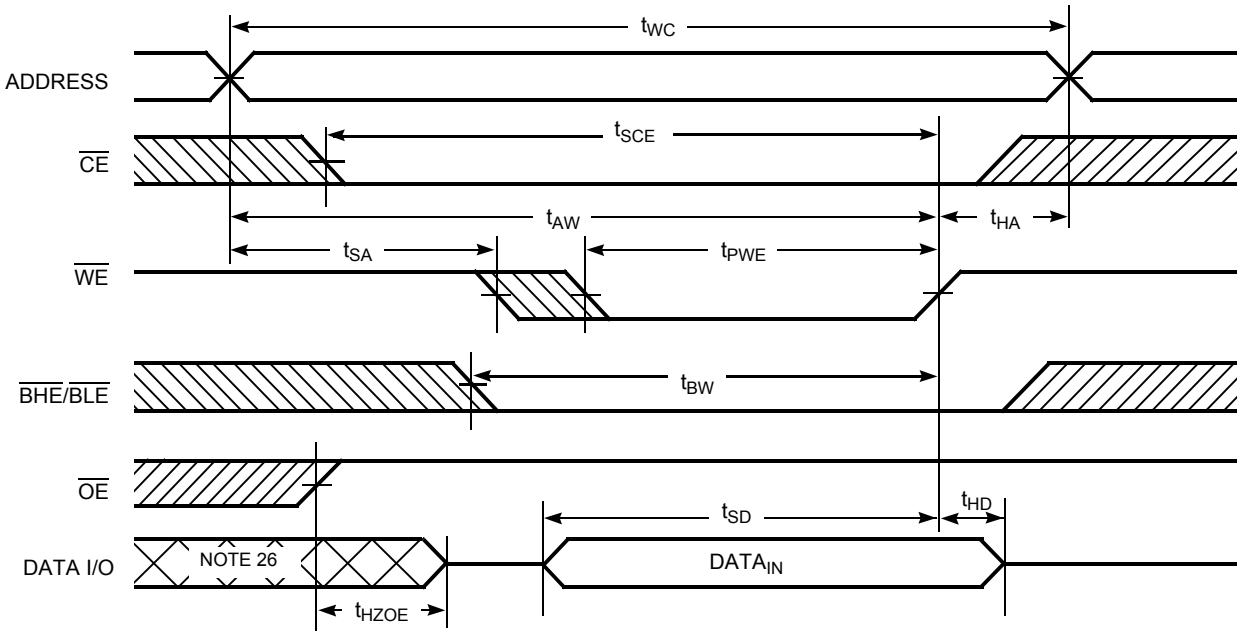
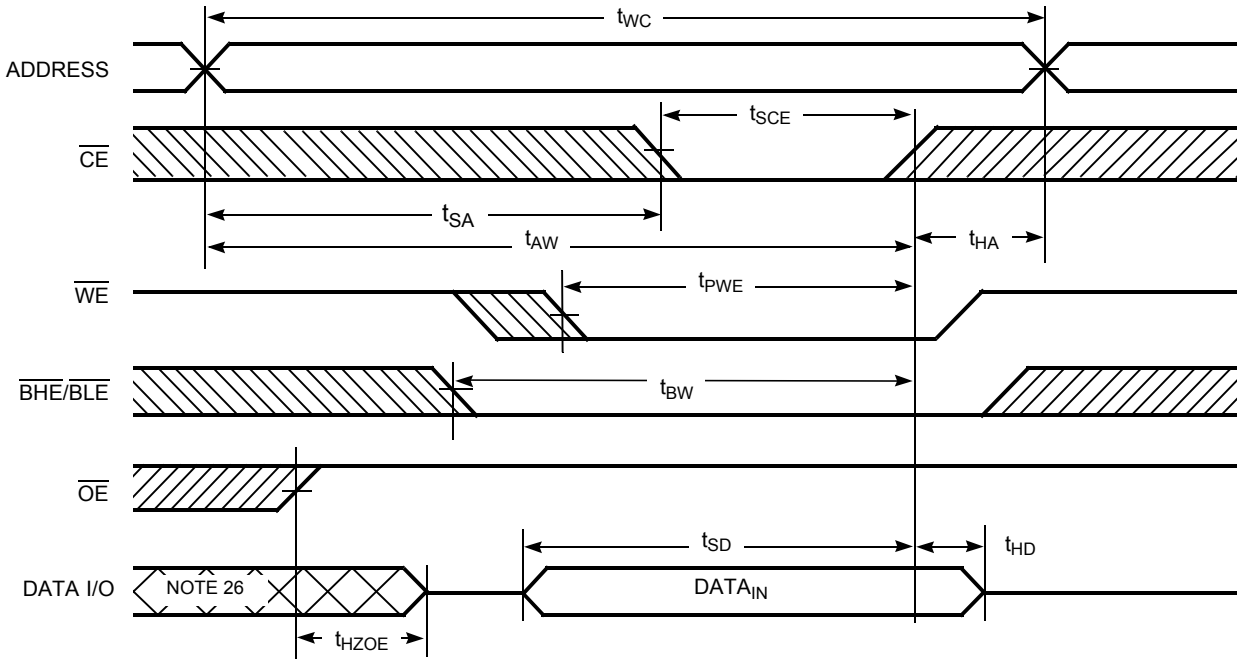



**Figure 7. Write Cycle 2: $\overline{CE}$ Controlled** [23, 24, 25]




**Notes**

23. The internal write time of the memory is defined by the overlap of $\overline{WE}$, $\overline{CE}$ = $V_{IL}$, $\overline{BHE}$ and/or $\overline{BLE}$ = $V_{IL}$. All signals are ACTIVE to initiate a write and any of these signals terminate a write by going INACTIVE. The data input setup and hold timing are referenced to the edge of the signal that terminates the write.
24. Data I/O is high impedance if $\overline{OE}$ = $V_{IH}$.
25. If $\overline{CE}$ goes HIGH simultaneously with $\overline{WE}$ = $V_{IH}$, the output remains in a high impedance state.
26. During this period, the I/Os are in output state. Do not apply input signals.

## Switching Waveforms (continued)

**Figure 8. Write Cycle 3: $\overline{WE}$ Controlled, $\overline{OE}$ LOW [27]**

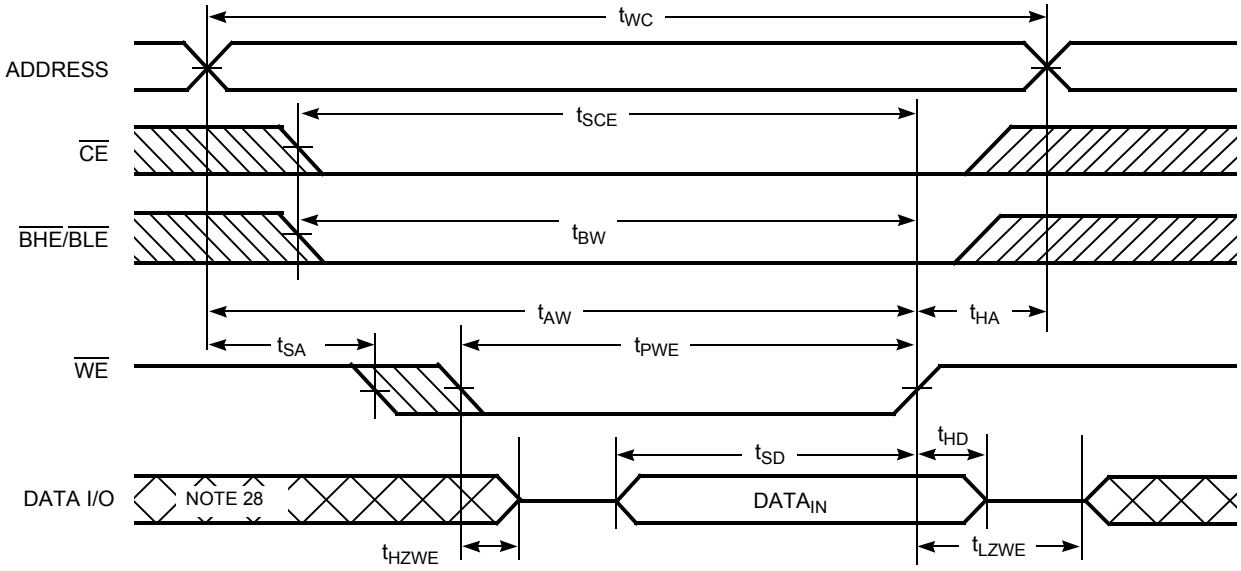
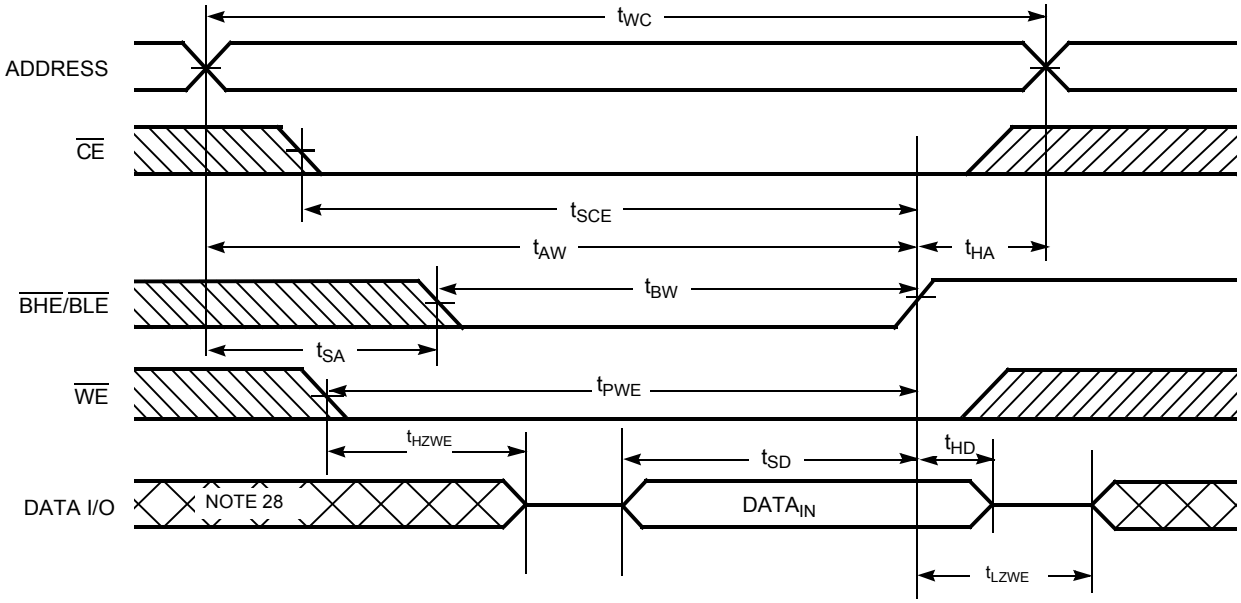



**Figure 9. Write Cycle 4: $\overline{BHE}/\overline{BLE}$ Controlled, $\overline{OE}$ LOW [27]**




**Notes**
27. If $\overline{CE}$ goes HIGH simultaneously with $\overline{WE}$ = $V_{IH}$, the output remains in a high impedance state.
28. During this period, the I/Os are in output state. Do not apply input signals.

## Truth Table

| $\overline{CE}$ | $\overline{WE}$ | $\overline{OE}$ | $\overline{BHE}$ | $\overline{BLE}$ | Inputs or Outputs | Mode | Power |
|---|---|---|---|---|---|---|---|
| H | X | X | X [29] | X [29] | High Z | Deselect or power-down | Standby ($I_{SB}$) |
| X [29] | X | X | H | H | High Z | Deselect or power-down | Standby ($I_{SB}$) |
| L | H | L | L | L | Data out ($I/O_0$–$I/O_{15}$) | Read | Active ($I_{CC}$) |
| L | H | L | H | L | Data out ($I/O_0$–$I/O_7$); $I/O_8$–$I/O_{15}$ in High Z | Read | Active ($I_{CC}$) |
| L | H | L | L | H | Data out ($I/O_8$–$I/O_{15}$); $I/O_0$–$I/O_7$ in High Z | Read | Active ($I_{CC}$) |
| L | H | H | L | L | High Z | Output disabled | Active ($I_{CC}$) |
| L | H | H | H | L | High Z | Output disabled | Active ($I_{CC}$) |
| L | H | H | L | H | High Z | Output disabled | Active ($I_{CC}$) |
| L | L | X | L | L | Data in ($I/O_0$–$I/O_{15}$) | Write | Active ($I_{CC}$) |
| L | L | X | H | L | Data in ($I/O_0$–$I/O_7$); $I/O_8$–$I/O_{15}$ in High Z | Write | Active ($I_{CC}$) |
| L | L | X | L | H | Data in ($I/O_8$–$I/O_{15}$); $I/O_0$–$I/O_7$ in High Z | Write | Active ($I_{CC}$) |

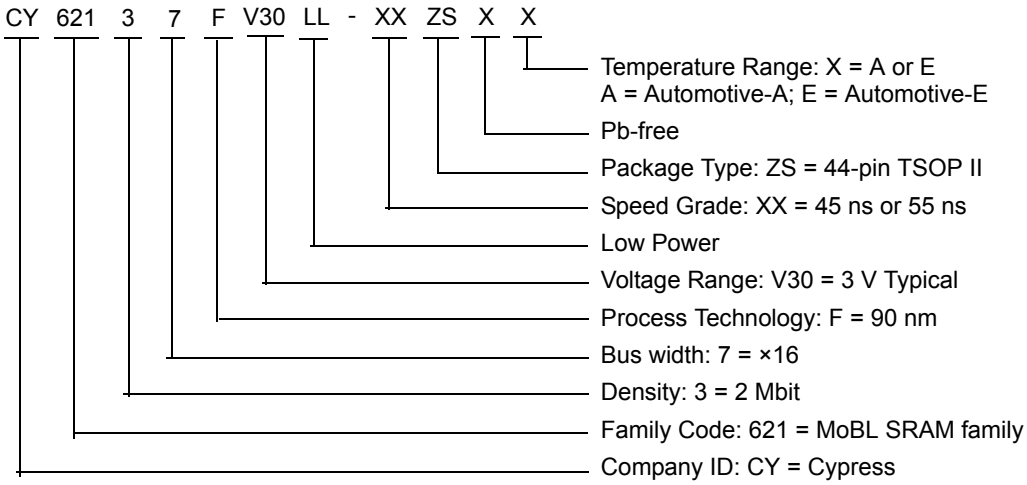
**Note**
29. The 'X' (Don't care) state for the Chip enable ($\overline{CE}$) and Byte enables ($\overline{BHE}$ and $\overline{BLE}$) in the truth table refer to the logic state (either HIGH or LOW). Intermediate voltage levels on these pins is not permitted.

## Ordering Information

| Speed (ns) | Ordering Code | Package Diagram | Package Type | Operating Range |
|---|---|---|---|---|
| 45 | CY62137FV30LL-45ZSXA | 51-85087 | 44-pin TSOP II (Pb-free) | Automotive-A |
| 55 | CY62137FV30LL-55ZSXE | | | Automotive-E |

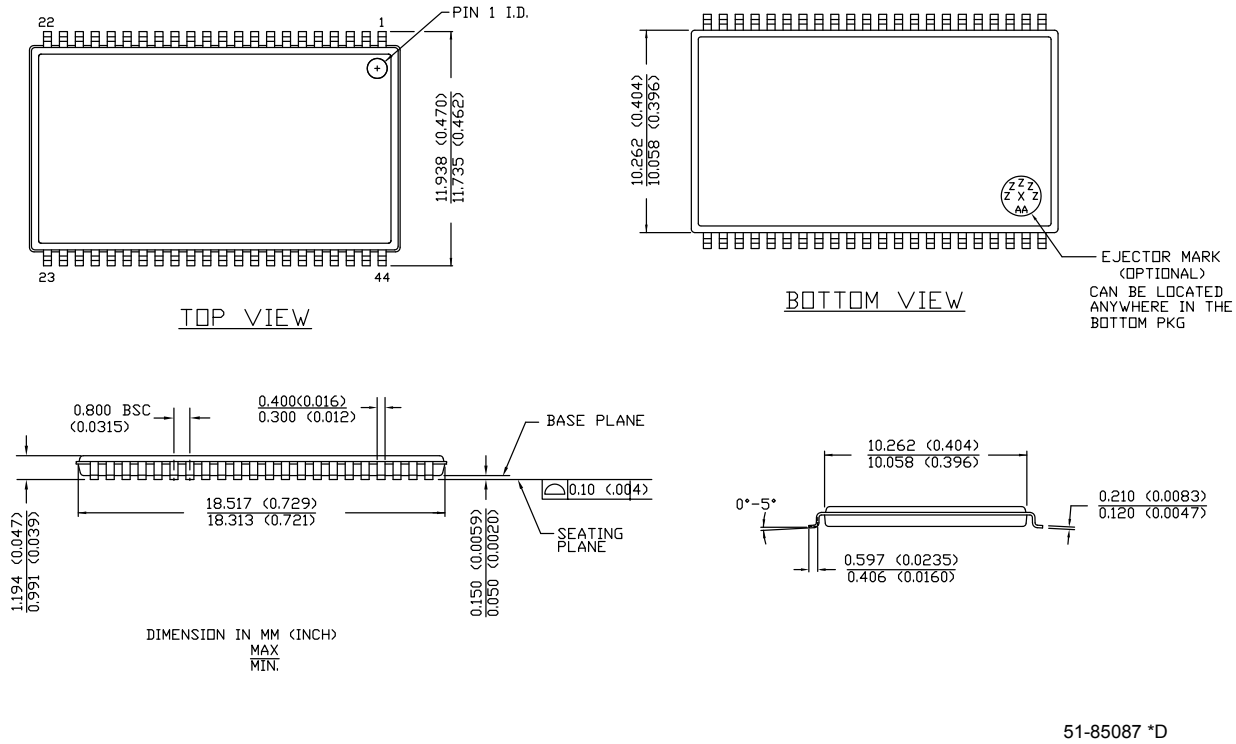
Contact your local Cypress sales representative for availability of these parts.

### Ordering Code Definitions



## Package Diagrams

**Figure 10. 44-pin TSOP Z44-II Package Outline, 51-85087**



## Acronyms

| Acronym | Description |
|---|---|
| $\overline{BHE}$ | byte high enable |
| $\overline{BLE}$ | byte low enable |
| $\overline{CE}$ | chip enable |
| CMOS | complementary metal oxide semiconductor |
| I/O | input/output |
| $\overline{OE}$ | output enable |
| SRAM | static random access memory |
| TSOP | thin small outline package |
| $\overline{WE}$ | write enable |

## Document Conventions

### Units of Measure

| Symbol | Unit of Measure |
|---|---|
| °C | degree Celsius |
| MHz | megahertz |
| µA | microampere |
| µs | microsecond |
| mA | milliampere |
| ns | nanosecond |
| Ω | ohm |
| pF | picofarad |
| V | volt |
| W | watt |

## Document History Page

| Document Title: CY62137FV30 MoBL®, Automotive 2-Mbit (128 K × 16) Static RAM<br>Document Number: 001-66190 | | | | |
|---|---|---|---|---|
| **Rev.** | **ECN No.** | **Issue Date** | **Orig. of Change** | **Description of Change** |
| ** | 3124003 | 01/12/2011 | RAME | Created new Automotive datasheet from document number 001-07141 Rev. *H |
| *A | 3503362 | 01/20/2012 | TAVA | Updated Functional Description.<br>Updated Package Diagrams.<br>Updated in new template. |

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