Low-Cost, Low-Power, 6-Bit DACs with 3-Wire Serial Interface in SOT23

ABSOLUTE MAXIMUM RATINGS

V_{DD} to GND .....-0.3V to +6V
OUT .....-0.3V to (V_{DD} + 0.3V)
$\overline{CS}$, SCLK, DIN to GND .....-0.3V to +6V
Maximum Current into Any Pin.....50mA
Continuous Power Dissipation (T_A = +70°C)
6-Pin SOT23 (derate 8.7mW/°C above +70°C).....696mW

Operating Temperature Range .....-40°C to +85°C
Storage Temperature Range .....-65°C to +150°C
Maximum Junction Temperature .....+150°C
Lead Temperature (soldering, 10s) .....+300°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

(V_{DD} = +2.7V to +3.6V (MAX5363), V_{DD} = +4.5V to +5.5V (MAX5364), V_{DD} = +2.7V to +5.5V (MAX5365), R_L = 10kΩ, C_L = 50pF, T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are T_A = +25°C.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
STATIC ACCURACY							
Resolution				6			Bits
Integral Linearity Error	INL	(Note 1)				±1	LSB
Differential Linearity Error	DNL	Guaranteed monotonic				±1	LSB
Offset Error	V_{OS}	(Note 2)			±1	±25	mV
Offset Error Supply Rejection		MAX5365 (Notes 2, 3)				60	dB
Offset Error Temperature Coefficient		MAX5363/MAX5364			3		ppm/°C
		MAX5365			1		
Full-Scale Error		Code = 63, no load	MAX5363/MAX5364			10	% of ideal FS
			MAX5365			5	
Full-Scale Error Supply		Code = 63 (Note 4)	MAX5363/MAX5364			50	dB
Full-Scale Error Temperature Coefficient		Code = 63	MAX5363/MAX5364		±40		ppm/°C
			MAX5365		±10		
DAC OUTPUT							
Internal Reference Voltage (Note 5)	R_{EF}	MAX5363		1.8	2	2.2	V
		MAX5364		3.6	4	4.4	
		MAX5365		0.85 × V_{DD}	0.9 × V_{DD}	0.95 × V_{DD}	
Output Load Regulation		Code = 63, 0 to 100µA			0.5		LSB
		Code = 0, 0 to 100µA			0.5		
Shutdown Output Resistance to GND		V_{OUT} = 0 to V_{DD}	[D13, D12] = 0, 1		1k		Ω
			[D13, D12] = 1, 0		100k		
			[D13, D12] = 1, 1		1M		
DYNAMIC PERFORMANCE							
Voltage Output Slew Rate		Positive and negative			0.4		V/µs
Output Settling Time		To 1/2 LSB, 50kΩ and 50pF load (Note 6)			20		µs
Digital Feedthrough		Code = 0, all digital inputs from 0 to V_{DD}			2		nVs

ELECTRICAL CHARACTERISTICS (continued)

(V_{DD} = +2.7V to +3.6V (MAX5363), V_{DD} = +4.5V to +5.5V (MAX5364), V_{DD} = +2.7V to +5.5V (MAX5365), R_L = 10kΩ, C_L = 50pF, T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are T_A = +25°C.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Digital-Analog Glitch Impulse		Code 31 to code 32		40		nVs
Wake-Up Time		From software shutdown		50		µs
POWER REQUIREMENTS						
Supply Voltage	V_{DD}	MAX5363	2.7		3.6	V
		MAX5364	4.5		5.5	
		MAX5365	2.7		5.5	
Supply Current	I_{DD}	No load, all digital inputs at 0 or V_{DD}, code = 63		150	230	µA
		Shutdown mode			1	
DIGITAL INPUTS						
Input Low Voltage	V_{IL}				$0.3 \times V_{DD}$	V
Input High Voltage	V_{IH}		$0.7 \times V_{DD}$			V
Input Hysteresis	V_H			$0.05 \times V_{DD}$		V
Input Capacitance	C_{IN}	(Note 7)		10		pF
Input Leakage Current	I_{IN}				±1	µA

TIMING CHARACTERISTICS

(Figures 3 and 4, V_{DD} = +2.7V to +3.6V (MAX5363), V_{DD} = +4.5V to +5.5V (MAX5364), V_{DD} = +2.7V to +5.5V (MAX5365), R_L = 10kΩ, C_L = 50pF, T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are T_A = +25°C.) (Note 7)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
SCLK Period	t_{CP}		100			ns
SCLK Pulse Width High	t_{CH}		40			ns
SCLK Pulse Width Low	t_{CL}		40			ns
$\overline{CS}$ Fall to SCLK Rise Setup Time	t_{CSS}		40			ns
SCLK Rise to $\overline{CS}$ Rise Hold Time	t_{CSH}		0			ns
DIN Setup Time	t_{DS}		40			ns
DIN Hold Time	t_{DH}		0			ns
SCLK Rise to $\overline{CS}$ Fall Delay	t_{CS0}		10			ns
$\overline{CS}$ Rise to SCLK Rise Hold	t_{CS1}		40			ns
$\overline{CS}$ Pulse Width High	t_{CSW}		100			ns

Low-Cost, Low-Power, 6-Bit DACs with 3-Wire Serial Interface in SOT23

TIMING CHARACTERISTICS (continued)

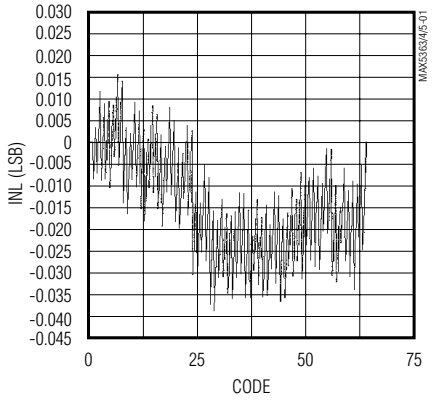
(Figures 3 and 4, V_{DD} = +2.7V to +3.6V (MAX5363), V_{DD} = +4.5V to +5.5V (MAX5364), V_{DD} = +2.7V to +5.5V (MAX5365), R_L = 10kΩ, C_L = 50pF, T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are T_A = +25°C.) (Note 7)

Note 1: Guaranteed from code 2 to code 63.
Note 2: The offset value extrapolated from the range over which the INL is guaranteed.
Note 3: MAX5365 tested at 5V ±10%.
Note 4: MAX5363 tested at 3V ±10%; MAX5364 tested at 5V ±10%.
Note 5: Actual output voltages at full scale are 63/64 × V_{REF}.
Note 6: Output settling time is measured by stepping from code 2 to code 63, and from code 63 to code 2.
Note 7: Guaranteed by design.

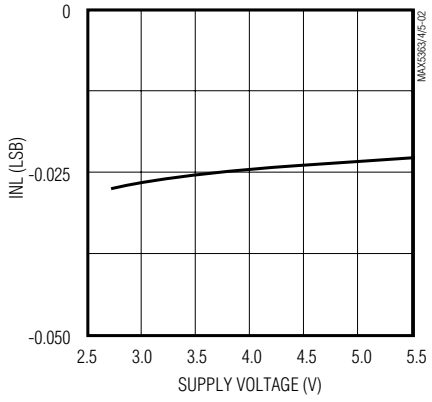
Typical Operating Characteristics

(V_{DD} = +3.0V (MAX5363), V_{DD} = +5.0V (MAX5364/MAX5365), T_A = +25°C, unless otherwise noted.)

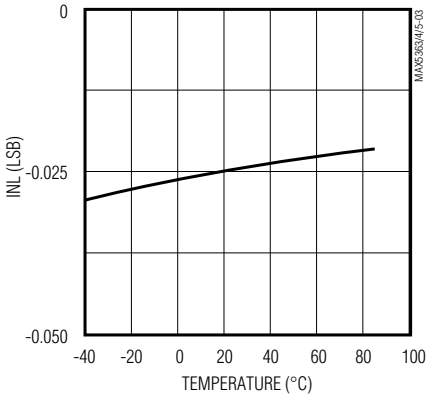
INTEGRAL NONLINEARITY vs. CODE



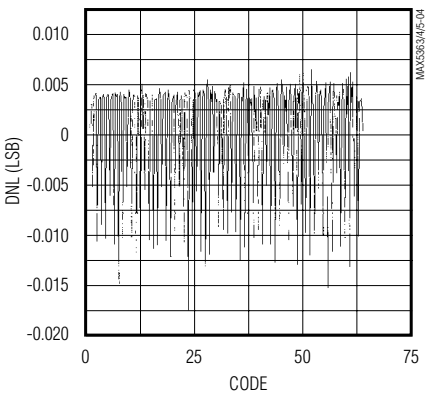
INTEGRAL NONLINEARITY vs. SUPPLY VOLTAGE



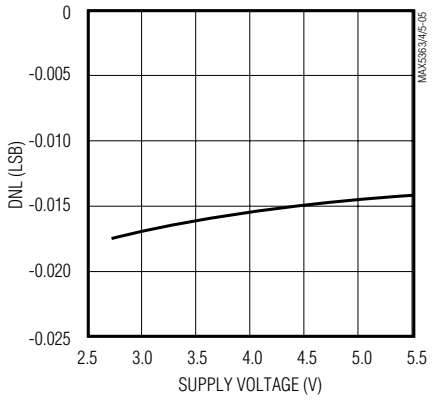
INTEGRAL NONLINEARITY vs. TEMPERATURE



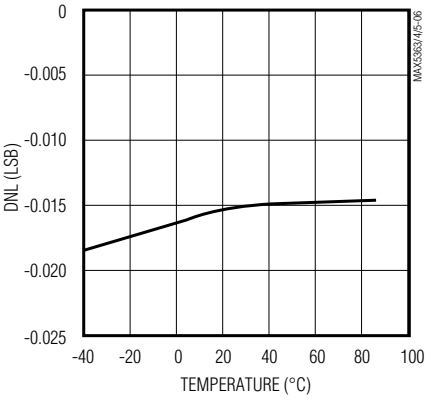
DIFFERENTIAL NONLINEARITY vs. CODE



DIFFERENTIAL NONLINEARITY vs. SUPPLY VOLTAGE



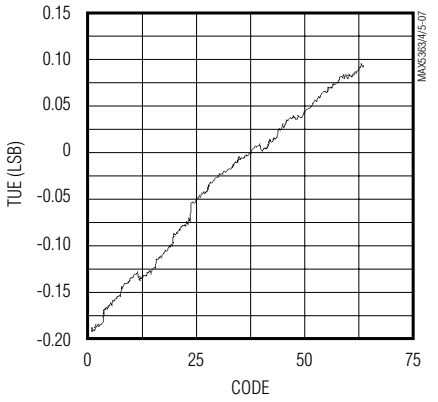
DIFFERENTIAL NONLINEARITY vs. TEMPERATURE



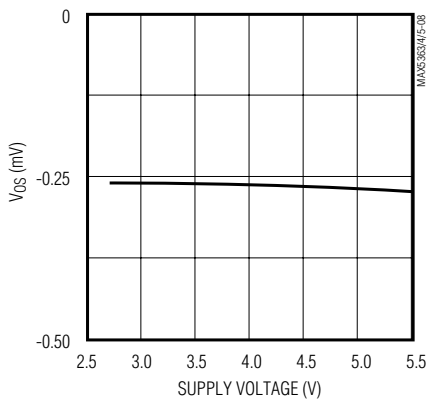
Typical Operating Characteristics (continued)

(V_{DD} = +3.0V (MAX5363), V_{DD} = +5.0V (MAX5364/MAX5365), T_A = +25°C, unless otherwise noted.)

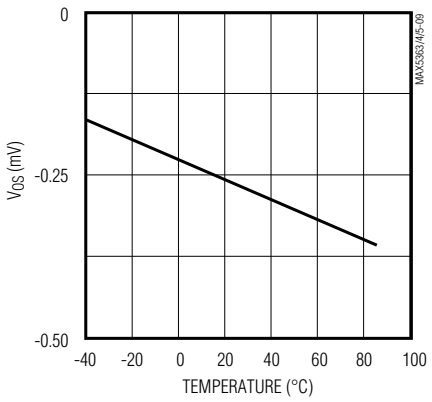
TOTAL UNADJUSTED ERROR vs. CODE



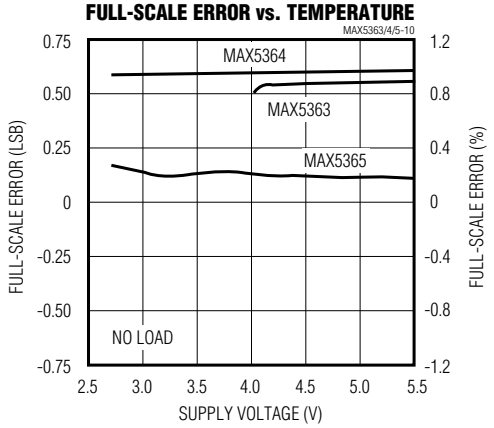
OFFSET ERROR vs. SUPPLY VOLTAGE



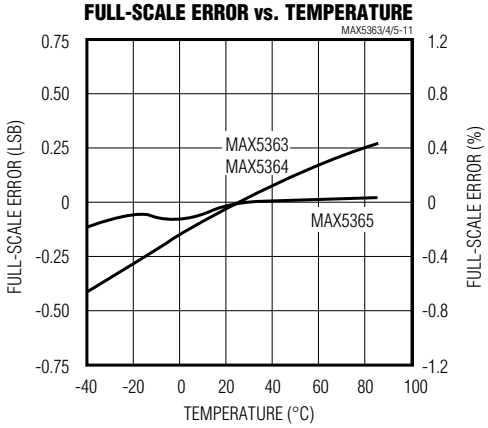
OFFSET ERROR vs. TEMPERATURE



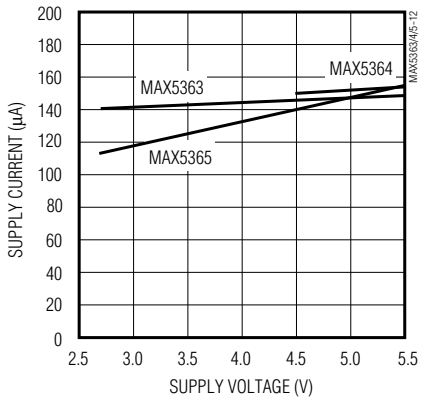
FULL-SCALE ERROR vs. TEMPERATURE



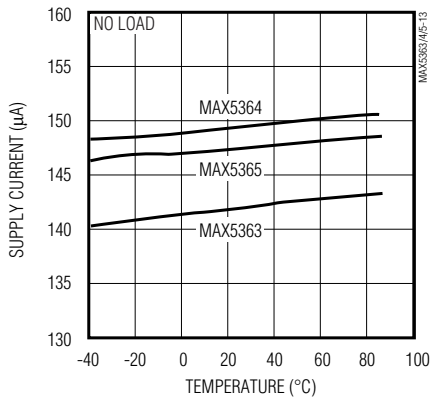
FULL-SCALE ERROR vs. TEMPERATURE



SUPPLY CURRENT vs. SUPPLY VOLTAGE



SUPPLY CURRENT vs. TEMPERATURE

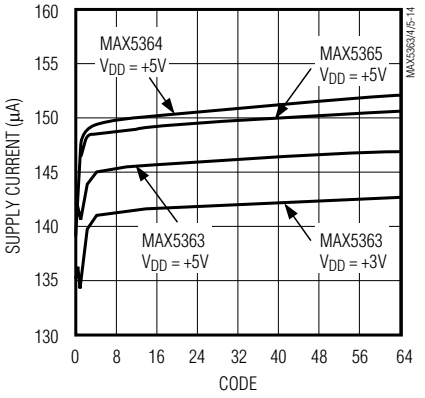


Low-Cost, Low-Power, 6-Bit DACs with 3-Wire Serial Interface in SOT23

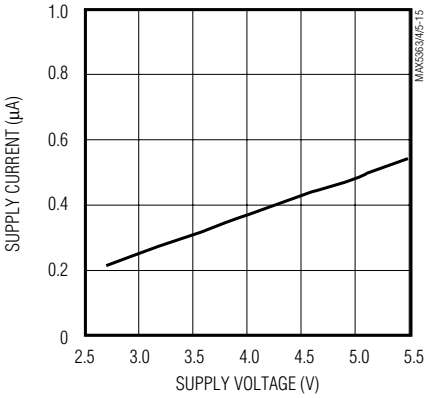
Typical Operating Characteristics (continued)

(V_{DD} = +3.0V (MAX5363), V_{DD} = +5.0V (MAX5364/MAX5365), T_A = +25°C, unless otherwise noted.)

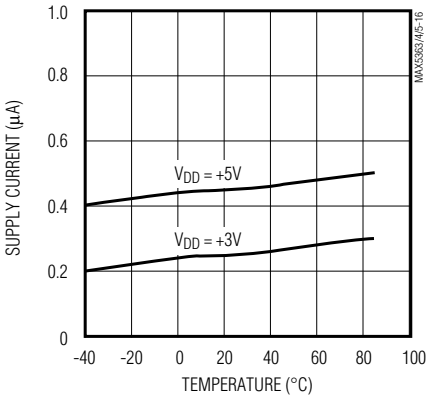
SUPPLY CURRENT vs. CODE



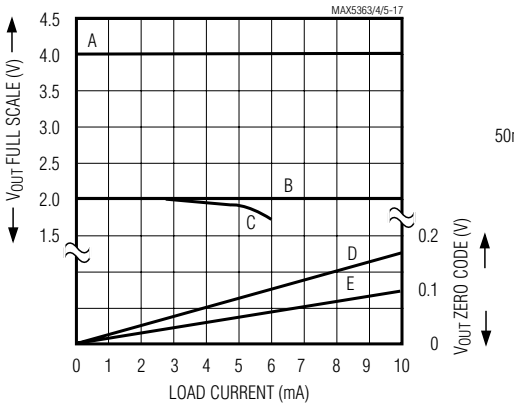
SHUTDOWN SUPPLY CURRENT vs. SUPPLY VOLTAGE



SHUTDOWN SUPPLY CURRENT vs. TEMPERATURE

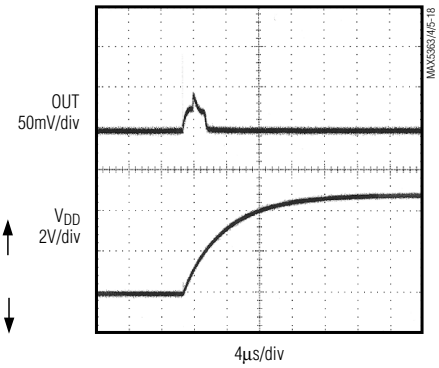


OUTPUT LOAD REGULATION

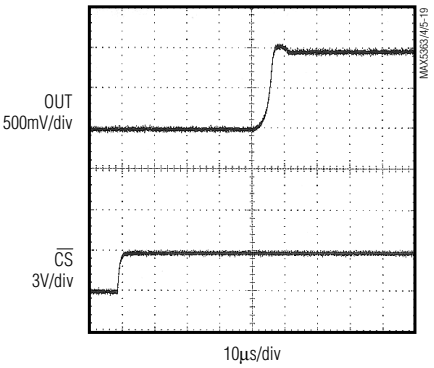


A: MAX5364/MAX5365, V_{DD} = +4.5V, FULL SCALE OR SOURCING
B: MAX5363, FULL SCALE, V_{DD} = +2.7V SINKING, V_{DD} = +5.0V SOURCING
C: MAX5363, FULL SCALE, V_{DD} = +2.7V SOURCING
D: ZERO CODE, V_{DD} = +2.7V SINKING
E: ZERO CODE, V_{DD} = +5.5V SINKING

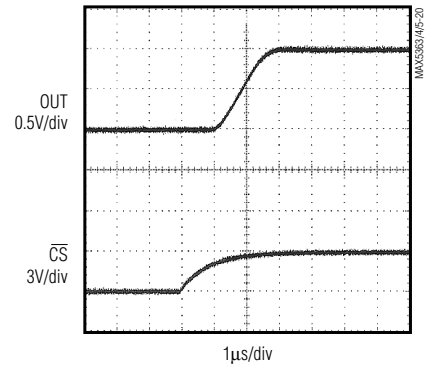
OUTPUT VOLTAGE ON POWER-UP



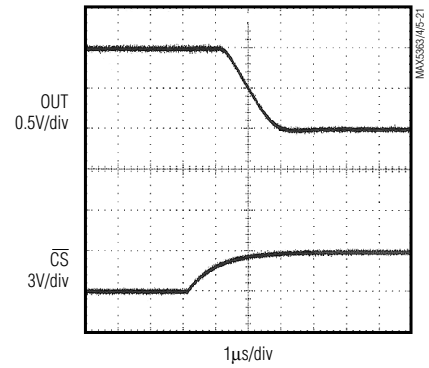
MAX5363 OUTPUT VOLTAGE EXITING SHUTDOWN



MAX5363 OUTPUT SETTLING FROM 1/4FS TO 3/4FS



MAX5363 OUTPUT SETTLING FROM 3/4FS TO 1/4FS

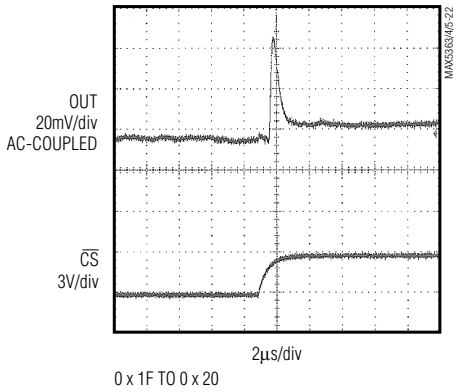


MAXIM

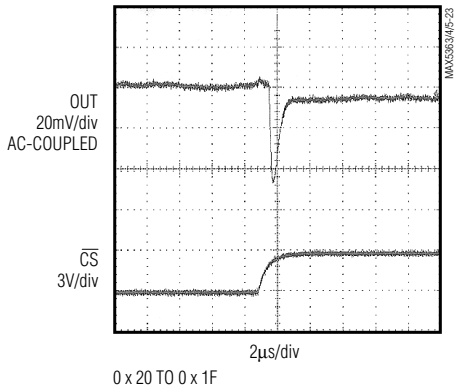
Typical Operating Characteristics (continued)

(V_{DD} = +3.0V (MAX5363), V_{DD} = +5.0V (MAX5364/MAX5365), T_A = +25°C, unless otherwise noted.)

MAX5363
OUTPUT SETTLING
1/4LSB STEP UP



MAX5363
OUTPUT SETTLING
1/4LSB STEP DOWN



Pin Description

PIN	NAME	FUNCTION
1	OUT	DAC Voltage Output
2	GND	Ground
3	V_{DD}	Power-Supply Input
4	DIN	Serial Data Input
5	SCLK	Serial Clock Input
6	$\overline{CS}$	Chip-Select Input

Detailed Description

The MAX5363/MAX5364/MAX5365 voltage-output, 6-bit DACs offer full 6-bit performance with less than 1LSB integral nonlinearity error and less than 1LSB differential nonlinearity error, ensuring monotonic performance. The devices use a simple 3-wire, SPI/QSPI/ MICROWIRE-compatible serial interface that operates up to 10MHz. The MAX5363/MAX5364/MAX5365 include an internal reference, an output buffer, and three low-current shutdown modes, making these devices ideal for low-power, highly integrated applications. Figure 1 shows the devices' functional diagram.

Analog Section

The MAX5363/MAX5364MAX5365 employ a current-steering DAC topology as shown in Figure 2. At the core of the DAC is a reference voltage-to-current converter (V/I) that generates a reference current. This current is mirrored to 63 equally weighted current sources. DAC switches control the outputs of these current mirrors so that only the desired fraction of the total current-mirror currents is steered to the DAC output. The current is then converted to a voltage across a resistor, and this voltage is buffered by the output buffer amplifier.

Output Voltage

Table 1 shows the relationship between the DAC code and the analog output voltage. The 6-bit DAC code is binary unipolar with 1LSB = (V_{REF}/64). The MAX5363/MAX5364 have a full-scale output voltage of (+2V - 1LSB) and (+4V - 1LSB), respectively, set by the internal references. The MAX5365 has a full-scale output voltage of ($0.9 \times V_{DD}$ - 1LSB).

Output Buffer

The DAC voltage output is an internally buffered unity-gain follower that slews up to ±0.4V/µs. The output can swing from 0 to full scale. With a 1/4FS to 3/4FS output transition, the amplifier outputs typically settle to 1/2LSB in less than 5µs when loaded with 10kΩ in parallel with 50pF. The buffer amplifiers are stable with any

Low-Cost, Low-Power, 6-Bit DACs with 3-Wire Serial Interface in SOT23

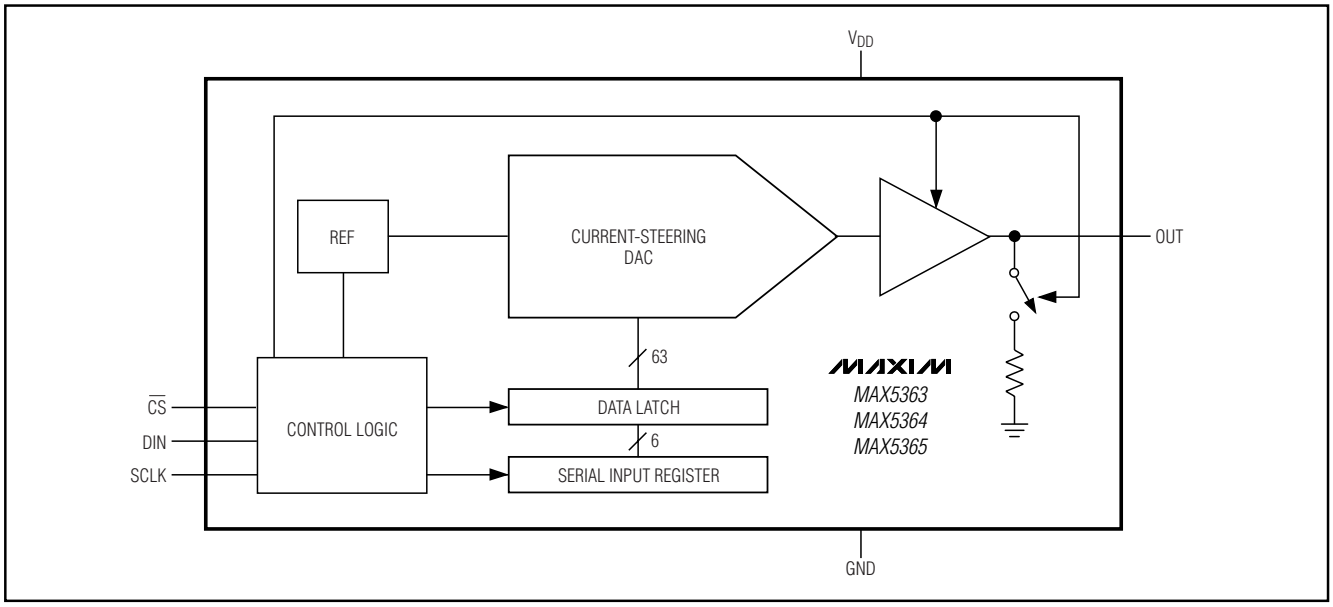


Figure 1. Functional Diagram

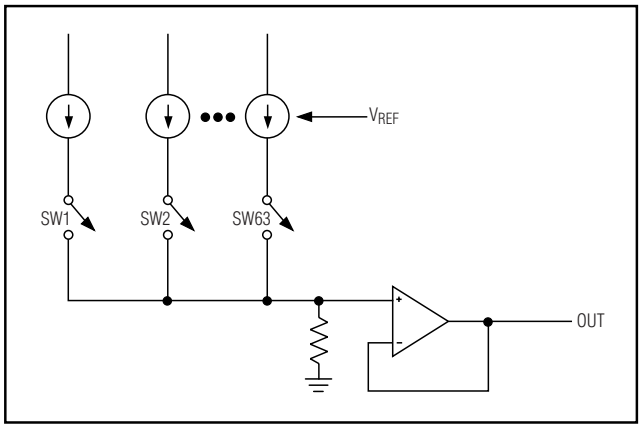


Figure 2. Current-Steering DAC Topology

Table 1. Unipolar Code Output Voltage

DAC CODE [D11–D6]	OUTPUT VOLTAGE		
	MAX5363	MAX5364	MAX5365
111 111	2V × (63/64)	4V × (63/64)	0.9 × V_{DD} × (63/64)
100 000	1V	2V	0.9 × V_{DD} / 2
000 001	31mV	63mV	0.9 × V_{DD} / 64
000 000	0	0	0

combination of resistive loads >10kΩ and capacitive loads <50pF.

Power-On Reset

The MAX5363/MAX5364/MAX5365 have a power-on reset circuit to set the DAC's output to 0 when V_{DD} is first applied or when V_{DD} dips below 1.7V (typ). This ensures that unwanted DAC output voltages will not occur immediately following a system startup, such as after a loss of power. The output glitch on startup is typically less than 50mV.

Shutdown Mode

The MAX5363/MAX5364/MAX5365 include three software-controlled shutdown modes that reduce the supply current to <1µA. All internal circuitry is disabled, and a known impedance is placed from OUT to GND to ensure 0V while in shutdown. Table 2 details the three shutdown modes of operation.

Digital Section

3-Wire Serial Interface

The MAX5363/MAX5364/MAX5365s' digital interface is a standard 3-wire connection compatible with SPI/QSPI/MICROWIRE interfaces. The chip-select input ($\overline{CS}$) frames the serial data loading at the data-input pin (DIN). Immediately following $\overline{CS}$'s high-to-low transition, the data is shifted synchronously and latched into the input register on the rising edge of the serial clock input (SCLK). After 16 bits have been loaded into the serial

input register, it transfers its contents to the DAC latch on $\overline{CS}$'s low-to-high transition (Figure 3). Note that if $\overline{CS}$ is not kept low during the entire 16 SCLK cycles, data will be corrupted. In this case, reload the DAC latch with a new 16-bit word. The serial clock (SCLK) can idle either high or low between transitions. Figure 4 shows the complete 3-wire serial interface transmission. Table 3 lists serial interface mapping.

Applications Information

Device Powered by an External Reference

Since the MAX5365 generates an output voltage proportional to V_{DD}, a noisy power supply will affect the accuracy of the on-board reference, thereby affecting the overall accuracy of the DAC. The circuit in Figure 5 rejects this power-supply noise by powering the device directly with a precision voltage reference, improving overall system accuracy. The MAX6103 (+3V, 75ppm) or the MAX6105 (+5V, 75ppm) precision voltage references are ideal choices due to the low power requirements of the MAX5365. This solution is also useful when the required full-scale output voltage is different from the available supply voltages.

Digital Inputs and Interface Logic

The digital interface for the 6-bit DAC is based on a 3-wire standard that is compatible with SPI, QSPI, and MICROWIRE interfaces. The three digital inputs ($\overline{CS}$, DIN, and SCLK) load the digital input serially into the DAC.

All of the digital inputs include Schmitt-trigger buffers to accept slow-transition interfaces. This means that optocouplers can interface directly to the MAX5363/MAX5364/MAX5365 without additional external logic. The digital inputs are compatible with CMOS logic levels and can be driven with voltages up to +5.5V regardless of the supply voltage.

Power-Supply Bypassing and Layout

Careful PC board layout is important for best system performance. To reduce crosstalk and noise injection, keep analog and digital signals separate. To ensure that the ground return from GND to the supply ground is short and low impedance, a ground plane is recommended. Bypass V_{DD} with a 0.1µF to ground as close as possible to the device. If the supply is excessively noisy, connect a 10Ω resistor in series with the supply and V_{DD} and add additional capacitance.

Table 2. Shutdown Modes

DAC CODE [D13 AND D12]	MODE	OUTPUT RESISTANCE TO GROUND (Ω)	MAXIMUM SUPPLY CURRENT (µA)
01	Shutdown	1k	1
10	Shutdown	100k	1
11	Shutdown	1M	1

Table 3. Serial Interface Mapping

16-BIT SERIAL WORD				ANALOG OUTPUT	FUNCTION
MSB			LSB		
XX00	0000	0000	XXXX	0V	Normal operation
XX00	1111	11XX	XXXX	$V_{REF} \times (63/64)$	Normal operation
XX00	0000	01XX	XXXX	$V_{REF} \times (1/64)$	Normal operation
XX00	1000	00XX	XXXX	$V_{REF} \times (32/64)$	Normal operation
XX01	XXXX	XXXX	XXXX	0V	Shutdown, 1kΩ to GND
XX10	XXXX	XXXX	XXXX	0V	Shutdown, 100kΩ to GND
XX11	XXXX	XXXX	XXXX	0V	Shutdown, 1MΩ to GND

X = *Don't care*

Low-Cost, Low-Power, 6-Bit DACs with 3-Wire Serial Interface in SOT23

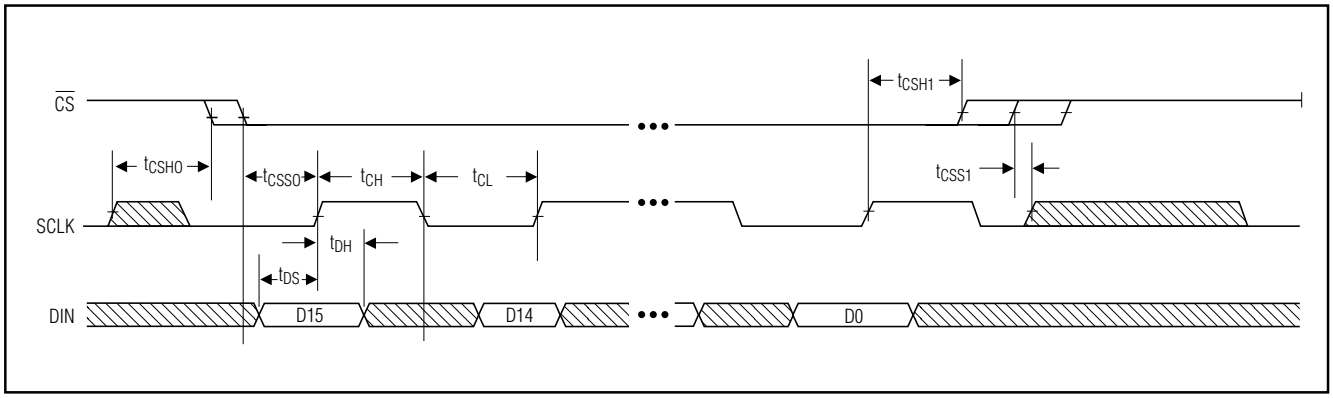


Figure 3. 3-Wire Serial Interface Timing Diagram

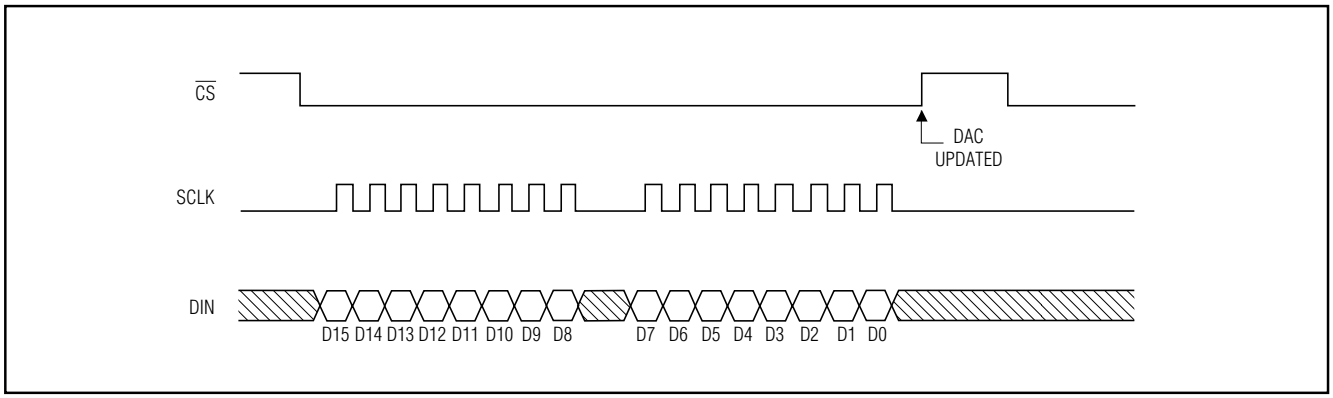


Figure 4. Complete 3-Wire Serial Interface Transmission

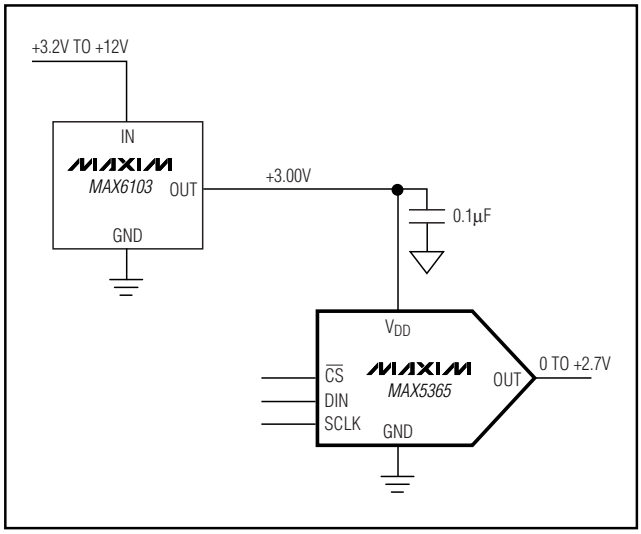


Figure 5. Powering the MAX5365 with a Precision Voltage Reference

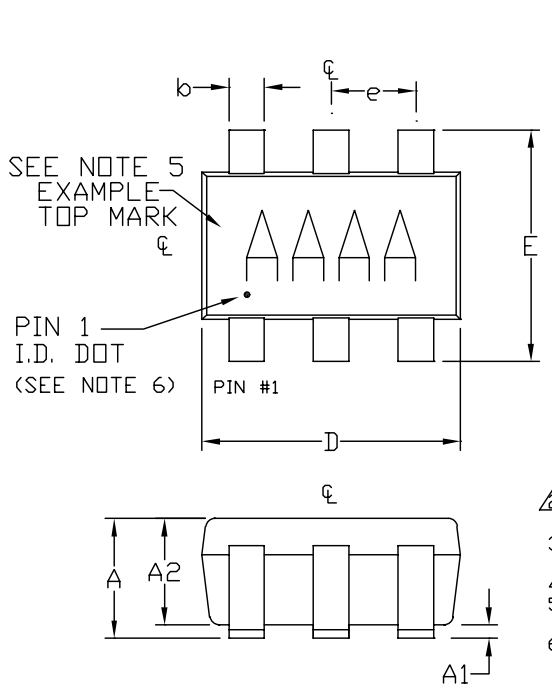
Chip Information

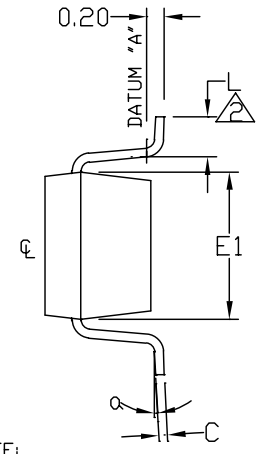
TRANSISTOR COUNT: 2160

Low-Cost, Low-Power, 6-Bit DACs with 3-Wire Serial Interface in SOT23

Package Information

6LSOT.EPS





SYMBOL	MIN	MAX
A	0.90	1.45
A1	0.00	0.15
A2	0.90	1.30
b	0.35	0.50
C	0.08	0.20
D	2.80	3.00
E	2.60	3.00
E1	1.50	1.75
L	0.35	0.55
e	0.95 REF	
α	0°	10°

NOTE:

1. ALL DIMENSIONS ARE IN MILLIMETERS.
2. FOOT LENGTH MEASURED AT INTERCEPT POINT BETWEEN DATUM A & LEAD SURFACE.
3. PACKAGE OUTLINE EXCLUSIVE OF MOLD FLASH & METAL BURR.
4. PACKAGE OUTLINE INCLUSIVE OF SOLDER PLATING.
5. PIN 1 IS LOWER LEFT PIN WHEN READING TOP MARK FROM LEFT TO RIGHT. (SEE EXAMPLE TOP MARK)
6. PIN 1 I.D. DOT IS 0.3 MM ø MIN. LOCATED ABOVE PIN 1.

MAXIM

PROPRIETARY INFORMATION

TITLE:

PACKAGE OUTLINE, SOT23, 6L

APPROVAL	DOCUMENT CONTROL NO.	REV	
	21-0058	D	1/1

NOTES

Mouser Electronics

Authorized Distributor

Click to View Pricing, Inventory, Delivery & Lifecycle Information:

Maxim Integrated:

MAX5363EUT+T MAX5364EUT+T MAX5365EUT+T