17-Output LED Driver/GPO with Intensity Control and Hot-Insertion Protection

ABSOLUTE MAXIMUM RATINGS

Voltage (with respect to GND)
V+ .....-0.3V to +4V
SCL, SDA, AD0, BLINK, $\overline{RST}$ .....-0.3V to +6V
O0–O16 .....-0.3V to +8V
DC Current on O0 to O16 .....55mA
DC Current on SDA.....10mA
Maximum GND Current 350mA

Continuous Power Dissipation (T_A = +70°C)
24-Pin QSOP (derate 9.5mW/°C over +70°C).....761mW
24-Pin QFN (derate 20.8mW/°C over +70°C) 1666mW
Operating Temperature Range .....-40°C to +125°C
Junction Temperature.....+150°C
Storage Temperature Range .....-65°C to +150°C
Lead Temperature (soldering, 10s) .....+300°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

(Typical Operating Circuit, V+ = 2V to 3.6V, T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are at V+ = 3.3V, T_A = +25°C.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
Operating Supply Voltage	V+			2.0		3.6	V
Output Load External Supply Voltage	V_{EXT}			0		7	V
Standby Current (Interface Idle, PWM Disabled)	I_+	SCL and SDA at V+; other digital inputs at V+ or GND; PWM intensity control disabled	T_A = +25°C		1.2	2.3	µA
			T_A = -40°C to +85°C			2.6	
			T_A = T_{MIN} to T_{MAX}			3.3	
Supply Current (Interface Idle, PWM Enabled)	I_+	SCL and SDA at V+; other digital inputs at V+ or GND; PWM intensity control disabled	T_A = +25°C		8.5	15.1	µA
			T_A = -40°C to +85°C			16.5	
			T_A = T_{MIN} to T_{MAX}			17.2	
Supply Current (Interface Running, PWM Disabled)	I_+	f_{SCL} = 400kHz; other digital inputs at V+ or GND; PWM intensity control enabled	T_A = +25°C		50	95.3	µA
			T_A = -40°C to +85°C			99.2	
			T_A = T_{MIN} to T_{MAX}			102.4	
Supply Current (Interface Running, PWM Enabled)	I_+	f_{SCL} = 400kHz; other digital inputs at V+ or GND; PWM intensity control enabled	T_A = +25°C		57	110.2	µA
			T_A = -40°C to +85°C			117.4	
			T_A = T_{MIN} to T_{MAX}			122.1	
Input High Voltage SDA, SCL, AD0, BLINK, $\overline{RST}$	V_{IH}			0.7 x V+			V
Input Low Voltage SDA, SCL, AD0, BLINK, $\overline{RST}$	V_{IL}					0.3 x V+	V
Input Leakage Current SDA, SCL, AD0, BLINK, $\overline{RST}$	I_{IH}, I_{IL}	0 ≤ input voltage ≤ 5.5V		-0.2		+0.2	µA
Input Capacitance SDA, SCL, AD0, BLINK, $\overline{RST}$					8		pF

ELECTRICAL CHARACTERISTICS (continued)

(Typical Operating Circuit, V+ = 2V to 3.6V, $T_A = T_{MIN}$ to T_{MAX}, unless otherwise noted. Typical values are at V+ = 3.3V, T_A= + 25°C.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
Output Low Voltage O0–O16	V_{OL}	V+ = 2V, I_{SINK} = 20mA	T_A = +25°C		0.15	0.26	V
			T_A = -40°C to +85°C			0.3	
			$T_A = T_{MIN}$ to T_{MAX}			0.32	
		V+ = 2.5V, I_{SINK} = 20mA	T_A = +25°C		0.13	0.23	V
			T_A = -40°C to +85°C			0.26	
			$T_A = T_{MIN}$ to T_{MAX}			0.28	
		V+ = 3.3V, I_{SINK} = 20mA	T_A = +25°C		0.12	0.23	V
			T_A = -40°C to +85°C			0.24	
			$T_A = T_{MIN}$ to T_{MAX}			0.26	
Output Low-Voltage SDA	V_{OLSDA}	I_{SINK} = 6mA				0.4	V
PWM Clock Frequency	f_{PWM}				32		kHz

TIMING CHARACTERISTICS

(Typical Operating Circuit, V+ = 2V to 3.6V, $T_A = T_{MIN}$ to T_{MAX}, unless otherwise noted. Typical values are at V+ = 3.3V, T_A = +25°C.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Serial Clock Frequency	f_{SCL}				400	kHz
Bus Free Time Between a STOP and a START Condition	t_{BUF}		1.3			µs
Hold Time, Repeated START Condition	$t_{HD, STA}$		0.6			µs
Repeated START Condition Setup Time	$t_{SU, STA}$		0.6			µs
STOP Condition Setup Time	$t_{SU, STO}$		0.6			µs
Data Hold Time	$t_{HD, DAT}$	(Note 2)			0.9	µs
Data Setup Time	$t_{SU, DAT}$		180			ns
SCL Clock Low Period	t_{LOW}		1.3			µs
SCL Clock High Period	t_{HIGH}		0.7			µs
Rise Time of Both SDA and SCL Signals, Receiving	t_R	(Notes 3, 4)		$20 + 0.1C_b$	300	ns
Fall Time of Both SDA and SCL Signals, Receiving	t_F	(Notes 3, 4)		$20 + 0.1C_b$	300	ns
Fall Time of SDA Transmitting	$t_{F.TX}$	(Notes 3, 5)		$20 + 0.1C_b$	250	ns
Pulse Width of Spike Suppressed	t_{SP}	(Note 6)		50		ns

17-Output LED Driver/GPO with Intensity Control and Hot-Insertion Protection

TIMING CHARACTERISTICS (continued)

(Typical Operating Circuit, V+ = 2V to 3.6V, $T_A = T_{MIN}$ to T_{MAX}, unless otherwise noted. Typical values are at V+ = 3.3V, T_A = +25°C.) (Note 1)

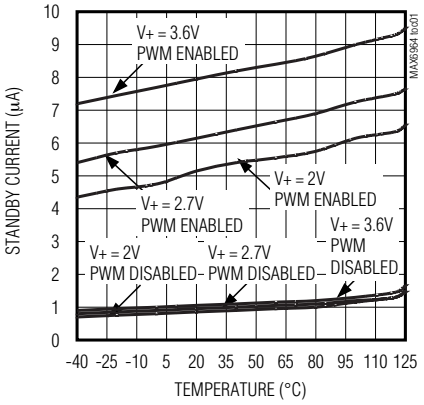
PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Capacitive Load for Each Bus Line	C_b	(Note 3)			400	pF
$\overline{RST}$ Pulse Width	t_W		1			ns
Output Data Valid	t_{DV}	Figure 10			5	ns

Note 1: All parameters tested at T_A = +25°C. Specifications over temperature are guaranteed by design.
Note 2: A master device must provide a hold time of at least 300ns for the SDA signal (referred to V_{IL} of the SCL signal) to bridge the undefined region of SCL's falling edge.
Note 3: Guaranteed by design.
Note 4: C_b = total capacitance of one bus line in pF. t_R and t_F measured between 0.3 x V_{DD} and 0.7 x V_{DD}.
Note 5: $I_{SINK} \le 6mA$. C_b = total capacitance of one bus line in pF. t_R and t_F measured between 0.3 x V_{DD} and 0.7 x V_{DD}.
Note 6: Input filters on the SDA and SCL inputs suppress noise spikes less than 50ns.

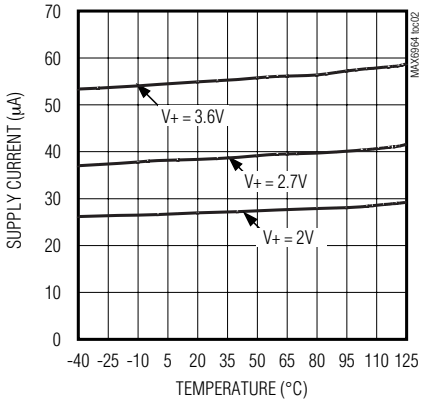
Typical Operating Characteristics

(T_A = +25°C, unless otherwise noted.)

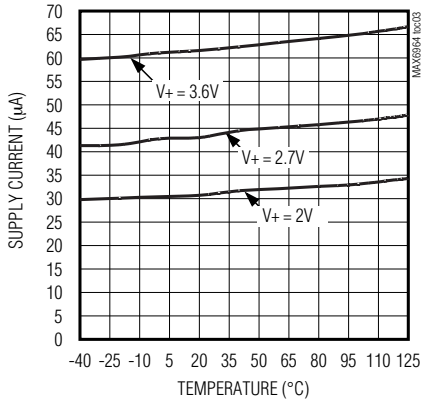
STANDBY CURRENT vs. TEMPERATURE



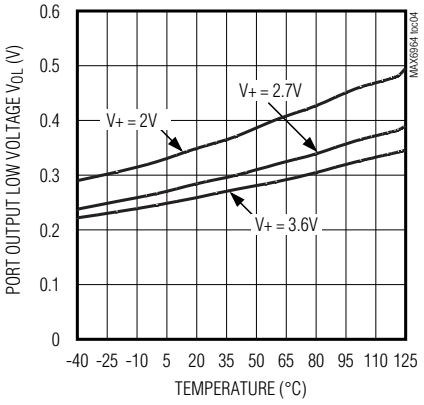
SUPPLY CURRENT vs. TEMPERATURE (PWM DISABLED; f_{SCL} = 400kHz)



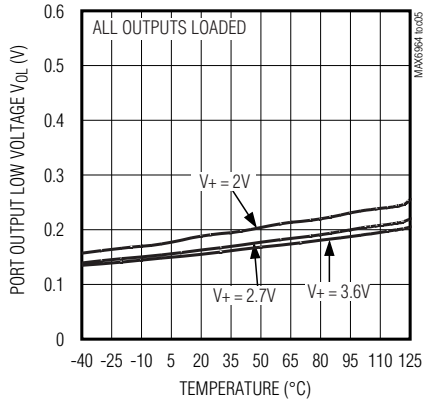
SUPPLY CURRENT vs. TEMPERATURE (PWM ENABLED; f_{SCL} = 400kHz)



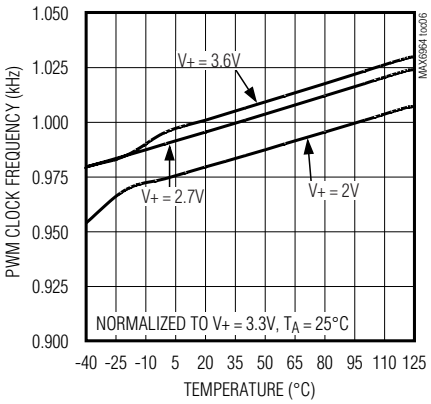
PORT OUTPUT LOW VOLTAGE WITH 50mA LOAD CURRENT vs. TEMPERATURE



PORT OUTPUT LOW VOLTAGE WITH 20mA LOAD CURRENT vs. TEMPERATURE



PWM CLOCK FREQUENCY vs. TEMPERATURE

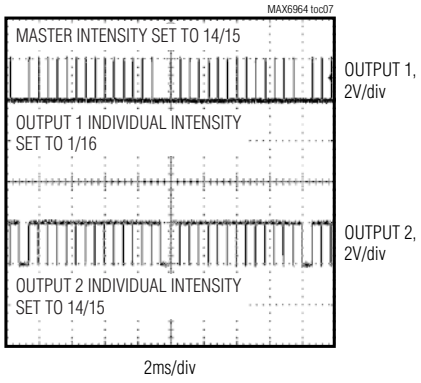


17-Output LED Driver/GPO with Intensity Control and Hot-Insertion Protection

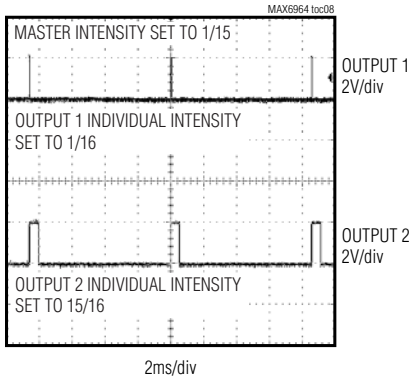
Typical Operating Characteristics (continued)

(T_A = +25°C, unless otherwise noted.)

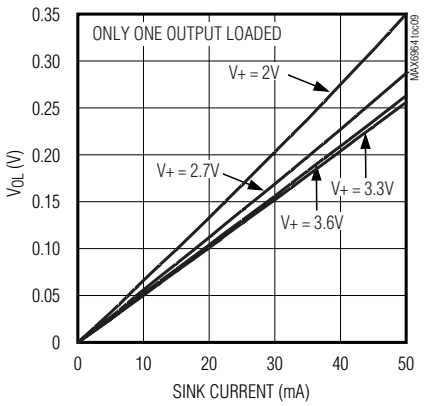
SCOPE SHOT OF OUTPUT PORTS



SCOPE SHOT OF OUTPUT PORTS



SINK CURRENT vs. V_{OL}



Pin Description

PIN		NAME	FUNCTION
QSOP	QFN		
1, 4–11, 13–20	1–8, 10–17, 22	O0-O16	Output Ports. Open-drain outputs rated at 7V, 50mA.
2	23	$\overline{RST}$	Reset Input. Active low clears the 2-wire interface and puts the device in the same condition as power-up reset.
3	24	AD0	Address Input. Sets device slave address. Connect to either GND, V+, SCL, or SDA to give 4 logic combinations. See Table 1.
12	9	GND	Ground. Do not sink more than 350mA into the GND pin.
21	18	BLINK	Input Port. Configurable as blink control or general-purpose input.
22	19	SCL	I²C-Compatible Serial Clock Input
23	20	SDA	I²C-Compatible Serial Data I/O
24	21	V+	Positive Supply Voltage. Bypass V+ to GND with a 0.047µF ceramic capacitor.
—	Pad	Exposed Pad	Exposed pad on package underside. Connect to GND.

17-Output LED Driver/GPO with Intensity Control and Hot-Insertion Protection

Functional Overview

The MAX6964 is a general-purpose output (GPO) peripheral that provides 17 output ports, O0–O16, controlled through an I²C-compatible serial interface. All outputs sink loads up to 50mA connected to external supplies up to 7V, independent of the MAX6964's supply voltage. The MAX6964 is rated for a ground current of 350mA, allowing all 17 outputs to sink 20mA at the same time. Figure 1 shows the output structure of the MAX6964. The outputs default to logic high (high impedance unless external pullup resistors are used) on power-up.

Output Control and LED Blinking

The two blink phase 0 registers set the output logic levels of the 16 outputs O0–O15 (Table 6). These registers control the port outputs if the blink function is disabled. A duplicate pair of registers, the blink phase 1 registers, are also used if the blink function is enabled (Table 7). In blink mode, the outputs can be flipped between using the blink phase 0 registers, and the blink phase 1 registers using hardware control (the BLINK input) and/or software control (the blink flip flag in the configuration register) (Table 4).

The 17th output, O16, is controlled through 2 bits in the configuration register, which provide the same static or blink control as the other 16 outputs (Table 4).

The logic level of the BLINK input may be read back through the blink status bit in the configuration register (Table 4). The BLINK input, therefore, may be used as a general-purpose logic input (GPI port) if the blink function is not required.

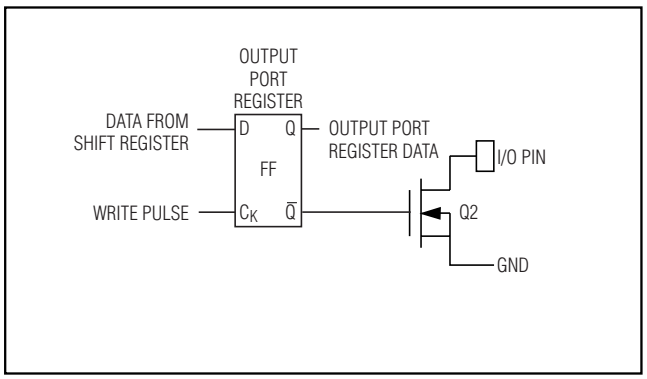


Figure 1. Simplified Schematic of I/O Ports

PWM Intensity Control

The MAX6964 includes an internal oscillator, nominally 32kHz, to generate PWM timing for LED intensity control. PWM intensity control can be enabled on an output-by-output basis, allowing the MAX6964 to provide any mix of PWM LED drives and glitch-free logic outputs (Table 8). PWM can be disabled entirely, in which case all outputs are static and the MAX6964 operating current is lowest because the internal oscillator is turned off.

PWM intensity control uses a 4-bit master control and 4 bits of individual control per output (Tables 11 and 12). The 4-bit master control provides 16 levels of overall intensity control, which applies to all PWM-enabled outputs. The master control sets the maximum pulse width from 1/15 to 15/15 of the PWM time period. The individual settings comprise a 4-bit number, further reducing the duty cycle to be from 1/16 to 15/16 of the time window set by the master control.

For applications requiring the same PWM setting for all output ports, a single global PWM control can be used instead of all the individual controls to simplify the control software and provide 240 steps of intensity control (Tables 8 and 11).

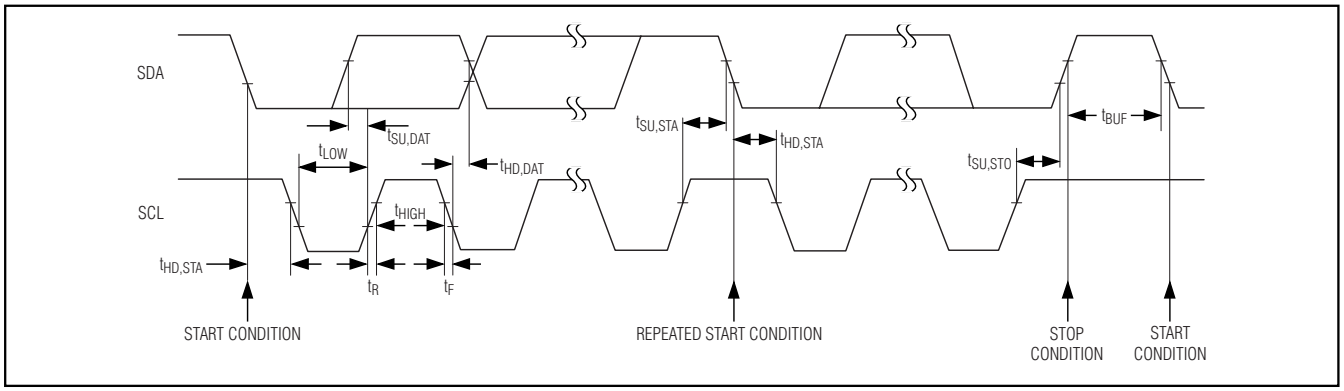


Figure 2. 2-Wire Serial Interface Timing Details

User RAM

The MAX6964 includes 2 register bytes, which are available as general-user RAM (Table 2). These bytes are reset to the value 0xFF on power-up and when the $\overline{RST}$ input is taken low (Table 3).

Standby Mode

When the serial interface is idle and the PWM intensity control is unused, the MAX6964 automatically enters standby mode. If the PWM intensity control is used, the operating current is slightly higher because the internal PWM oscillator is running. When the serial interface is active, the operating current also increases because the MAX6964, like all I²C slaves, has to monitor every transmission.

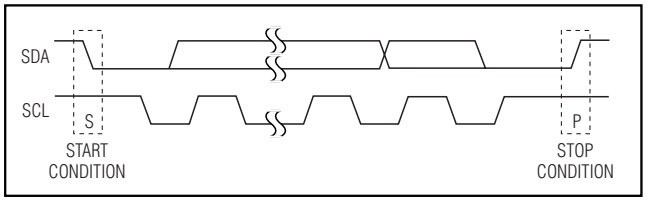


Figure 3. Start and Stop Conditions

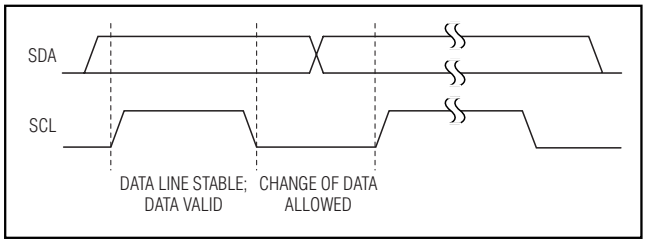


Figure 4. Bit Transfer

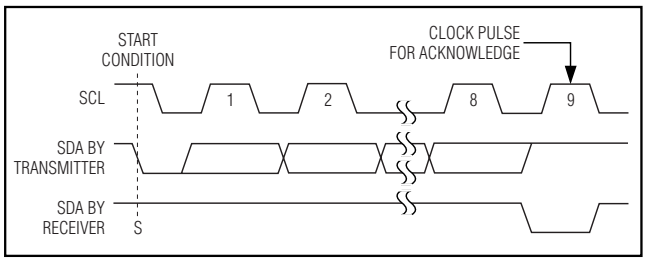


Figure 5. Acknowledge

Serial Interface

Serial Addressing

The MAX6964 operates as a slave that sends and receives data through an I²C-compatible 2-wire interface. The interface uses a serial data line (SDA) and a serial clock line (SCL) to achieve bidirectional communication between master(s) and slave(s). A master (typically a microcontroller) initiates all data transfers to and from the MAX6964 and generates the SCL clock that synchronizes the data transfer (Figure 2).

The MAX6964 SDA line operates as both an input and an open-drain output. A pullup resistor, typically 4.7kΩ, is required on SDA. The MAX6964 SCL line operates only as an input. A pullup resistor, typically 4.7kΩ, is required on SCL if there are multiple masters on the 2-wire interface, or if the master in a single-master system has an open-drain SCL output.

Each transmission consists of a START condition (Figure 3) sent by a master, followed by the MAX6964 7-bit slave address plus R/$\overline{W}$ bit, a register address byte, 1 or more data bytes, and finally a STOP condition (Figure 3).

Start and Stop Conditions

Both SCL and SDA remain high when the interface is not busy. A master signals the beginning of a transmission with a START (S) condition by transitioning SDA from high to low while SCL is high. When the master has finished communicating with the slave, it issues a STOP (P) condition by transitioning SDA from low to high while SCL is high. The bus is then free for another transmission (Figure 3).

Bit Transfer

One data bit is transferred during each clock pulse. The data on SDA must remain stable while SCL is high (Figure 4).

Acknowledge

The acknowledge bit is a clocked 9th bit that the recipient uses to handshake receipt of each byte of data (Figure 5). Thus, each byte transferred effectively requires 9 bits. The master generates the 9th clock pulse, and the recipient pulls down SDA during the acknowledge clock pulse so the SDA line is stable low

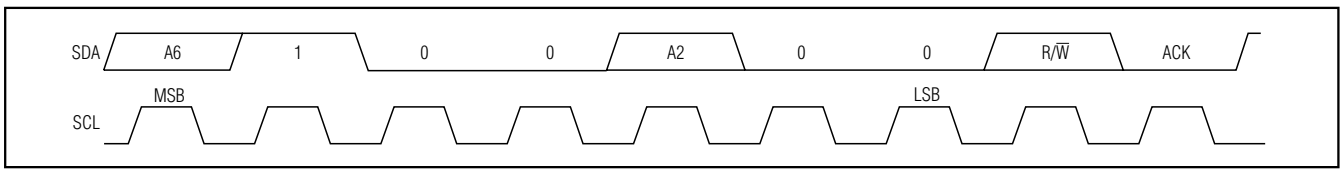


Figure 6. Slave Address

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Table 1. MAX6964 Address Map

PIN AD0	DEVICE ADDRESS						
	A6	A5	A4	A3	A2	A1	A0
SCL	1	1	0	0	0	0	0
SDA	1	1	0	0	1	0	0
GND	0	1	0	0	0	0	0
V+	0	1	0	0	1	0	0

Table 2. Register Address Map

REGISTER	ADDRESS CODE (hex)	AUTOINCREMENT ADDRESS
Blink phase 0 outputs O7–O0	0x02	0x03
Blink phase 0 outputs O15–O8	0x03	0x02
User RAM0	0x06	0x07
User RAM1	0x07	0x06
Blink phase 1 outputs O7–O0	0x0A	0x0B
Blink phase 1 outputs O15–O8	0x0B	0x0A
Master and global/O16 intensity	0x0E	—
Configuration	0x0F	—
Outputs intensity O1, O0	0x10	0x11
Outputs intensity O3, O2	0x11	0x12
Outputs intensity O5, O4	0x12	0x13
Outputs intensity O7, O6	0x13	0x14
Outputs intensity O9, O8	0x14	0x15
Outputs intensity O11, O10	0x15	0x16
Outputs intensity O13, O12	0x16	0x17
Outputs intensity O15, O14	0x17	0x10

during the high period of the clock pulse. When the master is transmitting to the MAX6964, the device generates the acknowledge bit because the MAX6964 is the recipient. When the MAX6964 is transmitting to the master, the master generates the acknowledge bit because the master is the recipient.

Slave Address

The MAX6964 has a 7-bit long slave address (Figure 6). The eighth bit following the 7-bit slave address is the R/$\overline{W}$ bit. The R/$\overline{W}$ bit is low for a write command, high for a read command.

The second (A5), third (A4), fourth (A3), sixth (A1), and last (A0) bits of the MAX6964 slave address are always 1, 0, 0, 0, and 0. Slave address bits A6 and A2 are selected by the address input AD0. AD0 can be connected to GND, V+, SDA, or SCL. The MAX6964 has four possible slave addresses (Table 1), and therefore a maximum of four MAX6964 devices can be controlled independently from the same interface.

Message Format for Writing the MAX6964

A write to the MAX6964 comprises the transmission of the MAX6964's slave address with the R/$\overline{W}$ bit set to zero, followed by at least 1 byte of information. The first byte of information is the command byte. The command byte determines which register of the MAX6964 is to be written to by the next byte, if received (Table 2). If a STOP condition is detected after the command byte is received, then the MAX6964 takes no further action beyond storing the command byte.

Any bytes received after the command byte are data bytes. The first data byte goes into the internal register of the MAX6964 selected by the command byte (Figure 8).

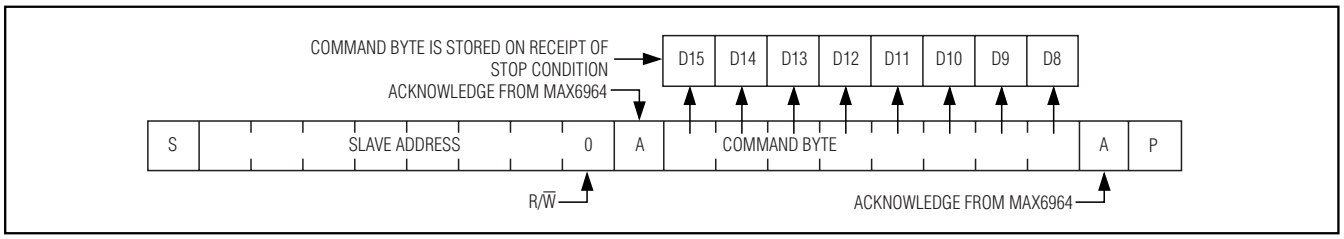

Figure 7. Command Byte Received

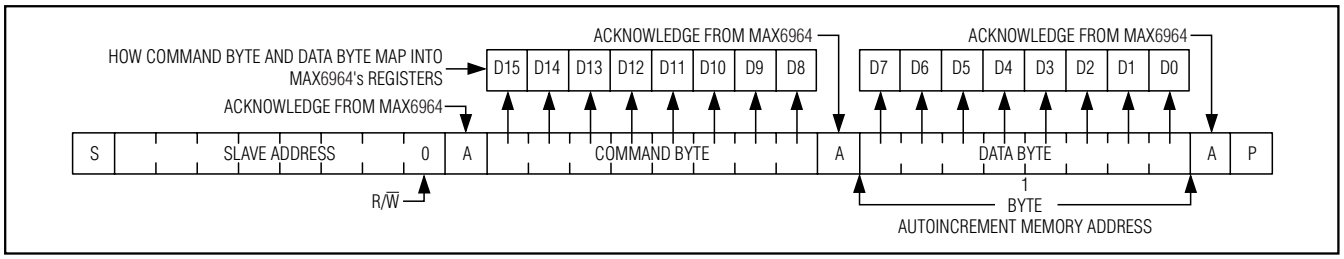

Figure 8. Command and Single Data Byte Received

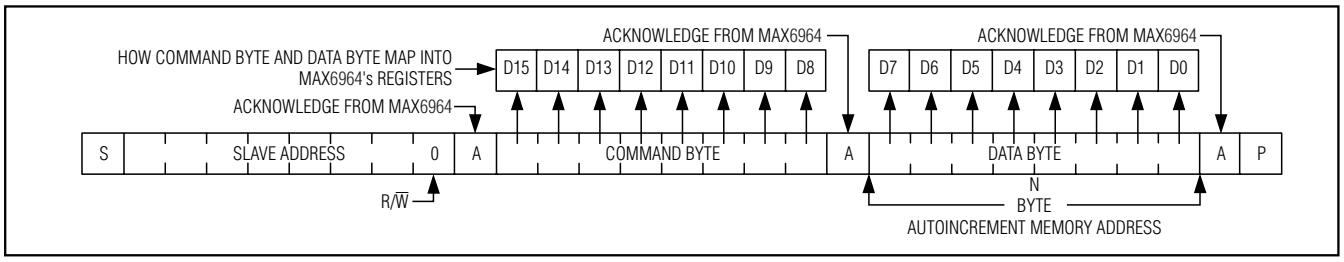

Figure 9. n Data Bytes Received

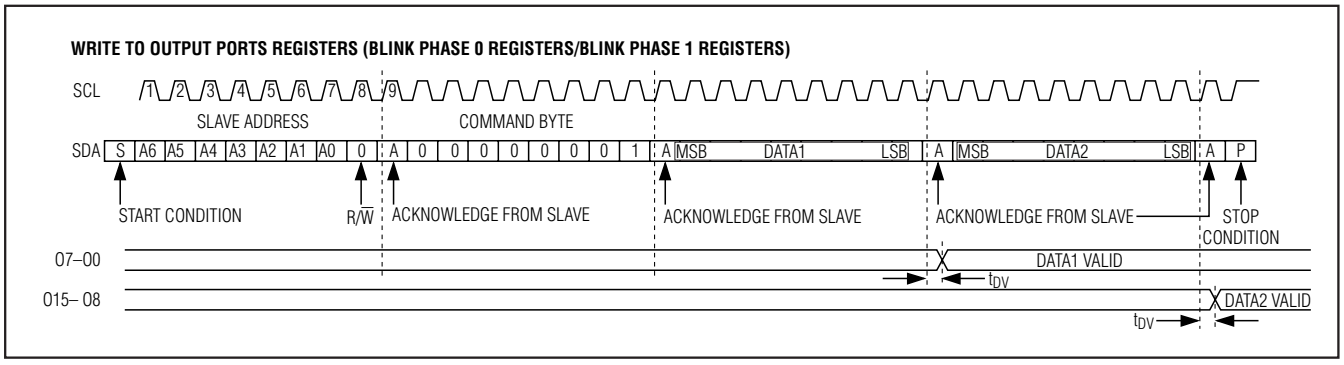

Figure 10. Write Timing Diagram

If multiple data bytes are transmitted before a STOP condition is detected, these bytes are generally stored in subsequent MAX6964 internal registers because the command byte address autoincrements (Table 2). A diagram of a write to the output ports registers (blink phase 0 registers or blink phase 1 registers) is given in Figure 10.

Message Format for Reading

The MAX6964 is read using the MAX6964's internally stored command byte as an address pointer the same way the stored command byte is used as an address pointer for a write. The pointer autoincrements after each data byte is read using the same rules as for a write (Table 2). Thus, a read is initiated by first configur-

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ing the MAX6964's command byte by performing a write (Figure 7). The master can now read n consecutive bytes from the MAX6964 with the first data byte being read from the register addressed by the initialized command byte. When performing read-after-write verification, remember to reset the command byte's address because the stored command byte address has been autoincremented after the write (Table 2).

Operation with Multiple Masters

If the MAX6964 is operated on a 2-wire interface with multiple masters, a master reading the MAX6964 should use a repeated start between the write, which sets the MAX6964's address pointer, and the read(s) that takes the data from the location(s) (Table 2). This is because it is possible for master 2 to take over the bus after master 1 has set up the MAX6964's address pointer but before master 1 has read the data. If master 2 subsequently changes the MAX6964's address pointer, then master 1's delayed read can be from an unexpected location.

Command Address Autoincrementing

The command address stored in the MAX6964 circulates around grouped register functions after each data byte is written or read (Table 2).

Device Reset

The reset input $\overline{RST}$ is an active-low input. When taken low, $\overline{RST}$ clears any transaction to or from the MAX6964 on the serial interface and configures the internal registers to the same state as a power-up reset (Table 3). The MAX6964 then waits for a START condition on the serial interface.

Detailed Description

Initial Power-Up

On power-up, and whenever the $\overline{RST}$ input is pulled low, all control registers are reset and the MAX6964 enters standby mode (Table 3). Power-up status makes all outputs logic high (high impedance if external pullup resistors are not fitted) and disables both the PWM oscillator and blink functionality. The $\overline{RST}$ input can be used as a hardware shutdown input, which effectively turns off any LED (or other) loads and puts the device into its lowest power condition.

Configuration Register

The configuration register is used to configure the PWM intensity mode and blink behavior, operate the O16 output, and read back the BLINK input logic level (Table 4).

Blink Mode

In blink mode, the outputs can be flipped between using either the blink phase 0 registers or the blink phase 1 registers. Flip control is both hardware (the BLINK input) and software control (the blink flip flag B in the configuration register) (Table 4).

The blink function can be used for LED effects by programming different display patterns in the two sets of output port registers, and using the software or hardware controls to flip between the patterns.

If the blink phase 1 registers are written with 0xFF, then the BLINK input can be used as a hardware disable to, for example, instantly turn off an LED pattern programmed into the blink phase 0 registers. This technique can be further extended by driving the BLINK input with a PWM signal to modulate the LED current to provide fading effects.

The blink mode is enabled by setting the blink enable flag E in the configuration register (Table 4). When blink mode is enabled, the state of the blink flip flag and BLINK input are EXORed to set the phase, and the outputs are set by either the blink phase 0 registers or the blink phase 1 registers (Figure 11, Table 5).

The blink mode is disabled by clearing the blink enable flag E in the configuration register (Table 4). When blink mode is disabled, the state of the blink flip flag is ignored, and the blink phase 0 registers alone control the outputs.

The logic status of BLINK is made available as the read-only blink status flag blink in the configuration register (Table 4). This flag allows BLINK to be used as an extra general-purpose input (GPI) in applications not using the blink function. When BLINK is going to be used as a GPI, blink mode should be disabled by clearing the blink enable flag E in the configuration register (Table 4).

Blink Phase Registers

When the blink function is disabled, the two blink phase 0 registers set the logic levels of the 16 outputs (O0 through O15) (Table 6). A duplicate pair of registers called the blink phase 1 registers are also used if the blink function is enabled (Table 7). A logic high sets the appropriate output high impedance, while a logic low makes the port go low.

Reading a blink phase register reads the value stored in the register, not the actual port condition. The port output itself may or may not be at a valid logic level, depending on the external load connected.

The 17th output, O16, is controlled through 2 bits in the configuration register, which provide the same static or blink control as the other 16 output ports.

Table 3. Power-Up Configuration

REGISTER FUNCTION	POWER-UP CONDITION	ADDRESS CODE (hex)	REGISTER DATA							
			D7	D6	D5	D4	D3	D2	D1	D0
Blink phase 0 outputs O7–O0	High-impedance outputs	0x02	1	1	1	1	1	1	1	1
Blink phase 0 outputs O15–O8	High-impedance outputs	0x03	1	1	1	1	1	1	1	1
User RAM0	0xFF	0x06	1	1	1	1	1	1	1	1
User RAM1	0xFF	0x07	1	1	1	1	1	1	1	1
Blink phase 1 outputs O7–O0	High-impedance outputs	0x0A	1	1	1	1	1	1	1	1
Blink phase 1 outputs O15–O8	High-impedance outputs	0x0B	1	1	1	1	1	1	1	1
Master and global/O16 intensity	PWM oscillator is disabled; O16 is static logic output	0x0E	0	0	0	0	1	1	1	1
Configuration	O16 is high-impedance output; blink is disabled; global intensity is enabled	0x0F	0	0	1	1	0	1	0	0
Outputs intensity O1, O0	O1, O0 are static logic outputs	0x10	1	1	1	1	1	1	1	1
Outputs intensity O3, O2	O3, O2 are static logic outputs	0x11	1	1	1	1	1	1	1	1
Outputs intensity O5, O4	O5, O4 are static logic outputs	0x12	1	1	1	1	1	1	1	1
Outputs intensity O7, O6	O7, O6 are static logic outputs	0x13	1	1	1	1	1	1	1	1
Outputs intensity O9, O8	O9, O8 are static logic outputs	0x14	1	1	1	1	1	1	1	1
Outputs intensity O11, O10	O11, O10 are static logic outputs	0x15	1	1	1	1	1	1	1	1
Outputs intensity O13, O12	O13, O12 are static logic outputs	0x16	1	1	1	1	1	1	1	1
Outputs intensity O15, O14	O15, O14 are static logic outputs	0x17	1	1	1	1	1	1	1	1

Table 4. Configuration Register

REGISTER		ADDRESS CODE (hex)	REGISTER DATA							
			D7	D6	D5	D4	D3	D2	D1	D0
CONFIGURATION	**R/$\overline{W}$**		**0**	**BLINK STATUS**	**OUTPUT O16**		**0**	**GLOBAL INTENSITY**	**BLINK FLIP**	**BLINK ENABLE**
Write device configuration	0	0x0F	X	BLINK	**O1**	**O0**	X	**G**	**B**	**E**
Read back device configuration	1		0				0			
Disable blink	—		X	X	X	X	X	X	X	**0**
Enable blink	—		X	X	X	X	X	X	X	**1**
Flip blink register (see text)	—		X	X	X	X	X	X	**0**	**1**
	—		X	X	X	X	X	X	**1**	**1**

X = Don't care.

17-Output LED Driver/GPO with Intensity Control and Hot-Insertion Protection

Table 4. Configuration Register (continued)

REGISTER		ADDRESS CODE (hex)	REGISTER DATA							
			D7	D6	D5	D4	D3	D2	D1	D0
CONFIGURATION	R/$\overline{W}$		0	BLINK STATUS	OUTPUT O16		0	GLOBAL INTENSITY	BLINK FLIP	BLINK ENABLE
Write device configuration	0	0x0F	X	BLINK	**O1**	**O0**	X	**G**	**B**	**E**
Read back device configuration	1		0				0			
Disable global intensity control—intensity is set by registers 0x10–0x17 for ports O0 through O15 when configured as outputs, and by D3–D0 of register 0x0E for output	—		X	X	X	X	X	**0**	X	X
Enable global intensity control—intensity for all ports configured as outputs is set by D3–D0 of register 0x0E	—		X	X	X	X	X	**1**	X	X
O16 output is low (blink is disabled)	—		X	X	X	**0**	**0**	X	X	**0**
O16 output is high impedance (blink is disabled)	—		X	X	X	**1**	**0**	X	X	**0**
O16 output is low during blink phase 0	—		X	X	X	**0**	**0**	X	X	**1**
O16 output is high impedance during blink phase 0	—		X	X	X	**1**	**0**	X	X	**1**
O16 output is low during blink phase 1	—		X	X	**0**	X	**0**	X	X	**1**
O16 output is high impedance during blink phase 1	—		X	X	**1**	X	**0**	X	X	**1**
Read back BLINK input pin status; input is low	1		X	**0**	X	X	X	X	X	X
Read back BLINK input pin status; input is high	1		X	**1**	X	X	X	X	X	X

X = Don't care.

Table 5. Blink Controls

BLINK ENABLE FLAG E	BLINK FLIP FLAG B	BLINK INPUT PIN	BLINK FLIP FLAG EXOR BLINK INPUT PIN	BLINK FUNCTION	OUTPUT REGISTERS USED
0	X	X	X	Disabled	Blink phase 0
1	0	0	0	Enabled	Blink phase 0
	0	1	1		Blink phase 1
	1	0	1		Blink phase 1
	1	1	0		Blink phase 0

X = Don't care.

Table 6. Blink Phase 0 Registers

REGISTER	R/$\overline{W}$	ADDRESS CODE (hex)	REGISTER DATA							
			D7	D6	D5	D4	D3	D2	D1	D0
Write outputs O7–O0 phase 0	0	0x02	OP7	OP6	OP5	OP4	OP3	OP2	OP1	OP0
Read back outputs O7–O0 phase 0	1									
Write outputs O15–O8 phase 0	0	0x03	OP15	OP14	OP13	OP12	OP11	OP10	OP9	OP8
Read back outputs O15–O8 phase 0	1									

Table 7. Blink Phase 1 Registers

REGISTER	R/$\overline{W}$	ADDRESS CODE (hex)	REGISTER DATA							
			D7	D6	D5	D4	D3	D2	D1	D0
Write outputs O7–O0 phase 1	0	0x0A	OP7	OP6	OP5	OP4	OP3	OP2	OP1	OP0
Read back outputs O7–O0 phase 1	1									
Write outputs O15–O8 phase 1	0	0x0B	OP15	OP14	OP13	OP12	OP11	OP10	OP9	OP8
Read back outputs O15–O8 phase 1	1									

Table 8. PWM Application Scenarios

APPLICATION	RECOMMENDED CONFIGURATION
All outputs static without PWM	Set the master and global intensity register 0x0E to any value from 0x00 to 0x0F. The global intensity G bit in the configuration register is don't care. The output intensity registers 0x10 through 0x17 are don't care.
A mix of static and PWM outputs, with PWM outputs using different PWM settings	Set the master and global intensity register 0x0E to any value from 0x10 to 0xFF. Clear global intensity G bit to zero in the configuration register to disable global intensity control. For the static outputs, set the output intensity value to 0xF. For the PWM outputs, set the output intensity value in the range 0x0 to 0xE.
A mix of static and PWM outputs, with PWM outputs all using the same PWM setting	As above. Global intensity control cannot be used with a mix of static and PWM outputs, so write the individual intensity registers with the same PWM value.
All outputs PWM using the same PWM setting	Set the master and global intensity register 0x0E to any value from 0x10 to 0xFF. Set global intensity G bit to 1 in the configuration register to enable global intensity control. The master and global intensity register 0x0E is the only intensity register used. The output intensity registers 0x10 through 0x17 are don't care.

17-Output LED Driver/GPO with Intensity Control and Hot-Insertion Protection

PWM Intensity Control

The MAX6964 includes an internal oscillator, nominally 32kHz, to generate PWM timing for LED intensity control or other applications such as PWM trim DACs. PWM can be disabled entirely for all the outputs. In this case, all outputs are static and the MAX6964 operating current is lowest because the internal PWM oscillator is turned off.

The MAX6964 can be configured to provide any combination of PWM outputs and glitch-free logic outputs. Each PWM output has an individual 4-bit intensity control (Table 12). When all outputs are to be used with the same PWM setting, the outputs can be controlled together instead using the global intensity control (Table 11). Table 8 shows how to set up the MAX6964 to suit a particular application.

PWM Timing

The PWM control uses a 240-step PWM period, divided into 15 master intensity timeslots. Each master intensity timeslot is divided further into 16 PWM cycles (Figure 12).

The master intensity operates as a gate, allowing the individual output settings to be enabled from 1 to 15 timeslots per PWM period (Figures 13, 14, and 15) (Table 11).

Each output's individual 4-bit intensity control only operates during the number of timeslots gated by the master intensity. The individual controls provide 16 intensity settings from 1/16 through 16/16 (Table 12).

Figures 16, 17, and 18 show examples of individual intensity control settings. The highest value an individual or global setting can be set to is 16/16. This setting forces the output to ignore the master control, and follow the logic level set by the appropriate blink phase register bit. The output becomes a glitch-free static output with no PWM.

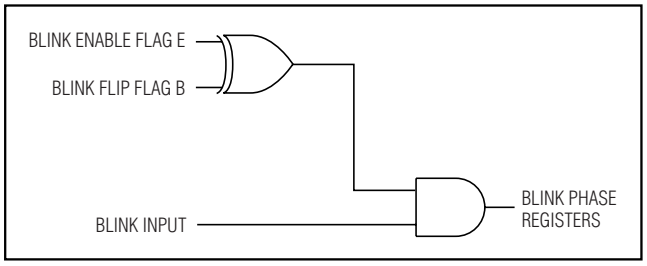


Figure 11. BLINK Logic

Using PWM Intensity Controls with Blink Disabled

When blink is disabled (Table 5), the blink phase 0 registers specify each output's logic level during the PWM on-time (Table 6). The effect of setting an output's blink phase 0 register bit to zero or 1 is shown in Table 9. With its output bit set to zero, an LED can be controlled with 16 intensity settings from 1/16th duty through fully on, but cannot be turned fully off using the PWM intensity control. With its output bit set to 1, an LED can be controlled with 16 intensity settings from fully off through 15/16th duty.

Using PWM Intensity Controls with Blink Enabled

When blink is enabled (Table 5), the blink phase 0 registers and blink phase 1 registers specify each output's logic level during the PWM on-time during the respective blink phases (Tables 6 and 7). The effect of setting an output's blink phase x register bit to 0 or 1 is shown in Table 10. LEDs can be flipped between either directly on and off, or between a variety of high/low PWM intensities.

Global/O16 Intensity Control

The 4 bits used for output O16's PWM individual intensity setting also double as the global intensity control (Table 11). Global intensity simplifies the PWM settings when the application requires them all to be the same, such as for backlight applications, by replacing the 17 individual settings with one setting. Global intensity is

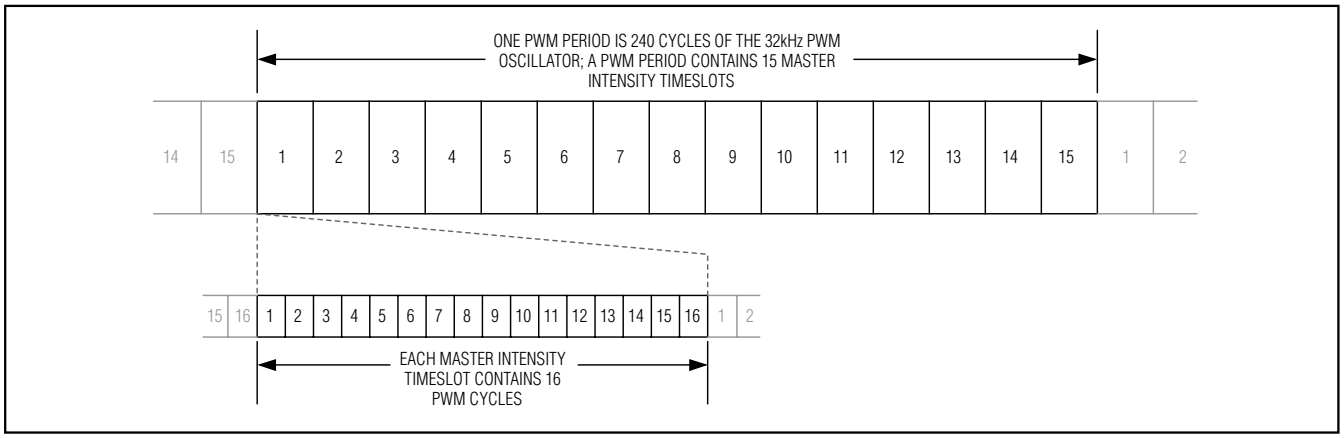


Figure 12. PWM Timing

enabled with the global intensity flag G in the configuration register (Table 4). When global PWM control is used, the 4 bits of master intensity and 4 bits of global intensity effectively combine to provide an 8-bit, 240-step intensity control applying to all outputs.

It is not possible to apply global PWM control to a subset of the ports, and use the others as logic outputs. To mix static logic outputs and PWM outputs, individual PWM control must be selected (Table 8).

Applications Information

Hot Insertion

The $\overline{RST}$ input, BLINK input, and serial interface SDA, SCL, AD0 remain high impedance with up to 6V asserted on them when the MAX6964 is powered down (V+ = 0V). Ouptut ports O0–O16 remain high impedance with up to 8V asserted on them. The MAX6964 can therefore be used in hot-swap applications.

Output Level Translation

The open-drain output architecture allows the ports to level translate the outputs to higher or lower voltages than the MAX6964 supply. An external pullup resistor can be used on any output to convert the high-impedance logic-high condition to a positive voltage level. The resistor can be connected to any voltage up to 7V. For interfacing CMOS inputs, a pullup resistor value of 220kΩ is a good starting point. Use a lower resistance to improve noise immunity, in applications where power consumption is less critical, or where a faster rise time is needed for a given capacitive load.

Driving LED Loads

When driving LEDs, a resistor in series with the LED must be used to limit the LED current to no more than 50mA. Choose the resistor value according to the following formula:

$$R_{LED} = (V_{SUPPLY} - V_{LED} - V_{OL}) / I_{LED}$$

where:

R_{LED} is the resistance of the resistor in series with the LED (Ω).
V_{SUPPLY} is the supply voltage used to drive the LED (V).
V_{LED} is the forward voltage of the LED (V).
V_{OL} is the output low voltage of the MAX6964 when sinking I_{LED} (V).
I_{LED} is the desired operating current of the LED (A).

Figure 13. Master Set to 1/15

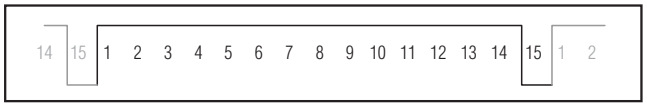


Figure 14. Master Set to 14/15

Figure 15. Master Set to 15/15

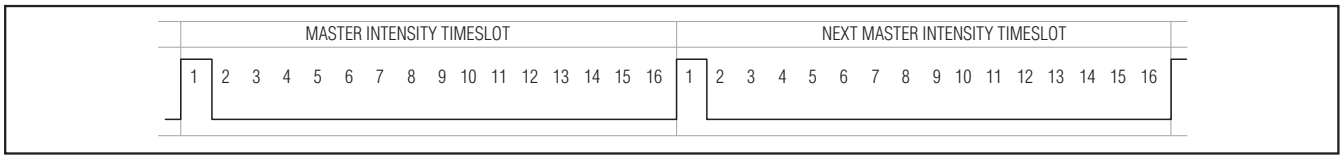


Figure 16. Individual (or Global) Set to 1/16

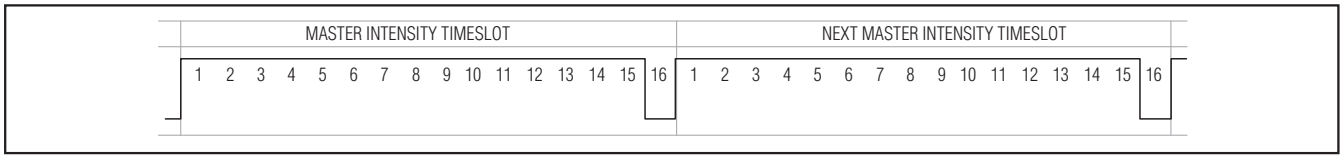


Figure 17. Individual (or Global) Set to 15/16

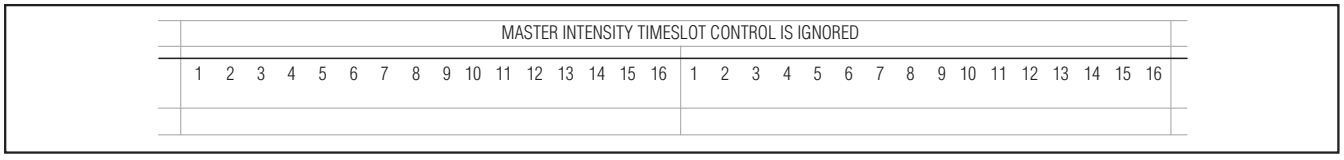


Figure 18. Individual (or Global) Set to 16/16

17-Output LED Driver/GPO with Intensity Control and Hot-Insertion Protection

For example, to operate a 2.2V red LED at 14mA from a 5V supply, R_{LED} = (5 - 2.2 - 0.25) / 0.014 = 182Ω.

Driving Load Currents Higher than 50mA

The MAX6964 can be used to drive loads drawing more than 50mA, like relays and high-current white LEDs, by paralleling outputs. Use at least one output per 50mA of load current; for example, a 6V 330mW relay draws 55mA and needs two paralleled outputs to drive it. Ensure that the paralleled outputs chosen are controlled by the same blink phase register, i.e., select outputs from the O0 through O7 range, or the O8 through O15 range. This way, the paralleled outputs are turned on and off together. Do not use output O16 as part of a load-sharing design. O16 cannot be switched at the same time as any of the other outputs because it is controlled by a different register.

The MAX6964 must be protected from the negative voltage transient generated when switching off inductive loads, such as relays, by connecting a reverse-biased diode across the inductive load (Figure 19). The peak current through the diode is the inductive load's operating current.

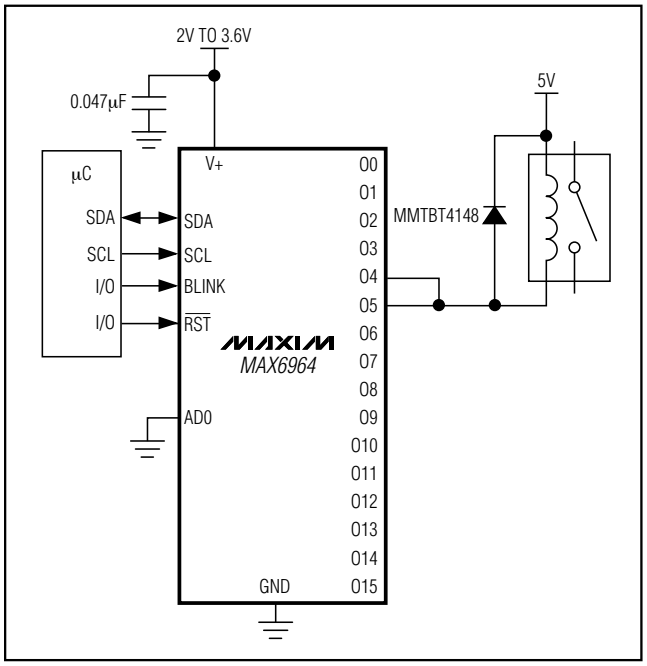


Figure 19. Diode-Protected Switching Inductive Load

Table 9. PWM Intensity Settings (Blink Disabled)

OUTPUT (OR GLOBAL) INTENSITY SETTING	PWM DUTY CYCLE OUTPUT BLINK PHASE 0 REGISTER BIT = 0		LED BEHAVIOR WHEN OUTPUT BLINK PHASE 0 REGISTER BIT = 0 (LED IS ON WHEN OUTPUT IS LOW)	PWM DUTY CYCLE OUTPUT BLINK PHASE 0 REGISTER = 1		LED BEHAVIOR WHEN OUTPUT BLINK PHASE 0 REGISTER BIT = 1 (LED IS ON WHEN OUTPUT IS LOW)
	LOW TIME	HIGH TIME		LOW TIME	HIGH TIME	
0x0	1/16	15/16	Lowest PWM intensity	15/16	1/16	Highest PWM intensity
0x1	2/16	14/16	← Increasing PWM intensity	14/16	2/16	Increasing PWM intensity →
0x2	3/16	13/16		13/16	3/16	
0x3	4/16	12/16		12/16	4/16	
0x4	5/16	11/16		11/16	5/16	
0x5	6/16	10/16		10/16	6/16	
0x6	7/16	9/16		9/16	7/16	
0x7	8/16	8/16		8/16	8/16	
0x8	9/16	7/16		7/16	9/16	
0x9	10/16	6/16		6/16	10/16	
0xA	11/16	5/16		5/16	11/16	
0xB	12/16	4/16		4/16	12/16	
0xC	13/16	3/16		3/16	13/16	
0xD	14/16	2/16		2/16	14/16	
0xE	15/16	1/16	Highest PWM intensity	1/16	15/16	Lowest PWM intensity
0xF	Static low	Static low	Full intensity, no PWM (LED on continuously)	Static high impedance	Static high impedance	LED off continuously

Table 10. PWM Intensity Settings (Blink Enabled)

OUTPUT (OR GLOBAL) INTENSITY SETTING	PWM DUTY CYCLE OUTPUT BLINK PHASE X REGISTER BIT = 0		PWM DUTY CYCLE OUTPUT BLINK PHASE X REGISTER = 1		EXAMPLES OF LED BLINK BEHAVIOR (LED IS ON WHEN OUTPUT IS LOW)	
					BLINK PHASE 0 REGISTER BIT = 0 BLINK PHASE 1 REGISTER BIT = 1	BLINK PHASE 0 REGISTER BIT = 1 BLINK PHASE 1 REGISTER BIT = 0
	LOW TIME	HIGH TIME	LOW TIME	HIGH TIME		
0x0	1/16	15/16	15/16	1/16	Phase 0: LED on at low intensity Phase 1: LED on at high intensity	Phase 0: LED on at high intensity Phase 1: LED on at low intensity
0x1	2/16	14/16	14/16	2/16		
0x2	3/16	13/16	13/16	3/16		
0x3	4/16	12/16	12/16	4/16		
0x4	5/16	11/16	11/16	5/16		
0x5	6/16	10/16	10/16	6/16		
0x6	7/16	9/16	9/16	7/16		
0x7	8/16	8/16	8/16	8/16	Output is half intensity during both blink phases	
0x8	9/16	7/16	7/16	9/16	Phase 0: LED on at high intensity Phase 1: LED on at low intensity	Phase 0: LED on at low intensity Phase 1: LED on at high intensity
0x9	10/16	6/16	6/16	10/16		
0xA	11/16	5/16	5/16	11/16		
0xB	12/16	4/16	4/16	12/16		
0xC	13/16	3/16	3/16	13/16		
0xD	14/16	2/16	2/16	14/16		
0xE	15/16	1/16	1/16	15/16		
0xF	Static low	Static low	Static high impedance	Static high impedance	Phase 0: LED on continuously Phase 1: LED off continuously	Phase 0: LED off continuously Phase 1: LED on continuously

Power-Supply Considerations

The MAX6964 operates with a power-supply voltage of 2V to 3.6V. Bypass the power supply to GND with at least 0.047µF as close to the device as possible. For the QFN version, connect the underside exposed pad to GND.

Table 11. Master, O16 Intensity Register

REGISTER	R/$\overline{W}$	ADDRESS CODE (hex)	REGISTER DATA							
			D7	D6	D5	D4	D3	D2	D1	D0
MASTER AND GLOBAL INTENSITY			MSB			LSB	MSB			LSB
			MASTER INTENSITY				O16 INTENSITY			
Write master and global intensity	0		M3	M2	M1	M0	G3	G2	G1	G0
Read back master and global intensity	1									
Master intensity duty cycle is 0/15 (off); **internal oscillator is disabled;** all outputs will be static with no PWM	—		0	0	0	0	—	—	—	—
Master intensity duty cycle is 1/15	—		0	0	0	1	—	—	—	—
Master intensity duty cycle is 2/15	—		0	0	1	0	—	—	—	—
Master intensity duty cycle is 3/15	—		0	0	1	1	—	—	—	—
—	—		—	—	—	—	—	—	—	—
Master intensity duty cycle is 13/15	—	0X0E	1	1	0	1	—	—	—	—
Master intensity duty cycle is 14/15	—		1	1	1	0	—	—	—	—
Master intensity duty cycle is 15/15 (full)	—		1	1	1	1	—	—	—	—
O/16 intensity duty cycle is 1/16	—		—	—	—	—	0	0	0	0
O/16 intensity duty cycle is 2/16	—		—	—	—	—	0	0	0	1
O/16 intensity duty cycle is 3/16	—		—	—	—	—	0	0	1	0
—	—		—	—	—	—	—	—	—	—
O/16 intensity duty cycle is 14/16	—		—	—	—	—	1	1	0	1
O/16 intensity duty cycle is 15/16	—		—	—	—	—	1	1	1	0
O/16 intensity duty cycle is 16/16 (static output, no PWM)	—		—	—	—	—	1	1	1	1

Table 12. Output Intensity Registers

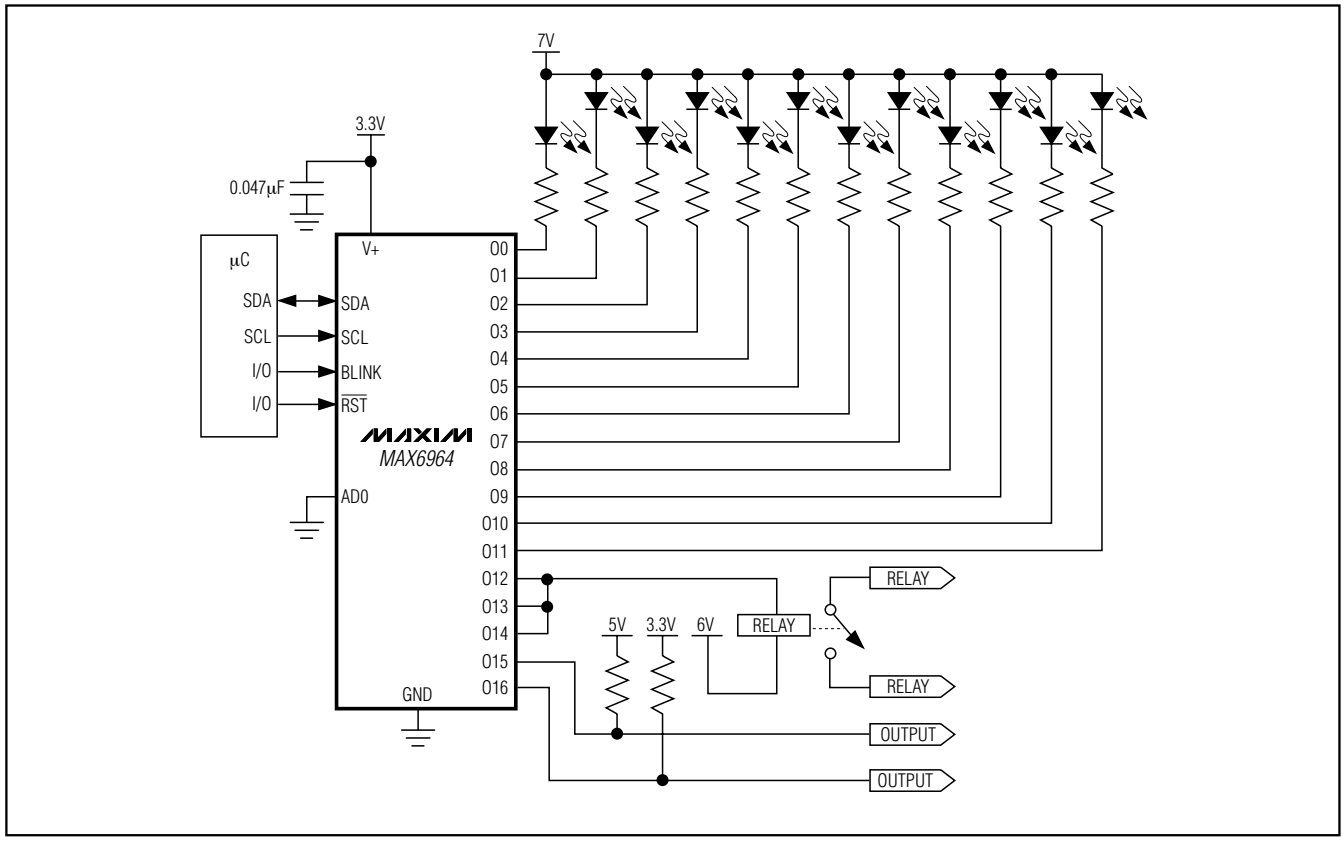
REGISTER	R/$\overline{W}$	ADDRESS CODE (hex)	REGISTER DATA							
			D7	D6	D5	D4	D3	D2	D1	D0
OUTPUTS O1, O0 INTENSITY		0X10	**MSB**			**LSB**	**MSB**			**LSB**
			OUTPUT O1 INTENSITY				**OUTPUT O0 INTENSITY**			
Write output O1, O0 intensity	0		O1I3	O1I2	O1I1	O1I0	O0I3	O0I2	O0I1	O0I0
Read back output O1, O0 intensity	1									
Output O1 intensity duty cycle is 1/16	—		0	0	0	0	—	—	—	—
Output O1 intensity duty cycle is 2/16	—		0	0	0	1	—	—	—	—
Output O1 intensity duty cycle is 3/16	—		0	0	1	0	—	—	—	—
—	—		—	—	—	—	—	—	—	—
Output O1 intensity duty cycle is 14/16	—		1	1	0	1	—	—	—	—
Output O1 intensity duty cycle is 15/16	—		1	1	1	0	—	—	—	—
Output O1 intensity duty cycle is 16/16 (static logic level, no PWM)	—		1	1	1	1	—	—	—	—
Output O0 intensity duty cycle is 1/16	—		—	—	—	—	0	0	0	0
Output O0 intensity duty cycle is 2/16	—		—	—	—	—	0	0	0	1
Output O0 intensity duty cycle is 3/16	—		—	—	—	—	0	0	1	0
—	—		—	—	—	—	—	—	—	—
Output O0 intensity duty cycle is 14/16	—		—	—	—	—	1	1	0	1
Output O0 intensity duty cycle is 15/16	—		—	—	—	—	1	1	1	0
Output O0 intensity duty cycle is 16/16 (static logic level, no PWM)	—		—	—	—	—	1	1	1	1
OUTPUTS O3, O2 INTENSITY		0x11	**MSB**			**LSB**	**MSB**			**LSB**
			OUTPUT O3 INTENSITY				**OUTPUT O2 INTENSITY**			
Write output O3, O2 intensity	0		O3I3	O3I2	O3I1	O3I0	O2I3	O2I2	O2I1	O2I0
Read back output O3, O2 intensity	1									
OUTPUTS O5, O4 INTENSITY		0x12	**MSB**			**LSB**	**MSB**			**LSB**
			OUTPUT O5 INTENSITY				**OUTPUT O4 INTENSITY**			
Write output O5, O4 intensity	0		O5I3	O5I2	O5I1	O5I0	O4I3	O4I2	O4I1	O4I0
Read back output O5, O4 intensity	1									
OUTPUTS O7, O6 INTENSITY		0x13	**MSB**			**LSB**	**MSB**			**LSB**
			OUTPUT O7 INTENSITY				**OUTPUT O6 INTENSITY**			
Write output O7, O6 intensity	0		O7I3	O7I2	O7I1	O7I0	O6I3	O6I2	O6I1	O6I0
Read back output O7, O6 intensity	1									

Table 12. Output Intensity Registers (continued)

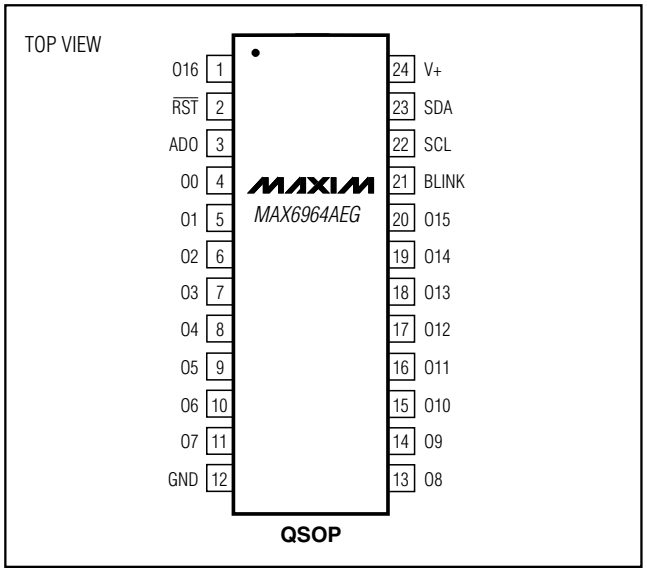
REGISTER	R/$\overline{W}$	ADDRESS CODE (hex)	REGISTER DATA							
			D7	D6	D5	D4	D3	D2	D1	D0
OUTPUTS O9, O8 INTENSITY		0x14	**MSB**			**LSB**	**MSB**			**LSB**
			OUTPUT O9 INTENSITY				**OUTPUT O8 INTENSITY**			
Write output O9, O8 intensity	0		O9I3	O9I2	O9I1	O9I0	O8I3	O8I2	O8I1	O8I0
Read back output O9, O8 intensity	1									
OUTPUTS O11, O10 INTENSITY		0x15	**MSB**			**LSB**	**MSB**			**LSB**
			OUTPUT O11 INTENSITY				**OUTPUT O10 INTENSITY**			
Write output O11, O10 intensity	0		O11I3	O11I2	O11I1	O11I0	O10I3	O10I2	O10I1	O10I0
Read back output O11, O10 intensity	1									
OUTPUTS O13, O12 INTENSITY		0x16	**MSB**			**LSB**	**MSB**			**LSB**
			OUTPUT O13 INTENSITY				**OUTPUT O12 INTENSITY**			
Write output O13, O12 intensity	0		O13I3	O13I2	O13I1	O13I0	O12I3	O12I2	O12I1	O12I0
Read back output O13, O12 intensity	1									
OUTPUTS O15, O14 INTENSITY		0x17	**MSB**			**LSB**	**MSB**			**LSB**
			OUTPUT O15 INTENSITY				**OUTPUT O14 INTENSITY**			
Write output O15, O14 intensity	0		O15I3	O15I2	O15I1	O15I0	O14I3	O14I2	O14I1	O14I0
Read back output O15, O14 intensity	1									
OUTPUT O16 INTENSITY			See master, 016 register (Table 11).							

17-Output LED Driver/GPO with Intensity Control and Hot-Insertion Protection

Typical Application Circuit



Pin Configurations (continued)



Chip Information

TRANSISTOR COUNT: 25,991

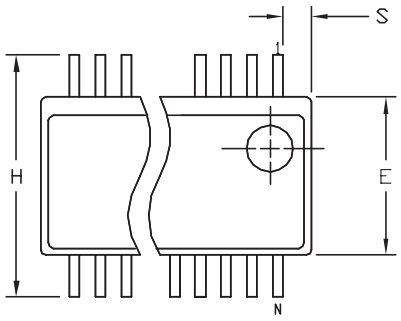
PROCESS: BiCMOS

17-Output LED Driver/GPO with Intensity Control and Hot-Insertion Protection

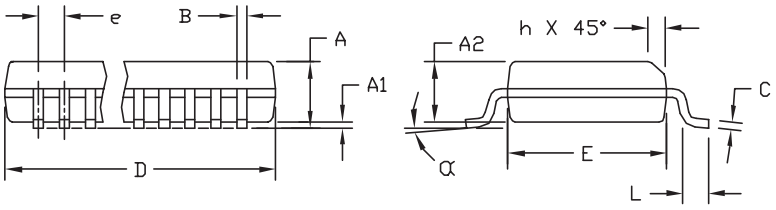
Package Information

(The package drawing(s) in this data sheet may not reflect the most current specifications. For the latest package outline information, go to **www.maxim-ic.com/packages**.)

QSOP.EPS



DIM	INCHES MIN	INCHES MAX	MILLIMETERS MIN	MILLIMETERS MAX
A	.053	.069	1.35	1.75
A1	.004	.010	.102	.254
A2	.049	.065	1.245	1.651
B	.008	.012	0.20	0.30
C	.0075	.0098	0.191	0.249
D	SEE VARIATIONS			
E	.150	.157	3.81	3.99
e	.025 BSC		0.635 BSC	
H	.230	.244	5.84	6.20
h	.010	.016	0.25	0.41
L	.016	.035	0.41	0.89
N	SEE VARIATIONS			
α	0°	8°	0°	8°



VARIATIONS:

	INCHES MIN.	INCHES MAX.	MILLIMETERS MIN.	MILLIMETERS MAX.	N	
D	.189	.196	4.80	4.98	16	AB
S	.0020	.0070	0.05	0.18		
D	.337	.344	8.56	8.74	20	AD
S	.0500	.0550	1.270	1.397		
D	.337	.344	8.56	8.74	24	AE
S	.0250	.0300	0.635	0.762		
D	.386	.393	9.80	9.98	28	AF
S	.0250	.0300	0.635	0.762		

NOTES:
1). D & E DO NOT INCLUDE MOLD FLASH OR PROTRUSIONS.
2). MOLD FLASH OR PROTRUSIONS NOT TO EXCEED .006" PER SIDE.
3). CONTROLLING DIMENSIONS: INCHES.
4). MEETS JEDEC MO137.

DALLAS SEMICONDUCTOR MAXIM
PROPRIETARY INFORMATION

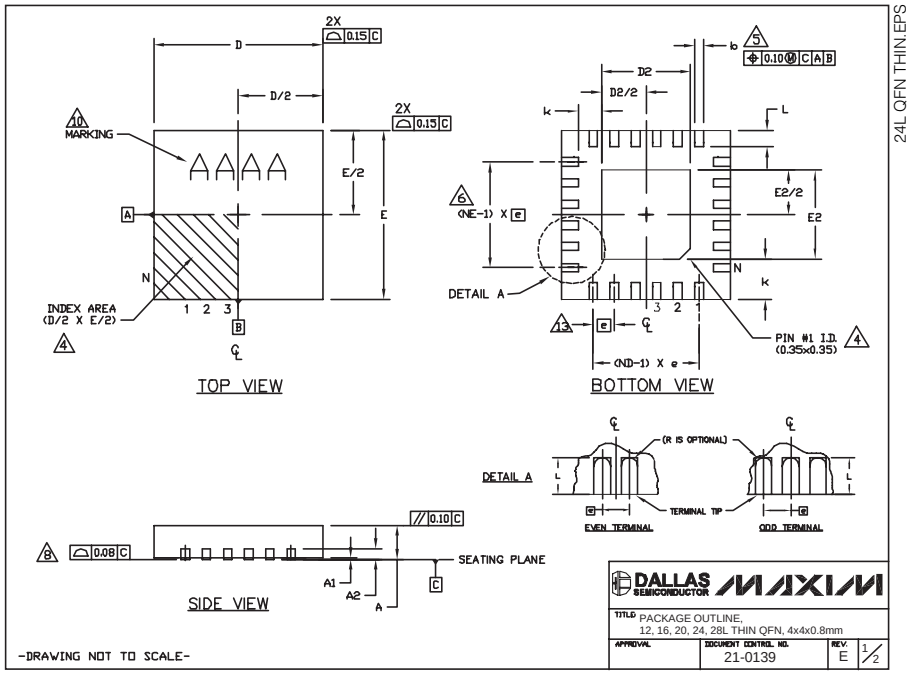
TITLE:
PACKAGE OUTLINE, QSOP .150", .025" LEAD PITCH

APPROVAL	DOCUMENT CONTROL NO.	REV.	
	21-0055	F	1/1

Package Information (continued)

(The package drawing(s) in this data sheet may not reflect the most current specifications. For the latest package outline information, go to **www.maxim-ic.com/packages**.)

24L QFN THIN.EPS



COMMON DIMENSIONS

PKG	12L 4x4			16L 4x4			20L 4x4			24L 4x4			28L 4x4		
REF.	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A	0.70	0.75	0.80	0.70	0.75	0.80	0.70	0.75	0.80	0.70	0.75	0.80	0.70	0.75	0.80
A1	0.0	0.02	0.05	0.0	0.02	0.05	0.0	0.02	0.05	0.0	0.02	0.05	0.0	0.02	0.05
A2	0.20 REF			0.20 REF			0.20 REF			0.20 REF			0.20 REF		
b	0.25	0.30	0.35	0.25	0.30	0.35	0.20	0.25	0.30	0.18	0.23	0.30	0.15	0.20	0.25
D	3.90	4.00	4.10	3.90	4.00	4.10	3.90	4.00	4.10	3.90	4.00	4.10	3.90	4.00	4.10
E	3.90	4.00	4.10	3.90	4.00	4.10	3.90	4.00	4.10	3.90	4.00	4.10	3.90	4.00	4.10
e	0.80 BSC.			0.65 BSC.			0.50 BSC.			0.50 BSC.			0.40 BSC.		
k	0.25	-	-	0.25	-	-	0.25	-	-	0.25	-	-	0.25	-	-
L	0.45	0.55	0.65	0.45	0.55	0.65	0.45	0.55	0.65	0.30	0.40	0.50	0.30	0.40	0.50
N	12			16			20			24			28		
ND	3			4			5			6			7		
NE	3			4			5			6			7		
Jedec Var.	WGGB			WGGC			WGGD-1			WGGD-2			WGGE		

EXPOSED PAD VARIATIONS

PKG. CODES	D2			E2			DOWN BONDS ALLOWED
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.	
T1244-3	1.95	2.10	2.25	1.95	2.10	2.25	YES
T1244-4	1.95	2.10	2.25	1.95	2.10	2.25	NO
T1644-3	1.95	2.10	2.25	1.95	2.10	2.25	YES
T1644-4	1.95	2.10	2.25	1.95	2.10	2.25	NO
T2044-2	1.95	2.10	2.25	1.95	2.10	2.25	YES
T2044-3	1.95	2.10	2.25	1.95	2.10	2.25	NO
T2444-2	1.95	2.10	2.25	1.95	2.10	2.25	YES
T2444-3	2.45	2.60	2.63	2.45	2.60	2.63	YES
T2444-4	2.45	2.60	2.63	2.45	2.60	2.63	NO
T2844-1	2.50	2.60	2.70	2.50	2.60	2.70	NO

NOTES:

1. DIMENSIONING & TOLERANCING CONFORM TO ASME Y14.5M-1994.
2. ALL DIMENSIONS ARE IN MILLIMETERS. ANGLES ARE IN DEGREES.
3. N IS THE TOTAL NUMBER OF TERMINALS.
4. THE TERMINAL #1 IDENTIFIER AND TERMINAL NUMBERING CONVENTION SHALL CONFORM TO JESD 95-1 SPP-012. DETAILS OF TERMINAL #1 IDENTIFIER ARE OPTIONAL, BUT MUST BE LOCATED WITHIN THE ZONE INDICATED. THE TERMINAL #1 IDENTIFIER MAY BE EITHER A MOLD OR MARKED FEATURE.
5. DIMENSION b APPLIES TO METALLIZED TERMINAL AND IS MEASURED BETWEEN 0.25 mm AND 0.30 mm FROM TERMINAL TIP.
6. ND AND NE REFER TO THE NUMBER OF TERMINALS ON EACH D AND E SIDE RESPECTIVELY.
7. DEPOPULATION IS POSSIBLE IN A SYMMETRICAL FASHION.
8. COPLANARITY APPLIES TO THE EXPOSED HEAT SINK SLUG AS WELL AS THE TERMINALS.
9. DRAWING CONFORMS TO JEDEC MO220, EXCEPT FOR T2444-3, T2444-4 AND T2844-1.
10. MARKING IS FOR PACKAGE ORIENTATION REFERENCE ONLY.
11. COPLANARITY SHALL NOT EXCEED 0.08mm
12. WARPAGE SHALL NOT EXCEEND 0.10mm
13. LEAD CENTERLINES TO BE AT TRUE POSITION AS DEFINED BY BASIC DIMENSION "e", ±0.05.
14. NUMBER OF LEADS SHOWN ARE FOR REFERENCE ONLY

-DRAWING NOT TO SCALE-

DALLAS SEMICONDUCTOR MAXIM
PACKAGE OUTLINE, 12, 16, 20, 24, 28L THIN QFN, 4x4x0.8mm
21-0139
E
2/2

Mouser Electronics

Authorized Distributor

Click to View Pricing, Inventory, Delivery & Lifecycle Information:

Maxim Integrated:

MAX6964AEG+ MAX6964AEG+T MAX6964ATG+ MAX6964ATG+T