## Absolute Maximum Ratings

(All pins referenced to GND, unless otherwise noted.)
$V_{IN}$ .....-0.3V to +80V
OUT ..... -0.3V to min (12V, IN + 0.3V)
ENABLE, ENABLE1, ENABLE2.....-0.3V to (IN + 0.3V)
$\overline{RESET}$ (open-drain output), TIMEOUT, WDI, RESETIN, SET .....-0.3V to 12V
$\overline{RESET}$ (push-pull output), $\overline{HOLD}$ .....-0.3V to (OUT + 0.3V)
Maximum Current (all pins except IN and OUT).....50mA
Continuous Power Dissipation ($T_A$ = +70°C)
6-Pin TDFN 3mm x 3mm
(derate 23.8mW/°C above +70°C) .....1904.8mW
8-Pin TDFN 3mm x 3mm
(derate 24.4mW/°C above +70°C) .....1951.2mW
Operating Temperature Range..... -40°C to +125°C
Junction Temperature.....+150°C
Storage Temperature Range..... -65°C to +150°C
Lead Temperature (soldering, 10s) .....+300°C
Soldering Temperature (reflow).....+260°C

*Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.*

## Package Information

### TDFN-6

| PACKAGE CODE | T633+2 |
|---|---|
| Outline Number | 21-0137 |
| Land Pattern Number | 90-0058 |
| **Thermal Resistance, Single-Layer Board:** | |
| Junction to Ambient ($\theta_{JA}$) | 55°C/W |
| Junction to Case ($\theta_{JC}$) | 9°C/W |
| **Thermal Resistance, Multi-Layer Board:** | |
| Junction to Ambient ($\theta_{JA}$) | 42°C/W |
| Junction to Case ($\theta_{JC}$) | 9°C/W |

### TDFN-8

| PACKAGE CODE | T833+2 |
|---|---|
| Outline Number | 21-0137 |
| Land Pattern Number | 90-0058 |
| **Thermal Resistance, Single-Layer Board:** | |
| Junction to Ambient ($\theta_{JA}$) | 54°C/W |
| Junction to Case ($\theta_{JC}$) | 8°C/W |
| **Thermal Resistance, Multi-Layer Board:** | |
| Junction to Ambient ($\theta_{JA}$) | 41°C/W |
| Junction to Case ($\theta_{JC}$) | 8°C/W |

For the latest package outline information and land patterns (footprints), go to **www.maximintegrated.com/packages**. Note that a "+", "#", or "-" in the package code indicates RoHS status only. Package drawings may show a different suffix character, but the drawing pertains to the package regardless of RoHS status.

Package thermal resistances were obtained using the method described in JEDEC specification JESD51-7, using a four-layer board. For detailed information on package thermal considerations, refer to **www.maximintegrated.com/thermal-tutorial**.

## Electrical Characteristics

($V_{IN}$ = 14V, $C_{IN}$ = 0.1µF, $C_{OUT}$ = 10µF, $T_A$ = $T_J$ = -40°C to +125°C, unless otherwise noted. Typical values are at $T_A$ = $T_J$ = +25°C.) (Note 1)

| PARAMETER | SYMBOL | CONDITIONS | MIN | TYP | MAX | UNITS |
|---|---|---|---|---|---|---|
| Supply Voltage Range | $V_{IN}$ | | 4 | | 72 | V |
| Supply Current (MAX6765–MAX6772) (Note 2) | | $I_{LOAD}$ = 0A | | 31 | 45 | µA |
| | | $I_{LOAD}$ = 50mA | | 35 | 50 | |
| | | $I_{LOAD}$ = 100mA, $V_{IN}$ = 14V | | 37 | 55 | |
| | | $I_{LOAD}$ = 0A, $V_{IN}$ = 42V | | 35 | 50 | |
| | | $I_{LOAD}$ = 10mA, $V_{IN}$ = 42V | | 37 | 55 | |
| Supply Current (MAX6773/MAX6773B/ MAX6774/MAX6774B) (Note 2) | | $I_{LOAD}$ = 0A | | 38 | 50 | µA |
| | | $I_{LOAD}$ = 50mA | | 42 | 55 | |
| | | $I_{LOAD}$ = 100mA | | 44 | 60 | |
| | | $I_{LOAD}$ = 0A, $V_{IN}$ = 42V | | 42 | 55 | |
| | | $I_{LOAD}$ = 10mA, $V_{IN}$ = 42V | | 44 | 60 | |
| Shutdown Supply Current | $I_{SHDN}$ | ENABLE , ENABLE1, ENABLE2 = GND | | 3.3 | 7 | µA |
| Output Voltage | $V_{OUT}$ | L/M, $I_{LOAD}$ = 1mA | 4.925 | 5 | 5.075 | V |
| | | L/M, 1mA ≤ $I_{LOAD}$ ≤ 100mA, $V_{IN}$ = 11V | 4.850 | 5 | 5.150 | |
| | | T/S, $I_{LOAD}$ = 1mA | 3.251 | 3.3 | 3.350 | |
| | | T/S, 1mA ≤ $I_{LOAD}$ ≤ 100mA, $V_{IN}$ = 9.3V | 3.201 | 3.3 | 3.399 | |
| | | Z/Y, $I_{LOAD}$ = 1mA | 2.463 | 2.5 | 2.538 | |
| | | Z/Y, 1mA ≤ $I_{LOAD}$ ≤ 100mA, $V_{IN}$ = 8.5V | 2.425 | 2.5 | 2.575 | |
| | | W/V, $I_{LOAD}$ = 1mA | 1.773 | 1.8 | 1.827 | |
| | | W/V, 1mA ≤ $I_{LOAD}$ ≤ 100mA, $V_{IN}$ = 7.8V | 1.746 | 1.8 | 1.854 | |
| Adjustable Output Voltage Range | $V_{OUT}$ | | 1.8 | | 11.0 | V |
| SET Threshold Voltage (MAX6767–MAX6774) | $V_{SET}$ | $I_{LOAD}$ = 1mA | 1.20 | 1.233 | 1.26 | V |
| Dual Mode™ SET Threshold | | SET rising | | 116 | | mV |
| | | SET falling | | 58 | | |

*Dual Mode is a trademark of Maxim Integrated Products, Inc.*

## Electrical Characteristics (continued)

($V_{IN}$ = 14V, $C_{IN}$ = 0.1µF, $C_{OUT}$ = 10µF, $T_A$ = $T_J$ = -40°C to +125°C, unless otherwise noted. Typical values are at $T_A$ = $T_J$ = +25°C.) (Note 1)

| PARAMETER | SYMBOL | CONDITIONS | | MIN | TYP | MAX | UNITS |
|---|---|---|---|---|---|---|---|
| SET Input Current (MAX6767–MAX6774) | $I_{SET}$ | $V_{SET}$ = 1.5V, $V_{IN}$ = 11V | | -100 | | +100 | nA |
| Dropout Voltage (Note 3) | $\Delta V_{DO}$ | L/M, 5V output option, $I_{LOAD}$ = 10mA | | | 60 | 130 | mV |
| | | L/M, 5V output option, $I_{LOAD}$ = 50mA | | | 300 | 630 | |
| | | L/M, 5V output option, $I_{LOAD}$ = 100mA | | | 620 | 1200 | |
| | | T/S, 3.3V output option, $I_{LOAD}$ = 100mA | | | 866 | 1600 | |
| Guaranteed Output Current (Note 4) | | | | 100 | | | mA |
| Output Current Limit | | Output shorted to GND, $V_{IN}$ = 14V | | 150 | 250 | | mA |
| Thermal-Shutdown Temperature | | | | | 160 | | °C |
| Thermal-Shutdown Hysteresis | | | | | 20 | | °C |
| Line Regulation | | 6.5V ≤ $V_{IN}$ ≤ 72V, $I_{LOAD}$ = 1mA | | | | 1 | % |
| Load Regulation (MAX6767–MAX6774) | | $I_{OUT}$ = 1mA to 100mA, $V_{IN}$ = $V_{OUT(NOM)}$ + 6V | | | | 1.5 | % |
| Power-Supply Rejection Ratio | PSRR | $I_{LOAD}$ = 10mA, $f_{IN}$ = 100Hz, 500m$V_{P-P}$ | | | 70 | | dB |
| Startup Response Time | $t_{START}$ | From ENABLE high to OUT, $I_{LOAD}$ = 100mA | | | 180 | | µs |
| Output Overvoltage Protection Threshold | $OV_{TH}$ | $I_{SINK}$ = 1mA (from OUT) | | 1.07 x $V_{OUT}$ | 1.1 x $V_{OUT}$ | 1.13 x $V_{OUT}$ | V |
| Output Overvoltage Protection Maximum Sink Current | | OUT = $OUT_{(NOM)}$ x 1.15 | | 5 | 10 | | mA |
| **LOGIC INPUT (ENABLE, ENABLE1, ENABLE2, $\overline{HOLD}$)** | | | | | | | |
| Input Low Voltage | $V_{IL}$ | ENABLE, ENABLE1, ENABLE2 | | | | 0.4 | V |
| Input High Voltage | $V_{IH}$ | ENABLE, ENABLE1, ENABLE2 | | 1.4 | | | V |
| ENABLE, ENABLE1, ENABLE2 Input Pulldown Current | | ENABLE, ENABLE1, ENABLE2 are internally pulled down to GND | | | 0.6 | | µA |
| $\overline{HOLD}$ Input Threshold Voltage | $V_{IL}$ | 1.8V ≤ $V_{OUT}$ ≤ 11V | | | | 0.4 | V |
| | $V_{IH}$ | 1.8V ≤ $V_{OUT}$ ≤ 11V | | OUT - 0.4 | | | |
| $\overline{HOLD}$ Input Pullup Current | | $\overline{HOLD}$ is internally pulled up to OUT | | | 1.8 | | µA |
| **$\overline{RESET}$ OUTPUT** | | | | | | | |
| $\overline{RESET}$ Threshold | | SET = GND, $\overline{RESET}$ falling | L | 4.500 | 4.625 | 4.750 | V |
| | | | M | 4.250 | 4.375 | 4.500 | |
| | | | T | 2.970 | 3.053 | 3.135 | |
| | | | S | 2.805 | 2.888 | 2.970 | |
| | | | Z | 2.250 | 2.313 | 2.375 | |
| | | | Y | 2.125 | 2.188 | 2.250 | |
| | | | W | 1.620 | 1.665 | 1.710 | |
| | | | V | 1.530 | 1.575 | 1.620 | |

## Electrical Characteristics (continued)

($V_{IN}$ = 14V, $C_{IN}$ = 0.1µF, $C_{OUT}$ = 10µF, $T_A$ = $T_J$ = -40°C to +125°C, unless otherwise noted. Typical values are at $T_A$ = $T_J$ = +25°C.) (Note 1)

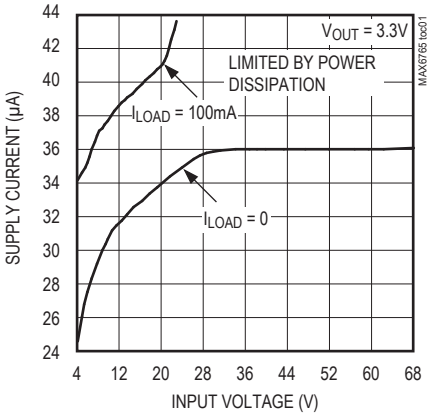
| PARAMETER | SYMBOL | CONDITIONS | | MIN | TYP | MAX | UNITS |
|---|---|---|---|---|---|---|---|
| $\overline{RESET}$ Threshold (Adjustable Output Voltage) | | L/T/Z/W, SET = resistive divider, $\overline{RESET}$ falling | | $V_{OUT}$ x 0.9 | $V_{OUT}$ x 0.925 | $V_{OUT}$ x 0.950 | V |
| | | M/S/Y/V, SET = resistive divider, $\overline{RESET}$ falling | | $V_{OUT}$ x 0.85 | $V_{OUT}$ x 0.875 | $V_{OUT}$ x 0.900 | |
| RESETIN Input Current | | $V_{RESETIN}$ = $V_{GND}$ or 12V | | -100 | | +100 | nA |
| RESETIN Threshold | | $V_{TH}$ = 87.5% of $V_{SET}$ (M/S/Y/V), $\overline{RESET}$ falling | | 1.057 | 1.085 | 1.112 | V |
| | | $V_{TH}$ = 92.5% of $V_{SET}$ (L/T/Z/W), $\overline{RESET}$ falling | | 1.118 | 1.147 | 1.176 | |
| OUT to $\overline{RESET}$ Delay | | $V_{OUT}$ falling | | | 0.3 | | µs |
| RESETIN To $\overline{RESET}$ Delay | | RESETIN falling | | | 35 | | µs |
| $\overline{RESET}$ Timeout Period (TIMEOUT Connected to OUT) | | $V_{OUT}$ rising | D0 | | 75 | | µs |
| | | | D1 | 2.187 | 3.125 | 4.063 | ms |
| | | | D2 | 8.75 | 12.5 | 16.25 | |
| | | | D3 | 35 | 50 | 65 | |
| | | | D4 | 140 | 200 | 260 | |
| TIMEOUT Ramp Current | | | | 800 | 1000 | 1200 | nA |
| TIMEOUT Ramp Threshold | | L/M/T/S options | | 1.160 | 1.220 | 1.259 | V |
| | | V/W/Y/Z options | | 1.060 | 1.170 | 1.242 | |
| $\overline{RESET}$ Output-Voltage Low (Open Drain or Push-Pull) | $V_{OL}$ | $V_{OUT}$ ≥ 1.8V, $I_{SINK}$ = 50µA, $\overline{RESET}$ asserted | | | | 0.3 | V |
| | | $V_{OUT}$ ≥ 1.8V, $I_{SINK}$ = 3.2mA, $\overline{RESET}$ asserted | | | | 0.4 | |
| $\overline{RESET}$ Output-Voltage High (Push-Pull) | $V_{OH}$ | $V_{OUT}$ ≥ 1.8V, $I_{SOURCE}$ = 250µA, $\overline{RESET}$ not asserted | | 0.8 x $V_{OUT}$ | | | V |
| $\overline{RESET}$ Open-Drain Leakage Current | | $\overline{RESET}$ not asserted, $\overline{RESET}$ = 12V | | | | 100 | nA |
| Watchdog Minimum Input Pulse | $t_{WDI}$ | 1.8V ≤ $V_{OUT}$ ≤ 11V | | 1 | | | µs |
| Watchdog Input Low Voltage | $V_{IL}$ | 1.8V ≤ $V_{OUT}$ ≤ 11V | | | | 0.4 | V |
| Watchdog Input High Voltage | $V_{IH}$ | 1.8V ≤ $V_{OUT}$ ≤ 11V | | $V_{OUT}$ - 0.4V | | | V |
| Watchdog Input Low Voltage | $V_{IL}$ | 1.8V ≤ $V_{OUT}$ ≤ 11V | | | | 0.4 | V |
| Watchdog Input Current | $I_{WDI}$ | $V_{WDI}$ = 0V or $V_{WDI}$ = 12V | | -1 | | +1 | µA |
| Watchdog Timeout Period | $t_{WD}$ | MAX6773/MAX6774 | | 1.12 | 1.6 | 2.08 | s |
| | | MAX6773B/MAX6774B | | 40 | 50 | 60 | ms |

**Note 1:** Production tested at $T_A$ = +25°C. Overtemperature limits are guaranteed by design.
**Note 2:** Device tested at internally set voltage.
**Note 3:** Dropout voltage for L/M versions is defined as ($V_{IN}$ - $V_{OUT}$) when $V_{OUT}$ equals 98% of the nominal value of $V_{OUT}$ when $V_{IN}$ = 11V. For T/S versions, dropout voltage is defined as ($V_{IN}$ - $V_{OUT}$) when $V_{OUT}$ equals 98% of the nominal value of $V_{OUT}$ when $V_{IN}$ = 9.3V.
**Note 4:** Observe the absolute maximum power dissipation limits.

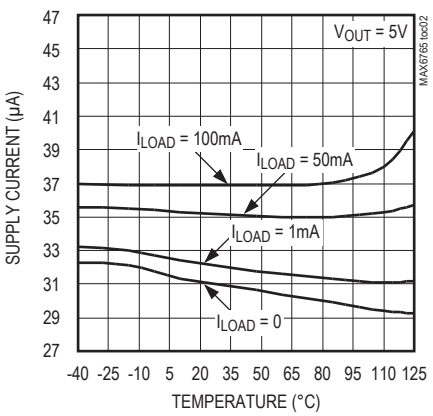
## Typical Operating Characteristics

($V_{IN}$ = 14V, $C_{OUT}$ = 10µF, $C_{IN}$ = 0.1µF, $T_A$ = +25°C, unless otherwise noted.)

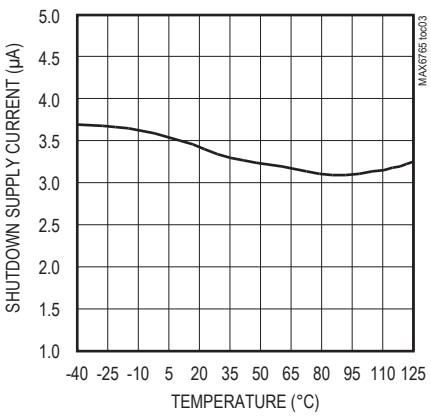
**SUPPLY CURRENT vs. INPUT VOLTAGE**



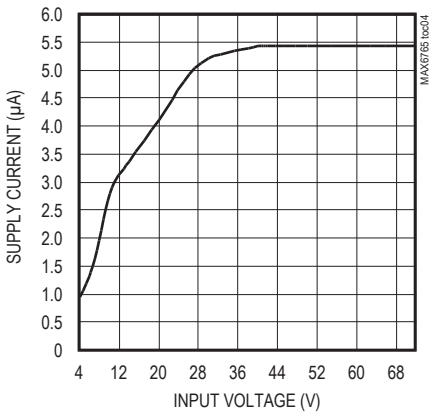

**SUPPLY CURRENT vs. TEMPERATURE**



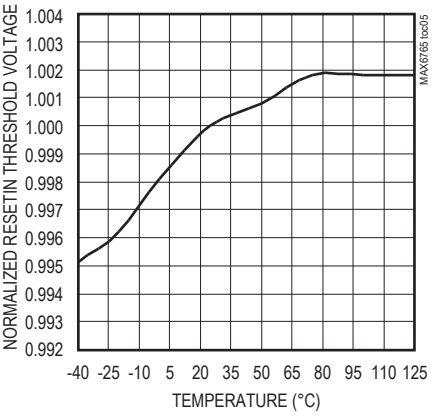

**SHUTDOWN SUPPLY CURRENT vs. TEMPERATURE**



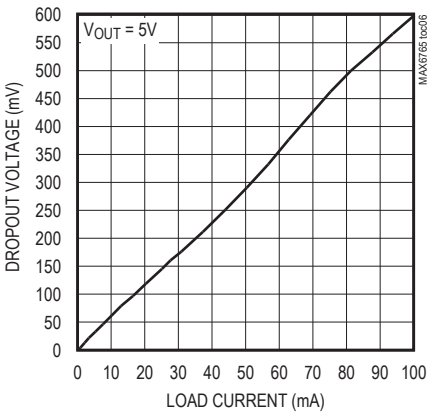

**SHUTDOWN SUPPLY CURRENT vs. INPUT VOLTAGE**



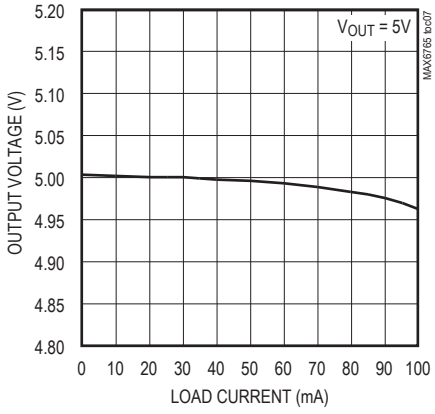

**NORMALIZED RESETIN THRESHOLD VOLTAGE vs. TEMPERATURE**



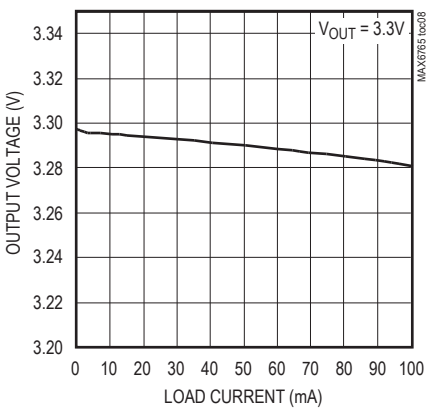

**DROPOUT VOLTAGE vs. LOAD CURRENT**




**OUTPUT VOLTAGE vs. LOAD CURRENT**



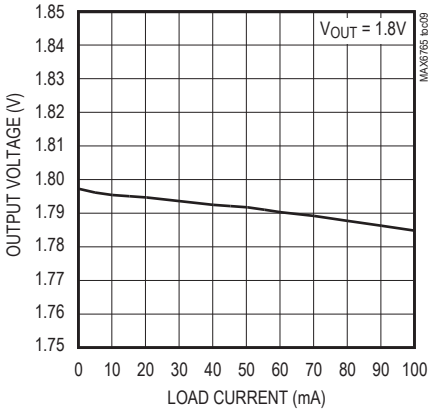

**OUTPUT VOLTAGE vs. LOAD CURRENT**



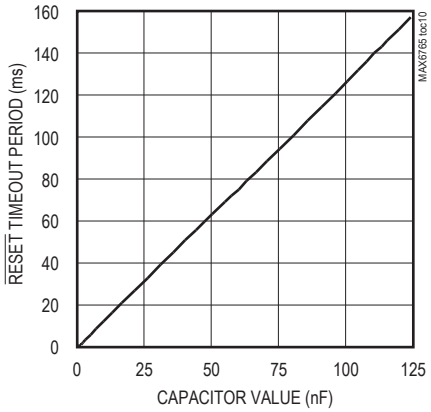
## Typical Operating Characteristics (continued)

($V_{IN}$ = 14V, $C_{OUT}$ = 10µF, $C_{IN}$ = 0.1µF, $T_A$ = +25°C, unless otherwise noted.)

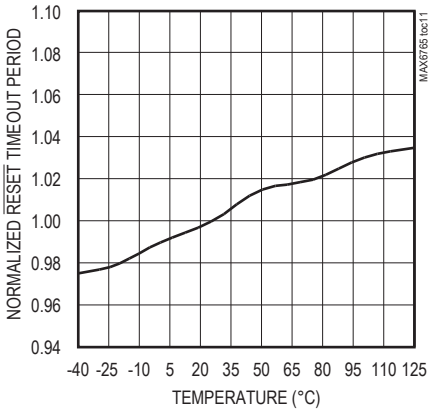
**OUTPUT VOLTAGE vs. LOAD CURRENT**



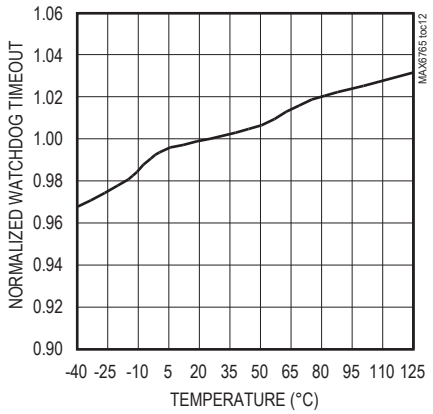

**RESET TIMEOUT PERIOD vs. CAPACITOR VALUE**



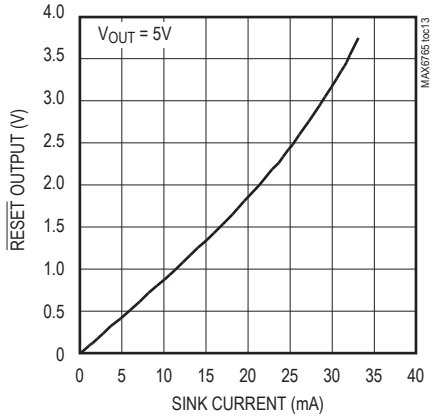

**NORMALIZED RESET TIMEOUT PERIOD vs. TEMPERATURE**



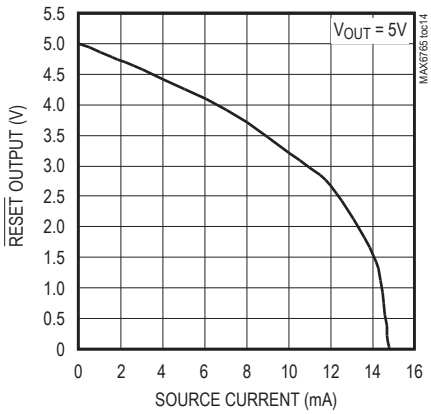

**NORMALIZED WATCHDOG TIMEOUT vs. TEMPERATURE**



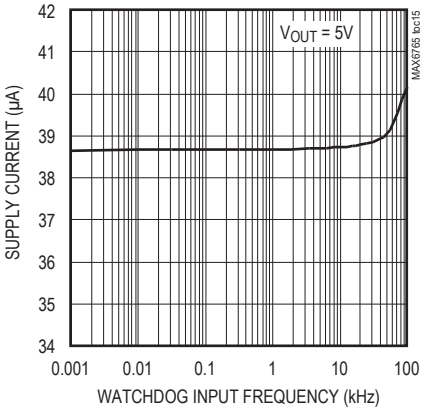

**RESET OUTPUT vs. SINK CURRENT**



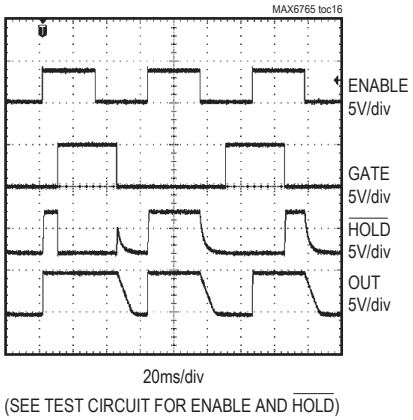

**RESET OUTPUT vs. SOURCE CURRENT**




**SUPPLY CURRENT vs. WATCHDOG INPUT FREQUENCY**




**OUT AND HOLD vs. ENABLE**

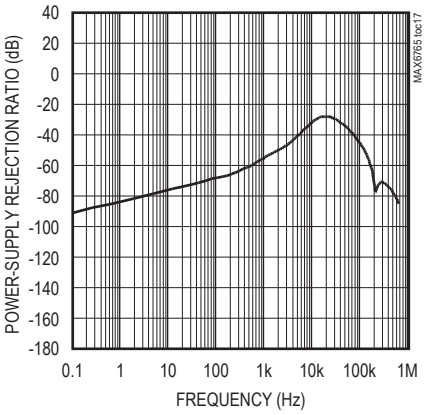



(SEE TEST CIRCUIT FOR ENABLE AND HOLD)

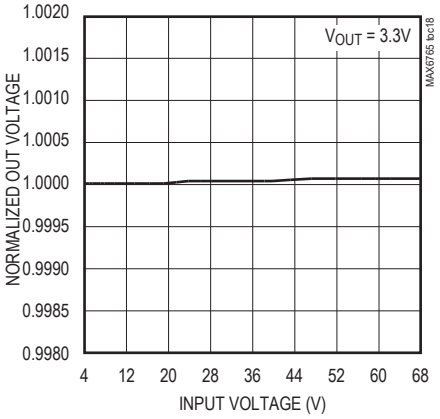
## Typical Operating Characteristics (continued)

($V_{IN}$ = 14V, $C_{OUT}$ = 10µF, $C_{IN}$ = 0.1µF, $T_A$ = +25°C, unless otherwise noted.)

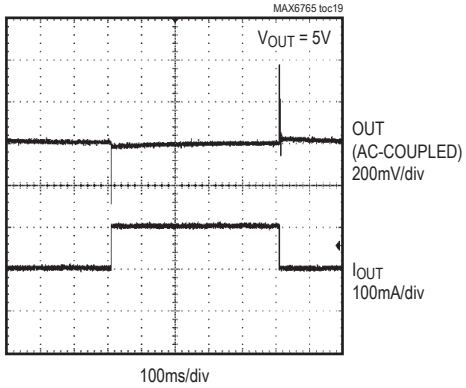
**POWER-SUPPLY REJECTION RATIO vs. FREQUENCY**



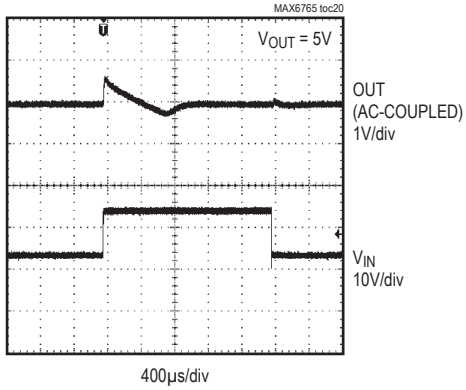

**NORMALIZED OUT VOLTAGE vs. INPUT VOLTAGE**



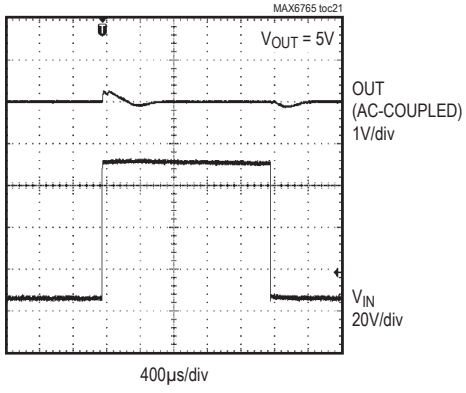

**LOAD-TRANSIENT RESPONSE**



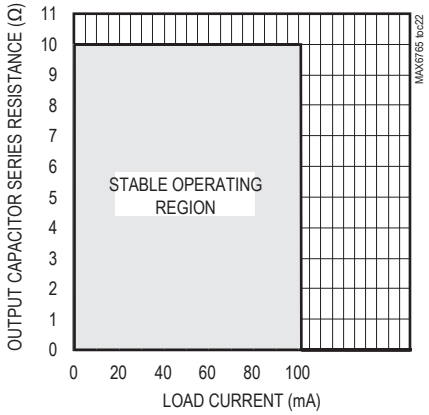

**LINE-TRANSIENT RESPONSE**



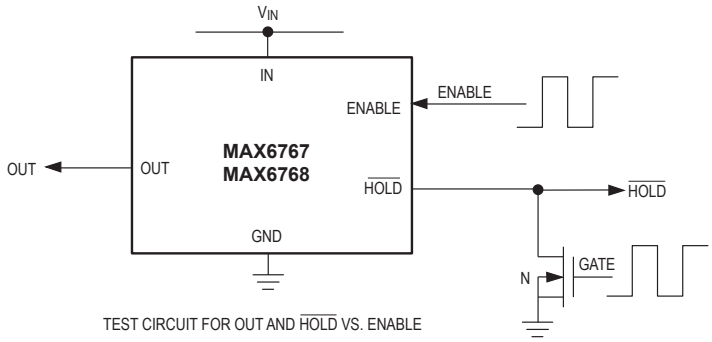

**LINE-TRANSIENT RESPONSE**




**OUTPUT CAPACITOR SERIES RESIGTANCE vs. LOAD CURRENT**



## Enable and Hold Test Circuit




TEST CIRCUIT FOR OUT AND $\overline{HOLD}$ VS. ENABLE

## Pin Description

| PIN | | | | | NAME | FUNCTION |
|---|---|---|---|---|---|---|
| MAX6765/ MAX6766 | MAX6767/ MAX6768 | MAX6769/ MAX6770 | MAX6771/ MAX6772 | MAX6773/ MAX6773B/ MAX6774/ MAX6774B | | |
| 1 | 1 | 1 | 1 | 1 | IN | Regulator Input. Bypass IN to GND with a capacitor with a minimum value of 0.1µF. |
| 2 | 2 | 2 | 2 | 2 | GND | Ground |
| 3 | 3 | 3 | — | 3 | ENABLE | Active-High Enable Input. Drive ENABLE high to turn on the regulator. ENABLE is internally connected to GND through a 0.6µA current sink. |
| 4 | 5 | 5 | 5 | 5 | $\overline{RESET}$ | Active-Low, Open-Drain/Push-Pull Reset Output. For the MAX6769/MAX6770, $\overline{RESET}$ asserts when RESETIN is below the internal $V_{TH}$ and deasserts when RESETIN is above the internal $V_{TH}$ threshold. For all other versions, $\overline{RESET}$ remains low while OUT is below the reset threshold. For all versions, $\overline{RESET}$ remains low for the duration of the reset timeout period after the reset conditions end. |
| 5 | 7 | 7 | 7 | 7 | TIMEOUT | Reset Timeout Adjust Input. Connect TIMEOUT to OUT for the internally fixed timeout period. For an adjustable timeout, connect a capacitor from TIMEOUT to GND. See the *Selecting Timeout Capacitor* section. |
| 6 | 8 | 8 | 8 | 8 | OUT | Regulator Output. The MAX6765/MAX6766 provide a fixed output (+1.8V, +2.5V, +3.3V, or +5V). The MAX6767–MAX6774 provide a fixed output voltage of +1.8V, +2.5V, +3.3V, or 5V, or adjust the output from +1.8V to +11V. Bypass to GND with a 10µF capacitor (min). |

## Pin Description (continued)

| PIN | | | | | NAME | FUNCTION |
|---|---|---|---|---|---|---|
| MAX6765/ MAX6766 | MAX6767/ MAX6768 | MAX6769/ MAX6770 | MAX6771/ MAX6772 | MAX6773/ MAX6773B/ MAX6774/ MAX6774B | | |
| — | 4 | — | — | — | $\overline{\text{HOLD}}$ | Active-Low Regulator Hold Input. When $\overline{\text{HOLD}}$ is forced low, OUT remains on even if ENABLE is pulled low. To shut down the regulator, release $\overline{\text{HOLD}}$ after ENABLE is pulled low. Connect $\overline{\text{HOLD}}$ to OUT or leave unconnected if unused. $\overline{\text{HOLD}}$ is internally connected to OUT through a 1.8µA current source. |
| — | 6 | 6 | 6 | 6 | SET | Feedback Input for Setting the Output Voltage. Connect SET to GND to select the preset output voltage. Connect to an external resistive divider for adjustable output operation. |
| — | — | 4 | — | — | RESETIN | Adjustable Reset Threshold Input. Connect to a resistive divider to set the desired threshold. |
| — | — | — | 3 | — | ENABLE1 | Active-High Enable Input 1. Drive ENABLE1 high to turn on the regulator. ENABLE1 is internally connected to ground through a 0.6µA current sink. |
| — | — | — | 4 | — | ENABLE2 | Active-High Enable Input 2. Drive ENABLE2 high to turn on the regulator. ENABLE2 is internally connected to ground through a 0.6µA current sink. |
| — | — | — | — | 4 | WDI | Watchdog Timer Input. If WDI remains high or low for longer than the watchdog timeout period, the internal watchdog timer expires and the reset output asserts for the reset timeout period. The internal watchdog timer clears whenever a reset is asserted or WDI sees a rising or falling edge. The watchdog timer cannot be disabled. Do not leave WDI unconnected. |
| — | — | — | — | — | EP | Exposed Pad. EP is internally connected to GND. Connect EP to the ground plane to provide a low thermal-resistance path from the IC junction to the PCB. Do not use as the electrical connection to GND. |

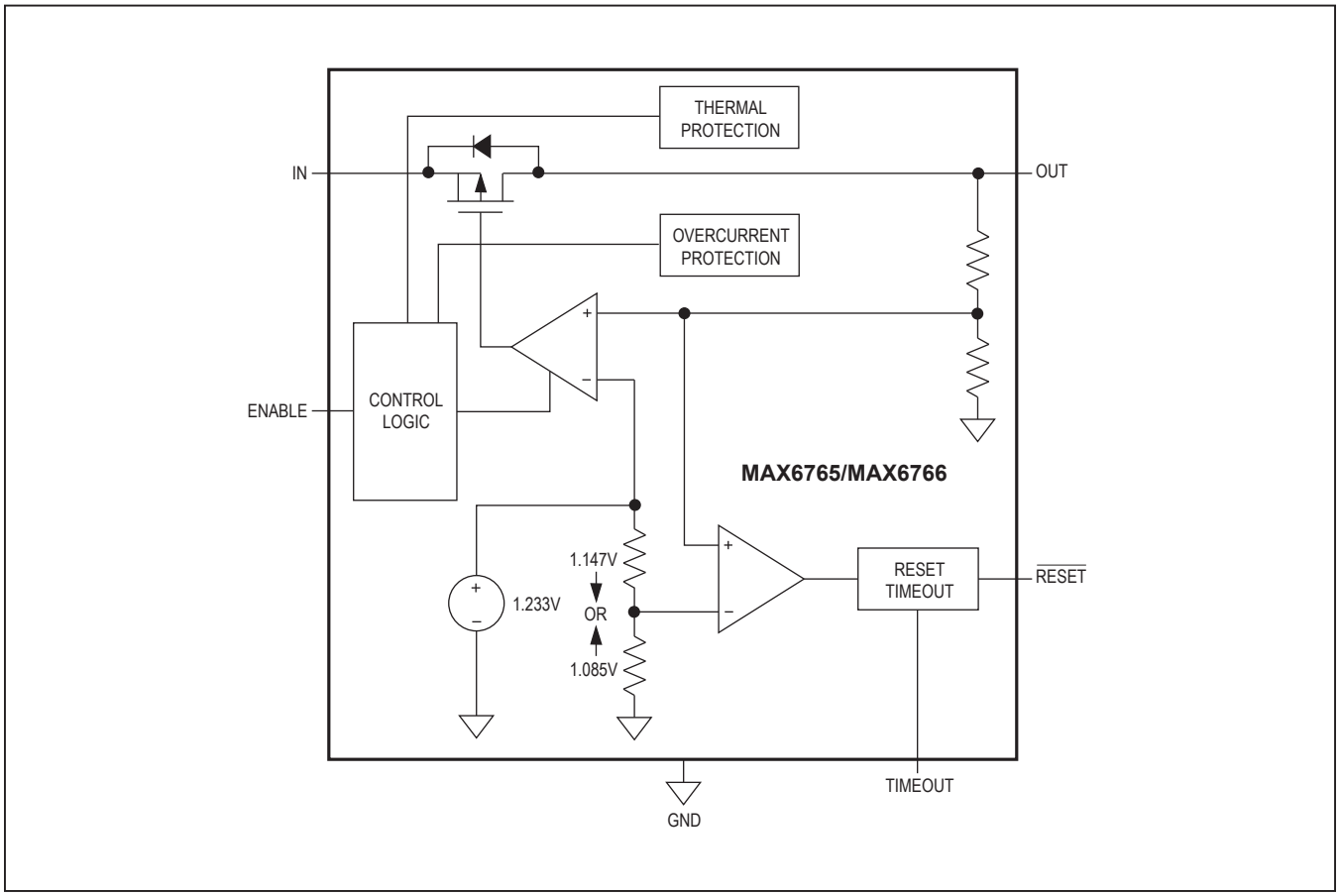
## Detailed Description

The MAX6765–MAX6774B low-quiescent-current, high-voltage linear regulators operate from a 4V to 72V input voltage and deliver more than 100mA of load current. The MAX6765–MAX6774B include an integrated µP reset circuit that monitors the regulator output voltage and asserts a reset output when OUT falls below a threshold limit, and includes an internally fixed or adjustable reset timeout using a capacitor from TIMEOUT to ground. All devices are available in a preset output-voltage option of +1.8V, +2.5V, +3.3V, and +5V.

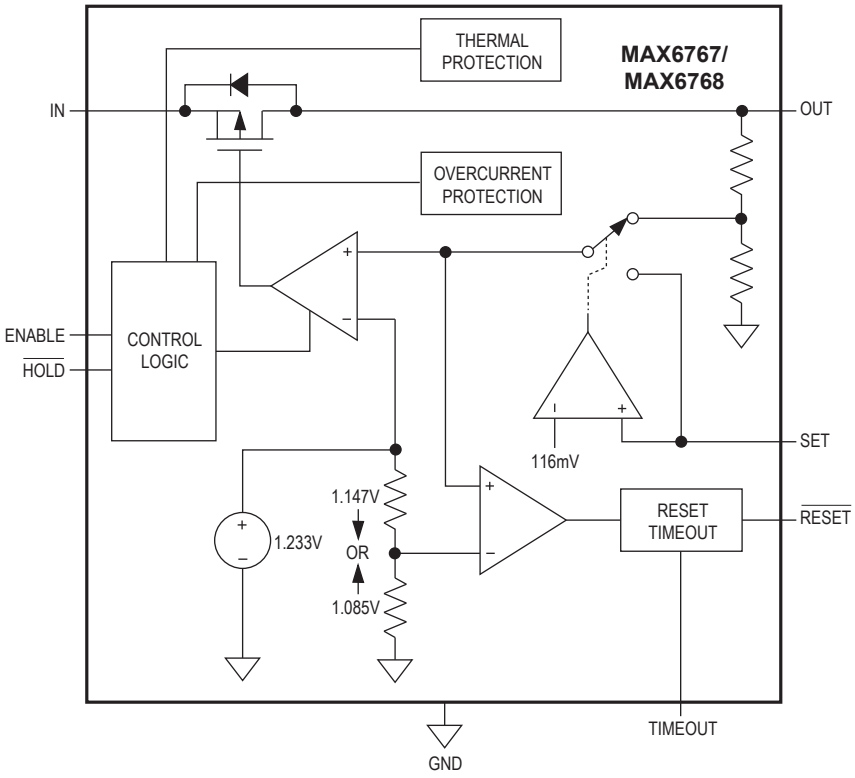
The output voltage of the MAX6767–MAX6774B is adjustable from +1.8V to +11V using a resistive divider at SET. The MAX6773/MAX6774 include a watchdog timer (WDI) with a 1.6s (typ) watchdog timeout period and the MAX6773B/MAX6774B include a watchdog timer with a 50ms (typ) watchdog timeout period. The MAX6769/MAX6770 feature an adjustable reset threshold using a resistive divider between the monitored voltage, RESETIN, and GND; see the *Functional Diagrams*.

The MAX6771/MAX6772 provide dual enable inputs (ENABLE1 and ENABLE2) to turn on and off the regulator either through an ignition switch or a bus transceiver.

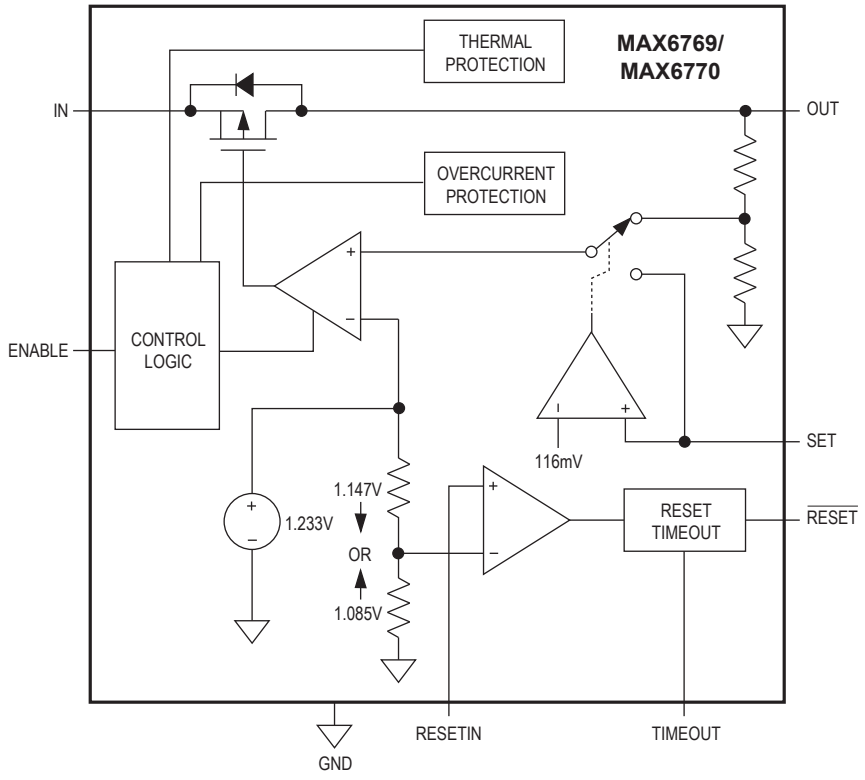
## Functional Diagrams



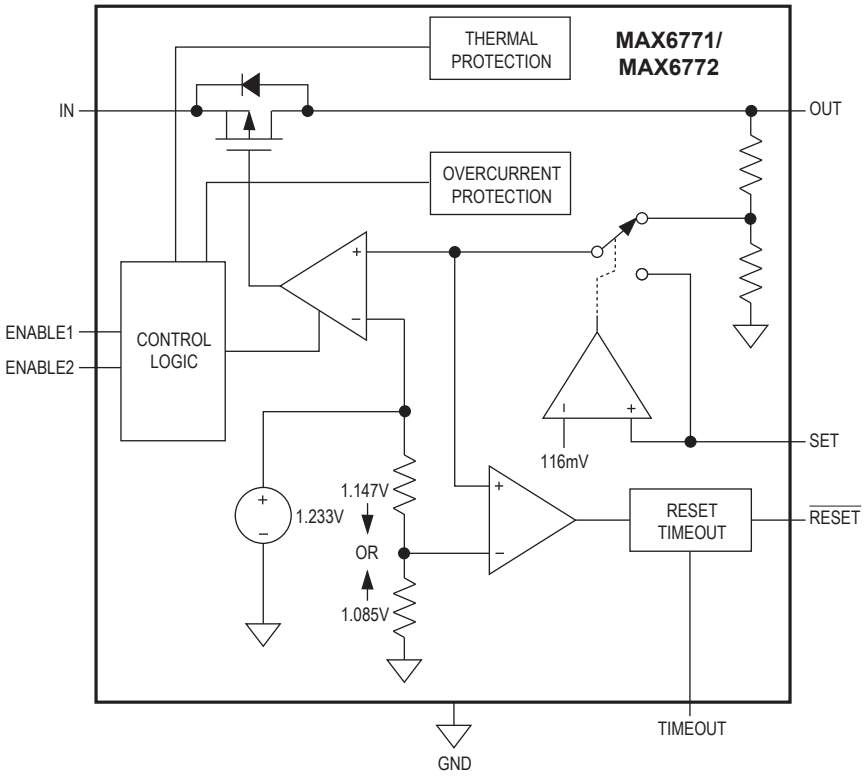
## Functional Diagrams (continued)



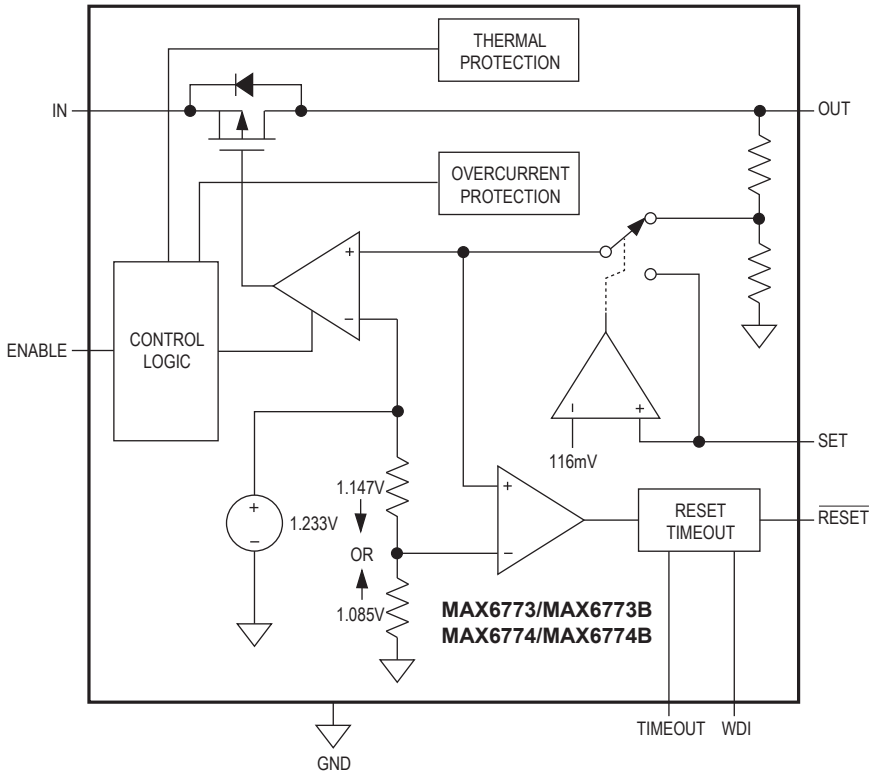
## Functional Diagrams (continued)



## Functional Diagrams (continued)



## Functional Diagrams (continued)



## Regulator

The regulator accepts an input voltage from +4V to +72V. All of the devices feature fixed output-voltage options of +1.8V, +2.5V, +3.3V, and +5V. The MAX6767–MAX6774B feature an adjustable output voltage set with an external resistive-divider network connected between OUT, SET, and GND. See Figure 1.

## Enable and Hold Inputs (MAX6767/MAX6768)

The MAX6767/MAX6768 support two logic inputs, ENABLE (active-high) and $\overline{HOLD}$ (active-low), making these devices "automotive friendly." For example, when the ignition key signal drives ENABLE high, the regulator turns on and remains on even if ENABLE goes low, as long as $\overline{HOLD}$ is forced low and kept low before ENABLE goes low. In this state, releasing $\overline{HOLD}$ turns the regulator output (OUT) off. This feature makes it possible to implement a self-holding circuit without external components. Forcing ENABLE low with $\overline{HOLD}$ high (or unconnected) places the MAX6767/MAX6768 into shutdown mode, drawing 3.3µA (typ) of supply current.

Table 3 shows the state of the regulator output with respect to the voltage level at ENABLE and $\overline{HOLD}$. Connect $\overline{HOLD}$ to OUT or leave it unconnected to allow the ENABLE input to act as a standard enable/shutdown switch for the regulator output (OUT).

## Reset Output

The reset output is typically connected to the reset input of a µP. A µP's reset input starts or restarts the µP in a known state. The MAX6765–MAX6774B supervisory circuits provide the reset logic to prevent code-execution errors during power-up, power-down, and brownout conditions (see the *Typical Application Circuit*). $\overline{RESET}$ changes from high to low whenever the monitored voltage drops below the reset threshold voltages. Once the monitored voltage exceeds its respective reset threshold voltage(s), $\overline{RESET}$ remains low for the reset timeout period, then goes high. See Table 1 and Table 2.

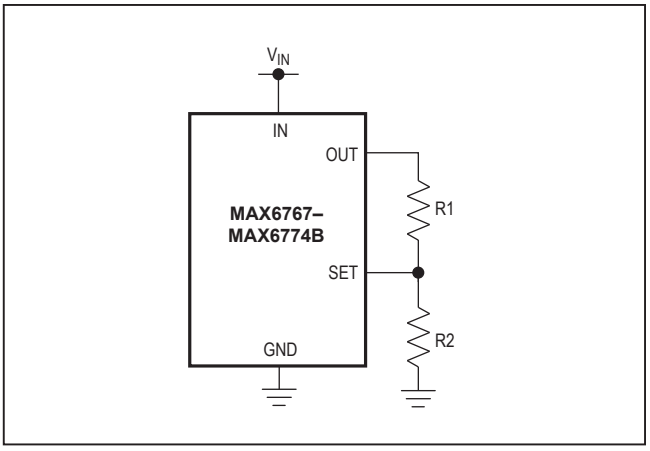



*Figure 1. Setting the Output Voltage Using a Resistive Divider*

## Table 1. Preset Timeout Period

| PART NUMBER SUFFIX (_) | TIMEOUT PERIOD |
|---|---|
| D0 | 75µs |
| D1 | 3.125ms |
| D2 | 12.5ms |
| D3 | 50ms |
| D4 | 200ms |

## RESETIN Threshold (MAX6769/MAX6770)

The MAX6769/MAX6770 monitor the voltage on RESETIN using an adjustable reset threshold ($V_{RESETIN}$) set with an external resistive voltage-divider and the internal reset threshold ($V_{TH}$). See Table 2.

## Table 2. Preset Output Voltage and Reset Threshold

| PART SUFFIX (_) | OUTPUT VOLTAGE (V) | RESET THRESHOLD (V) (ALL VERSIONS EXCEPT MAX6769/MAX6770) | RESETIN THRESHOLD (V) (MAX6769/MAX6770 ONLY) |
|---|---|---|---|
| L | 5 | 4.625 | 1.147 |
| M | 5 | 4.375 | 1.085 |
| T | 3.3 | 3.353 | 1.147 |
| S | 3.3 | 2.888 | 1.085 |
| Z | 2.5 | 2.313 | 1.147 |
| Y | 2.5 | 2.188 | 1.085 |
| W | 1.8 | 1.665 | 1.147 |
| V | 1.8 | 1.575 | 1.085 |

## Table 3. ENABLE/$\overline{\text{HOLD}}$ Truth Table/State Table

| OPERATING STATE | ENABLE | $\overline{\text{HOLD}}$ | REGULATOR OUTPUT | COMMENT |
|---|---|---|---|---|
| Initial State | Low | Don't care | Off | ENABLE is pulled to GND through an internal pulldown. $\overline{\text{HOLD}}$ is high impedance (pulled up to OUT). Regulator output is disabled. |
| Turn-On State | High | Don't care | On | ENABLE is externally driven high turning the regulator output on. $\overline{\text{HOLD}}$ is pulled up by OUT. |
| Hold Setup State | High | Low | On | $\overline{\text{HOLD}}$ is externally pulled low while ENABLE remains high (latches $\overline{\text{HOLD}}$ state). |
| Hold State | Low | Low | On | ENABLE is driven low (or pulled low by an internal pulldown). $\overline{\text{HOLD}}$ remains externally pulled low keeping the regulator output on. |
| Off-State | Low | High (pulled high) | Off | $\overline{\text{HOLD}}$ is driven high (or pulled high by an internal pullup) while ENABLE is low. Regulator output is shut off and ENABLE/$\overline{\text{HOLD}}$ logic returns to the initial state. |

### Watchdog Timer (MAX6773/MAX6773B/MAX6774/MAX6774B)

The MAX6773/MAX6774 include a watchdog timer that asserts $\overline{\text{RESET}}$ if the watchdog input (WDI) does not toggle within the watchdog timeout period, $t_{WD}$ (1.6s (typ) for the MAX6773/MAX6774 and 50ms (typ) for the MAX6773B/MAX6774B). $\overline{\text{RESET}}$ remains low for the reset timeout period, $t_{RP}$. If the watchdog is not updated for lengthy periods of time, the reset output appears as a pulse train, asserted for the reset timeout period and deasserted for the watchdog timeout period, until WDI is toggled again. When $\overline{\text{RESET}}$ asserts, it stays low for the entire reset timeout period ignoring any WDI transitions. To prevent the watchdog from asserting $\overline{\text{RESET}}$, toggle WDI with a valid rising or falling edge prior to $t_{WD}$ (min). The watchdog counter clears when WDI toggles prior to $t_{WD}$ or when $\overline{\text{RESET}}$ asserts. The watchdog resumes counting after $\overline{\text{RESET}}$ deasserts. The watchdog timer cannot be disabled.

### Thermal Protection

When the junction temperature exceeds $T_J$ = +160°C (typ), an internal thermal sensor signals the shutdown logic that turns off the pass transistor and allows the IC to cool. The thermal sensor turns the pass transistor on again after the IC's junction temperature cools by 20°C (typ), resulting in a cycled output during continuous thermal-overload conditions. Thermal protection protects the MAX6765–MAX6774B in the event of a fault condition. Never exceed the absolute maximum junction temperature rating of $T_J$ = +150°C. See Figures 3 and 4 for the safe operating area.

## Applications Information

### Output-Voltage Selection

The MAX6767–MAX6774B feature dual-mode operation and operate in either a preset or adjustable voltage mode. In preset voltage mode, internal trimmed feedback resistors set the internal linear regulator to +1.8V, +2.5V, +3.3V, or +5V (see Table 2). Select preset-voltage mode by connecting SET to ground. In adjustable mode, select an output voltage between +1.8V and +11V using two external resistors connected as a voltage-divider to SET (see Figure 1). Set the output voltage using the following equation:

$$V_{OUT} = V_{SET} (1 + R1/R2)$$

where $V_{SET}$ = 1.233V and the recommended value for R2 is 50kΩ (maximum 100kΩ).

### RESETIN Threshold Selection

The MAX6769/MAX6770 feature an adjustable reset threshold to monitor the voltage on RESETIN using a resistive divider between the monitored voltage, RESETIN and GND. See Figure 2. Use the following formula to set the desired reset threshold:

$$V_{MON} = V_{TH} (1 + R3/R4)$$

where $V_{TH}$ is 1.085V for the M/S/Y/V versions and 1.147V for the L/T/Z/W versions.

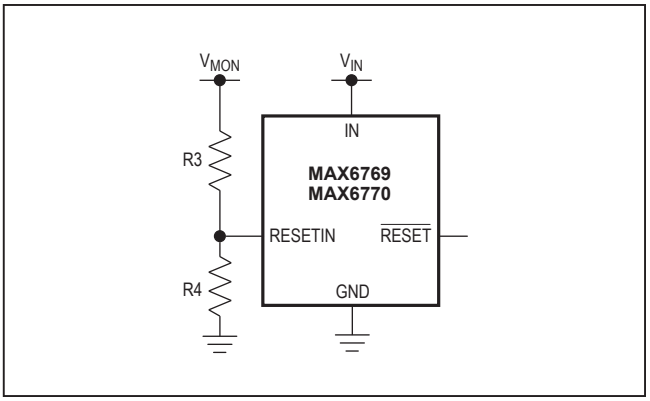



*Figure 2. RESETIN Threshold Selection*

## Available Output-Current Calculation

The MAX6765–MAX6774B provide up to 100mA of load current. Package power dissipation limits the amount of output current available for a given input/output voltage and ambient temperature. Figures 3 and 4 depict the maximum power dissipation curve for the MAX6765/MAX6766 and MAX6767–MAX6774B, respectively. The graph assumes that the exposed metal pad of the device package is soldered to a solid $1in^2$ section of 2oz. PCB copper (JESD51-3 AND JESD51-5). Use Figure 4 to determine the allowable package dissipation for a given ambient temperature. Alternately, use the following formula to calculate the allowable package dissipation:

$PD_{MAX}$ = Max. Power Dissip = 1.951W, for $T_A \le +70°C$

$PD_{MAX}$ = Max. Power Dissip = [1.9W - 0.0244W x ($T_A$ - 70°C)], for +70°C < $T_A \le$ +125°C

where 0.0244W is the MAX6767–MAX6774B package thermal derating in W/°C and $T_A$ is the ambient temperature in °C, under the same conditions used for Figure 4.

After determining the allowable package dissipation, calculate the maximum output current using the following formula:

$PD < PD_{MAX}$ where $PD = [(V_{IN} - V_{OUT}) \times I_{OUT}]$

Also, $I_{OUT}$ should be ≤ 100mA in any case.

## Selecting Timeout Capacitor

The reset timeout period is adjustable to accommodate a variety of µP applications. Adjust the reset timeout period by connecting a capacitor between TIMEOUT and GND.

$t_{RP} = C_{TIMEOUT} \times 1.22 \times 10^6 \Omega$ (L/M/T/S options)

$t_{RP} = C_{TIMEOUT} \times 1.17 \times 10^6 \Omega$ (V/W/Y/Z options)

where $t_{RP}$ is in seconds and $C_{TIMEOUT}$ is in Farads.

Connect TIMEOUT to OUT to select the internally fixed timeout period. $C_{TIMEOUT}$ must be a low-leakage (< 10nA) type capacitor. Ceramic capacitors are recommended; do not use capacitor values lower than 100pF to avoid the influence of parasitic capacitances.

## Capacitor Selection and Regulator Stability

For stable operation over the full temperature range and with load currents up to 100mA, use a 10µF (min) output capacitor with an ESR < 0.5Ω. To reduce noise and improve load-transient response, stability, and power-supply rejection, use larger output-capacitor values. Some ceramic dielectrics exhibit large capacitance and ESR variation with temperature. For dielectric capacitors such as Z5U and Y5V, use more capacitance to ensure stability at low temperatures. With X7R or X5R dielectrics, 10µF should be sufficient at all operating temperatures. For higher-ESR tantalum capacitors, use larger capacitor values to maintain stability. To improve power-supply rejection and transient response, use a larger capacitor than the minimum 0.1µF capacitor between IN and GND.

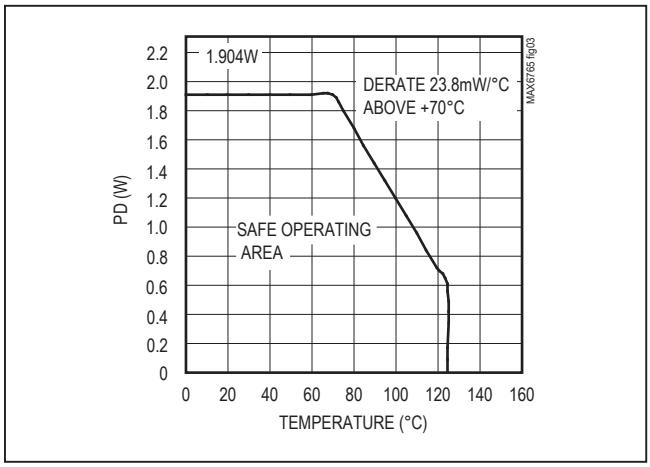



*Figure 3. Maximum Power Dissipation vs. Temperature (MAX6765/MAX6766)*

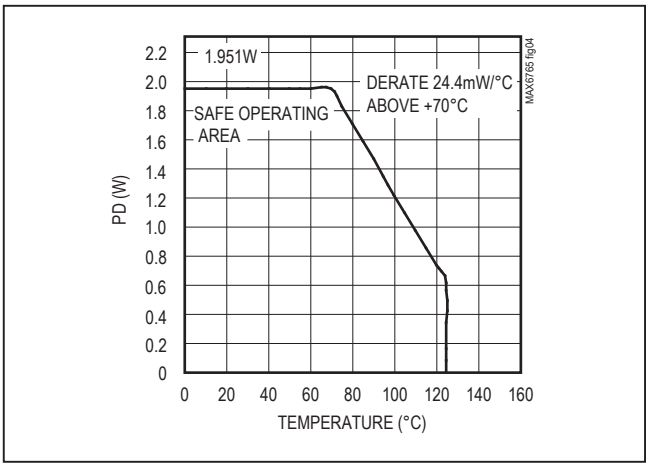



*Figure 4. Maximum Power Dissipation vs. Temperature (MAX6767–MAX6774B)*

### Ensuring a Valid $\overline{\text{RESET}}$ Output Down to $V_{IN}$ = 0V (MAX6766/MAX6768/MAX6770/ MAX6772/MAX6774/MAX6774B)

When $V_{IN}$ falls below 1V, $\overline{\text{RESET}}$ current-sinking capabilities decline drastically. High-impedance CMOS-logic inputs connected to $\overline{\text{RESET}}$ can drift to undetermined voltages. This presents no problems in most applications, since most µPs and other circuitry do not operate with supply voltages below 1V. In applications where $\overline{\text{RESET}}$ must be valid down to 0V, adding a pulldown resistor between $\overline{\text{RESET}}$ and ground sinks any stray leakage currents, holding $\overline{\text{RESET}}$ low (Figure 5). The value of the pulldown resistor is not critical; 100kΩ is large enough not to load $\overline{\text{RESET}}$ and small enough to pull $\overline{\text{RESET}}$ to ground. Open-drain $\overline{\text{RESET}}$ versions are not recommended for applications requiring valid logic for $V_{IN}$ down to 0V.

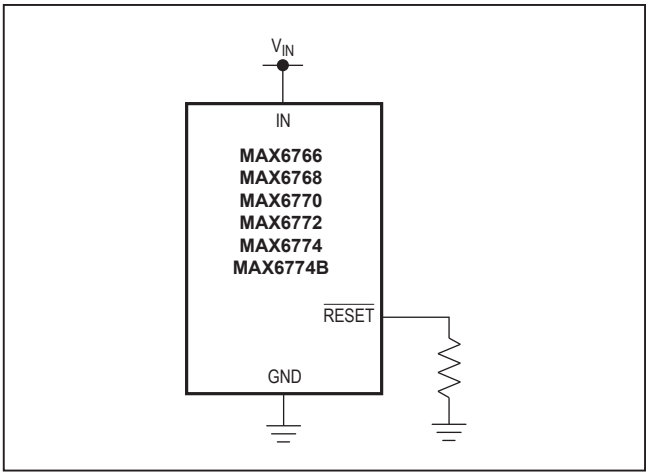



*Figure 5. Ensuring $\overline{\text{RESET}}$ Valid to $V_{IN}$ = 0V*

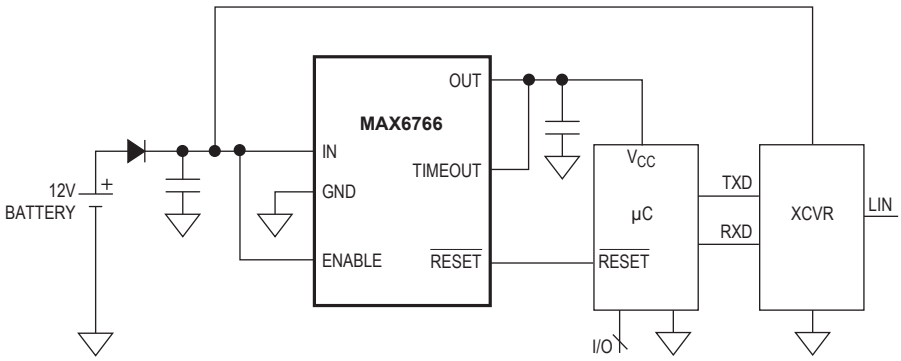
## Table 4. Standard Version Part Numbers

| PART | OUTPUT VOLTAGE (V) | $\overline{\text{RESET}}$ TIMEOUT PERIOD (ms) | RESET THRESHOLD (V) | RESETIN THRESHOLD (V) | TOP MARK |
|---|---|---|---|---|---|
| MAX6765TTLD2+T | 5 | 12.5 | 4.625 | — | +AQB |
| MAX6765TTLD2/V+T | 5 | 12.5 | 4.625 | — | +AVC |
| MAX6765TTSD2+T | 3.3 | 12.5 | 2.888 | — | +AQL |
| MAX6765TTSD2/V+T | 3.3 | 12.5 | 2.888 | — | +AUQ |
| MAX6766TTLD2+T | 5 | 12.5 | 4.625 | — | +ARO |
| MAX6766TTSD2+T | 3.3 | 12.5 | 2.888 | — | +ARZ |
| MAX6767TALD2+T | 5 | 12.5 | 4.625 | — | +AVI |
| MAX6767TALD2/V+T | 5 | 12.5 | 4.625 | — | +BRK |
| MAX6767TASD2+T | 3.3 | 12.5 | 2.888 | — | +AVS |
| MAX6768TALD2+T | 5 | 12.5 | 4.625 | — | +AVZ |
| MAX6768TASD2+T | 3.3 | 12.5 | 2.888 | — | +AXE |
| MAX6769TALD2+T | 5 | 12.5 | — | 1.147 | +AYH |
| MAX6769TASD2+T | 3.3 | 12.5 | — | 1.085 | +AYQ |
| MAX6769TALD2/V+T | 5 | 12.5 | — | 1.147 | +BQF |
| MAX6770TALD2+T | 5 | 12.5 | — | 1.147 | +AZS |
| MAX6770TASD2+T | 3.3 | 12.5 | — | 1.085 | +BAC |
| MAX6771TALD2+T | 5 | 12.5 | 4.625 | — | +BEG |
| MAX6771TASD2+T | 3.3 | 12.5 | 2.888 | — | +BEQ |
| MAX6772TALD2+T | 5 | 12.5 | 4.625 | — | +APY |
| MAX6772TASD2+T | 3.3 | 12.5 | 2.888 | — | +BGC |
| MAX6773TALD2+T | 5 | 12.5 | 4.625 | — | +BBG |
| MAX6773TASD2+T | 3.3 | 12.5 | 2.888 | — | +AQE |
| MAX6773BTALD2+T | 5 | 12.5 | 4.625 | — | +BHK |
| MAX6773BTASD2+T | 3.3 | 12.5 | 2.888 | — | +BHU |
| MAX6773BTASD2/V+T | 3.3 | 12.5 | 2.888 | — | +BNN |
| MAX6774TALD2+T | 5 | 12.5 | 4.625 | — | +BCS |
| MAX6774TASD2+T | 3.3 | 12.5 | 2.888 | — | +BDC |
| MAX6774BTALD2+T | 5 | 12.5 | 4.625 | — | +BIY |
| MAX6774BTASD2+T | 3.3 | 12.5 | 2.888 | — | +BJI |

## Selector Guide

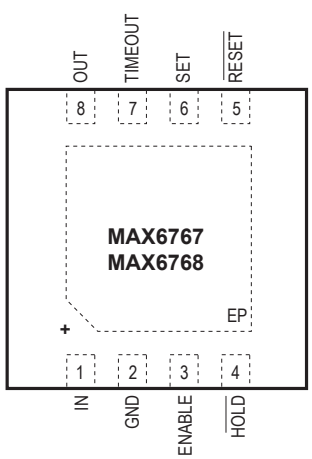
| PART | $\overline{\text{RESET}}$ OUTPUT | TYPICAL WATCHDOG TIMEOUT | OUTPUT VOLTAGE | RESETIN THRESHOLD | ENABLE INPUTS | HOLD INPUT |
|---|---|---|---|---|---|---|
| MAX6765 | Open drain | — | Fixed | — | Single | — |
| MAX6766 | Push-pull | — | Fixed | — | Single | — |
| MAX6767 | Open drain | — | Fixed/Adj | — | Single | √ |
| MAX6768 | Push-pull | — | Fixed/Adj | — | Single | √ |
| MAX6769 | Open drain | — | Fixed/Adj | √ | Single | — |
| MAX6770 | Push-pull | — | Fixed/Adj | √ | Single | — |
| MAX6771 | Open drain | — | Fixed/Adj | — | Dual | — |
| MAX6772 | Push-pull | — | Fixed/Adj | — | Dual | — |
| MAX6773 | Open drain | 1.6s | Fixed/Adj | — | Single | — |
| MAX6773B | Open drain | 50ms | Fixed/Adj | — | Single | — |
| MAX6774 | Push-pull | 1.6s | Fixed/Adj | — | Single | — |
| MAX6774B | Push-pull | 50ms | Fixed/Adj | — | Single | — |

## Typical Application Circuit



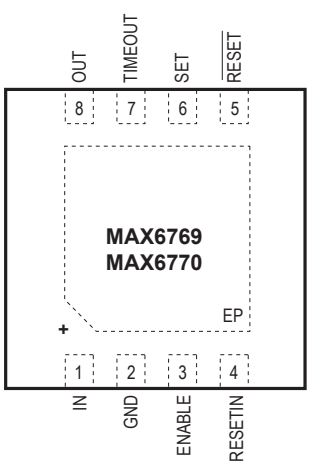
## Pin Configurations (continued)

TOP VIEW



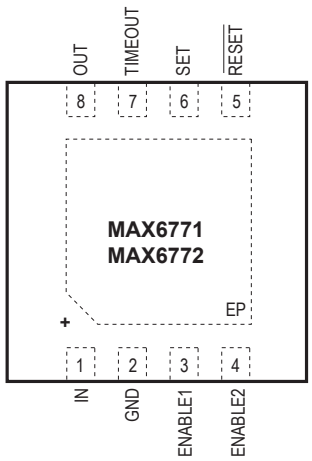

TDFN

TOP VIEW



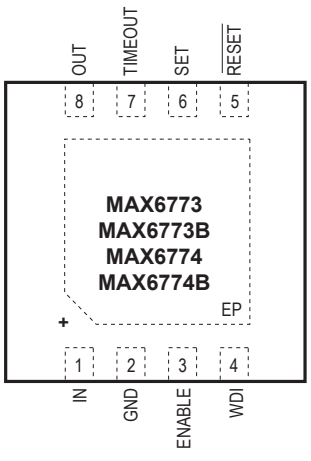

TDFN

TOP VIEW




TDFN

TOP VIEW




TDFN

## Ordering Information (continued)

| PART | TEMP RANGE | PIN-PACKAGE |
|---|---|---|
| **MAX6766**TT_D_+ | -40°C to +125°C | 8 TDFN-EP* |
| **MAX6767**TA_D_/V+ | -40°C to +125°C | 8 TDFN-EP* |
| **MAX6768**TA_D_+ | -40°C to +125°C | 8 TDFN-EP* |
| **MAX6769**TA_D_+ | -40°C to +125°C | 8 TDFN-EP* |
| **MAX6769**TA_D_/V+ | -40°C to +125°C | 8 TDFN-EP* |
| **MAX6770**TA_D_+ | -40°C to +125°C | 8 TDFN-EP* |
| **MAX6771**TA_D_+ | -40°C to +125°C | 8 TDFN-EP* |
| **MAX6772**TA_D_+ | -40°C to +125°C | 8 TDFN-EP* |
| **MAX6773**TA_D_/V+ | -40°C to +125°C | 8 TDFN-EP* |
| MAX6773BTA_D_/V+ | -40°C to +125°C | 8 TDFN-EP* |
| **MAX6774**TA_D_+ | -40°C to +125°C | 8 TDFN-EP* |
| MAX6774BTA_D_+ | -40°C to +125°C | 8 TDFN-EP* |

*The first "_" is a placeholder for the voltage output and reset threshold. The 2nd "_" designates the fixed reset-timeout option. See Tables 1 and 2 for details. For example, the MAX6765TTLD4 has a 5V output, a reset threshold of 4.65V, and a 200ms typical reset timeout.*

*+Denotes a lead(Pb)-free/RoHS-compliant package.*

*/V denotes an automotive qualified part.*

**EP = Exposed pad.*

*For tape-and-reel orders add a "T" after the "+" symbol to complete the part number. Tape-and-reel orders are available in 2.5k increments. Nonstandard versions require a 10k minimum order quantity.*

## Chip Information

PROCESS: BiCMOS

## Revision History

| REVISION NUMBER | REVISION DATE | DESCRIPTION | PAGES CHANGED |
|---|---|---|---|
| 0 | 10/06 | Initial release | — |
| 1 | 1/07 | Introduced MAX6765 and MAX6766 | 1, 21, 23 |
| 2 | 7/07 | Added the MAX6773B and MAX6774D to data sheet. Updated *Features*, *General Description*, *Ordering Information*, *Functional Diagrams*, *Table 4*, *Selector Guide*, *Watchdog Timer section*, *and Pin Configurations*. | 1, 4, 8, 9, 14, 16, 18–23 |
| 3 | 9/07 | Revised *Typical Operating Characteristics* | 7 |
| 4 | 6/10 | Added /V to the MAX6765TT_D_+ | 1 |
| 5 | 10/11 | Added /V to the MAX6773TA_D_+; added Timeout ramp threshold to *Electrical Characteristics* table. Changed $t_{RP}$ formula in *Selecting Timeout Capacitor* section. | 4, 17, 21 |
| 6 | 3/12 | Added /V to the MAX6769TA_D_/V+ | 21 |
| 7 | 10/12 | Added /V to the MAX6767TA_D_/V+ | 21 |
| 8 | 4/13 | Updated Tables 2 and 4 | 15, 18 |
| 9 | 8/17 | Added AEC-Q100 to *Features* section and updated Table 4 | 1, 18 |
| 10 | 11/18 | Updated *Package Information* section | 2, 22 |

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## Maxim Integrated:

MAX6765TTLD0+T MAX6765TTLD1+T MAX6765TTLD2+T MAX6765TTLD3+T MAX6765TTLD4+T
MAX6765TTMD0+T MAX6765TTMD1+T MAX6765TTMD2+T MAX6765TTMD3+T MAX6765TTMD4+T
MAX6765TTSD0+T MAX6765TTSD1+T MAX6765TTSD2+T MAX6765TTSD4+T MAX6765TTTD0+T
MAX6765TTTD1+T MAX6765TTTD2+T MAX6765TTTD3+T MAX6765TTTD4+T MAX6765TTVD0+T
MAX6765TTVD1+T MAX6765TTVD2+T MAX6765TTVD3+T MAX6765TTVD4+T MAX6765TTWD0+T
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