Dual, 10-Bit, 40MHz Current/Voltage Alternate-Phase Output DACs

ABSOLUTE MAXIMUM RATINGS

AV_{DD}, DV_{DD} to AGND, DGND .....-0.3V to +6V
Digital Inputs to DGND.....-0.3V to +6V
OUT1P, OUT1N, OUT2P, OUT2N, CREF1, CREF2 to AGND .....-0.3V to +6V
V_{REF} to AGND .....-0.3V to +6V
AGND to DGND.....-0.3V to +0.3V
AV_{DD} to DV_{DD}..... ±3.3V
Maximum Current into Any Pin.....50mA
Continuous Power Dissipation (T_A = +70°C)
28-Pin QSOP (derate 9.00mW/°C above +70°C)..... 725mW
Operating Temperature Ranges
MAX518_BEEI.....-40°C to +85°C
Storage Temperature Range .....-65°C to +150°C
Lead Temperature (soldering, 10s) ..... +300°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

(AV_{DD} = DV_{DD} = +3V ±10%, AGND = DGND = 0, f_{CLK} = 40MHz, I_{FS} = 1mA, 400Ω differential output, C_L = 5pF, T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are at T_A = +25°C.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
STATIC PERFORMANCE							
Resolution	N			10			Bits
Integral Nonlinearity	INL			-2	±0.5	+2	LSB
Differential Nonlinearity	DNL	Guaranteed monotonic		-1	±0.5	+1	LSB
Zero-Scale Error		MAX5182		-2		+2	LSB
		MAX5185		-8		+8	
Full-Scale Error		(Note 1)		-40	±15	+40	LSB
DYNAMIC PERFORMANCE							
Output Settling Time		To ±0.5LSB error band			25		ns
Glitch Impulse					10		pVs
Spurious-Free Dynamic Range to Nyquist	SFDR	f_{CLK} = 40MHz	f_{OUT} = 550kHz		72		dBc
			f_{OUT} = 2.2MHz, T_A = +25°C	57	70		
Total Harmonic Distortion to Nyquist	THD	f_{CLK} = 40MHz	f_{OUT} = 550kHz		-70		dB
			f_{OUT} = 2.2MHz, T_A = +25°C		-68	-63	
Signal-to-Noise Ratio to Nyquist	SNR	f_{CLK} = 40MHz	f_{OUT} = 550kHz		61		dB
			f_{OUT} = 2.2MHz, T_A = +25°C	56	59		
DAC-to-DAC Ouput Isolation		f_{OUT} = 2.2MHz			-60		dB
Clock and Data Feedthrough		All 0s to all 1s			50		nVs
Output Noise					10		pA/√Hz
Gain Mismatch Between DAC Outputs		f_{OUT} = 2.2MHz, T_A = +25°C			±0.5	±1	% FSR
ANALOG OUTPUT							
Full-Scale Output Voltage	V_{FS}				400		mV
Voltage Compliance of Output				-0.3		0.8	V
Output Leakage Current		DACEN = 0, MAX5182 only		-1		1	µA
Full-Scale Output Current	I_{FS}	MAX5182 only		0.5	1	1.5	mA
DAC External Output Resistor Load	R_L	MAX5182 only			400		Ω

ELECTRICAL CHARACTERISTICS (continued)

(AV_{DD} = DV_{DD} = +3V ±10%, AGND = DGND = 0, f_{CLK} = 40MHz, I_{FS} = 1mA, 400Ω differential output, C_L = 5pF, T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are at T_A = +25°C.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
REFERENCE						
Output Voltage Range	V_{REF}		2.7	1.2	1.28	V
Output Voltage Temperature Drift	TCV_{REF}			50		ppm/°C
Reference Output Drive Capability	I_{REFOUT}			10		µA
Reference Supply Rejection				0.5		mV/V
Current Gain (I_{FS} / I_{REF})				8		mA/mA
POWER REQUIREMENTS						
Analog Power-Supply Voltage	AV_{DD}		2.7		3.3	V
Analog Supply Current	I_{AVDD}	PD = 0, DACEN = 1, digital inputs at 0 or DV_{DD}		2.7	5.0	mA
Digital Power-Supply Voltage	DV_{DD}		2.7		3.3	V
Digital Supply Current	I_{DVDD}	PD = 0, DACEN = 1, digital inputs at 0 or DV_{DD}		4.2	5.0	mA
Standby Current	$I_{STANDBY}$	PD = 0, DACEN = 0, digital inputs at 0 or DV_{DD}		1.0	1.5	mA
Shutdown Current	I_{SHDN}	PD = 1, DACEN = X, digital inputs at 0 or DV_{DD} (X = don't care)		0.5	1	µA
LOGIC INPUTS AND OUTPUTS						
Digital Input Voltage High	V_{IH}		2			V
Digital Input Voltage Low	V_{IL}				0.8	V
Digital Input Current	I_{IN}	V_{IN} = 0 or DV_{DD}			±1	µA
Digital Input Capacitance	C_{IN}			10		pF
TIMING CHARACTERISTICS						
DAC1 DATA to CLK Rise Setup Time	t_{DS1}		10			ns
DAC2 DATA to CLK Fall Setup Time	t_{DS2}		10			ns
DAC1 CLK Rise to DATA Hold Time	t_{DH1}		0			ns
DAC2 CLK Fall to DATA Hold Time	t_{DH2}		0			ns
$\overline{CS}$ Fall to CLK Rise Time				5		ns
$\overline{CS}$ Fall to CLK Fall Time				5		ns
DACEN Rise Time to $V_{OUT\_}$				0.5		µs
PD Fall Time to $V_{OUT\_}$				50		µs
Clock Period	t_{CLK}		25			ns
Clock High Time	t_{CH}		10		0	ns
Clock Low Time	t_{CL}		10			ns

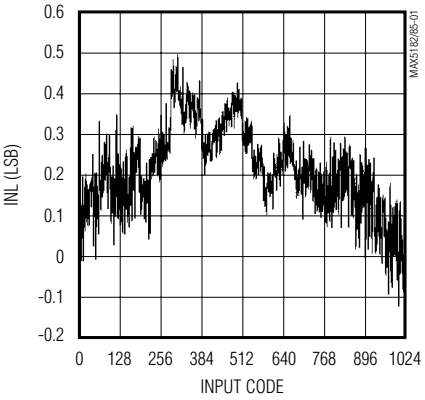
Note 1: Excludes reference and reference resistor (MAX5185) tolerance.

Dual, 10-Bit, 40MHz Current/Voltage Alternate-Phase Output DACs

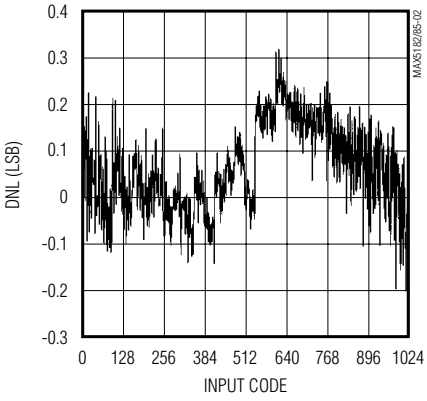
Typical Operating Characteristics

(AV_{DD} = DV_{DD} = +3V, AGND = DGND = 0, 400Ω differential output, I_{FS} = 1mA, C_L = 5pF, T_A = +25°C, unless otherwise noted.)

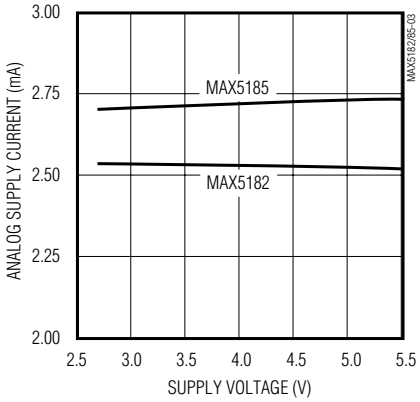
INTEGRAL NONLINEARITY vs. INPUT CODE



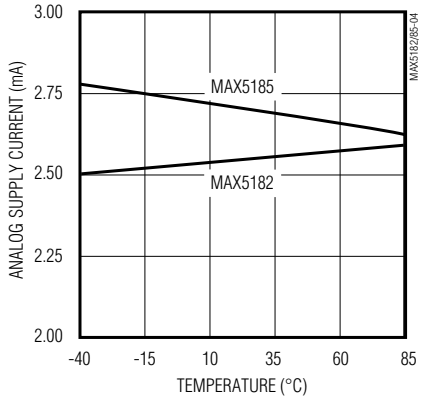
DIFFERENTIAL NONLINEARITY vs. INPUT CODE



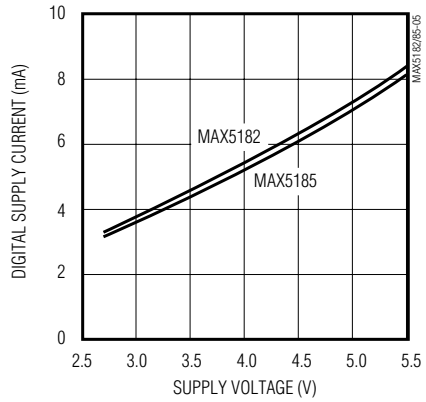
ANALOG SUPPLY CURRENT vs. SUPPLY VOLTAGE



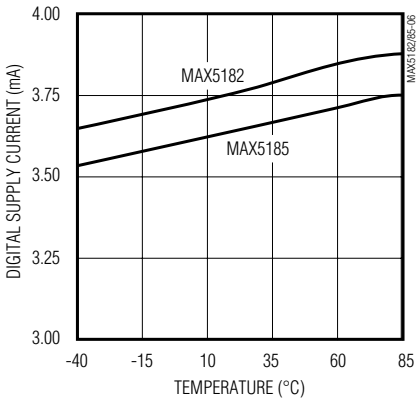
ANALOG SUPPLY CURRENT vs. TEMPERATURE



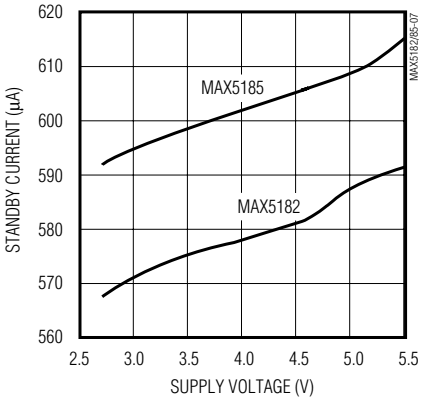
DIGITAL SUPPLY CURRENT vs. SUPPLY VOLTAGE



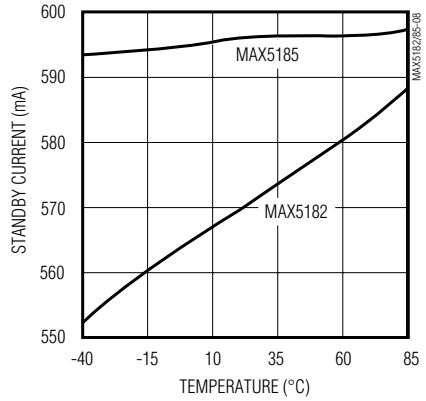
DIGITAL SUPPLY CURRENT vs. TEMPERATURE



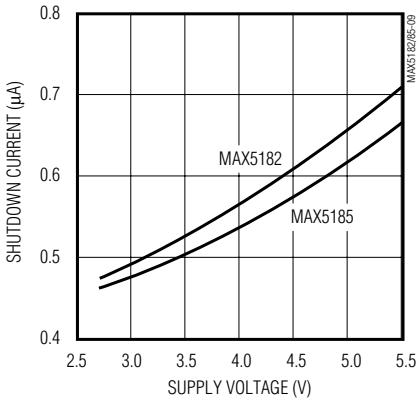
STANDBY CURRENT vs. SUPPLY VOLTAGE



MAX5182/MAX5185 STANDBY CURRENT vs. TEMPERATURE



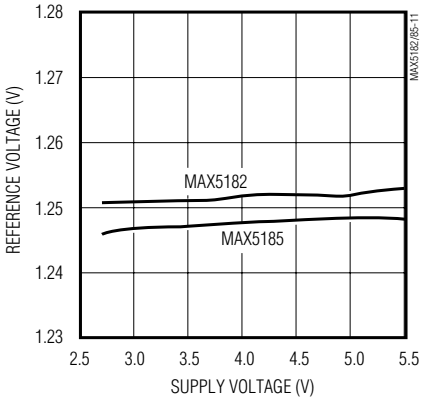
SHUTDOWN CURRENT vs. SUPPLY VOLTAGE



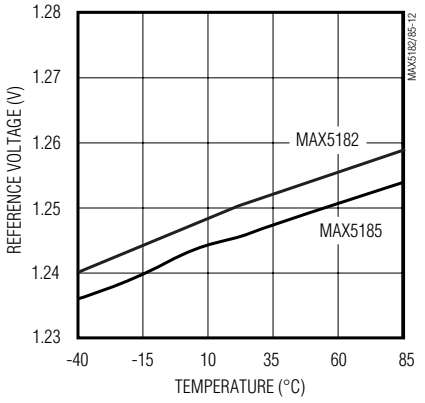
Typical Operating Characteristics (continued)

(AV_{DD} = DV_{DD} = +3V, AGND = DGND = 0, 400Ω differential output, I_{FS} = 1mA, C_L = 5pF, T_A = +25°C, unless otherwise noted.)

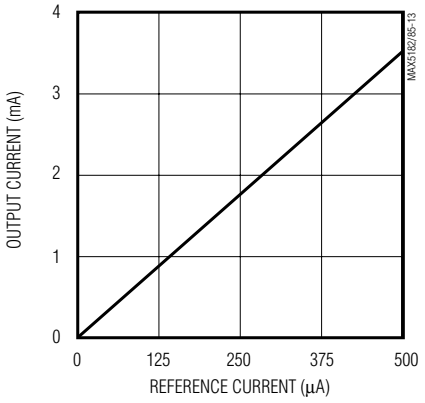
INTERNAL REFERENCE VOLTAGE vs. SUPPLY VOLTAGE



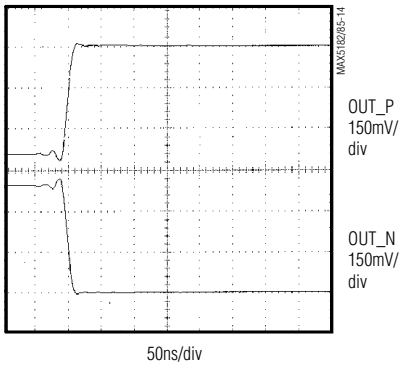
INTERNAL REFERENCE VOLTAGE vs. TEMPERATURE



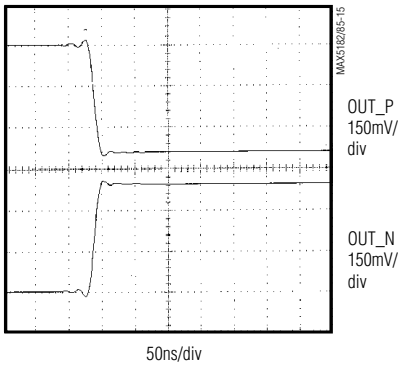
OUTPUT CURRENT vs. REFERENCE CURRENT



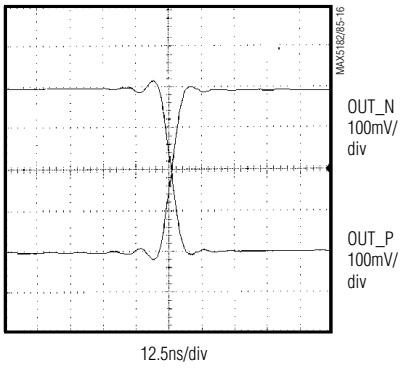
DYNAMIC RESPONSE RISE TIME



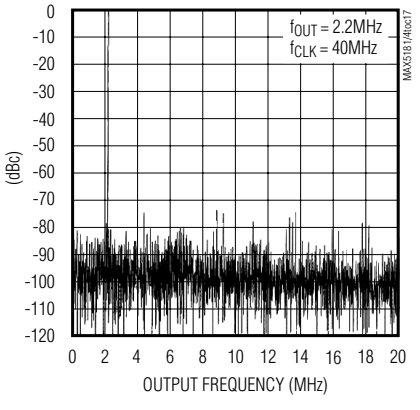
DYNAMIC RESPONSE FALL TIME



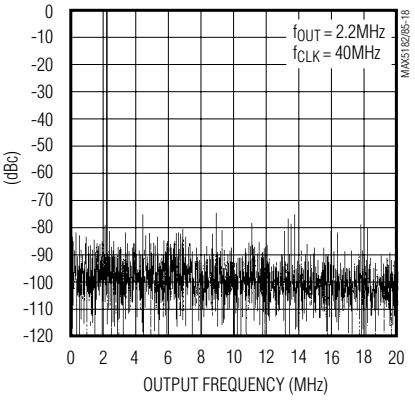
SETTLING TIME



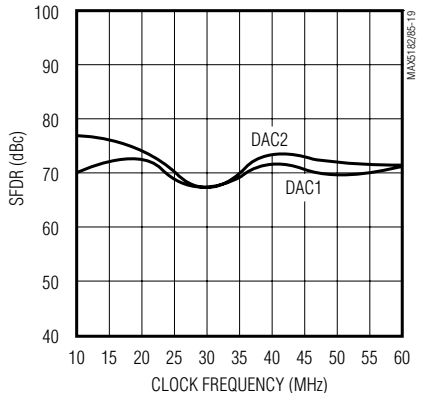
FFT PLOT, DAC1



FFT PLOT, DAC2



SPURIOUS-FREE DYNAMIC RANGE vs. CLOCK FREQUENCY

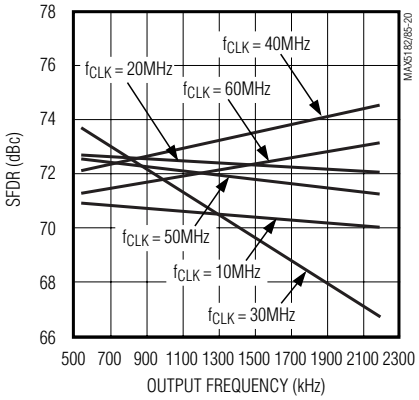


Dual, 10-Bit, 40MHz Current/Voltage Alternate-Phase Output DACs

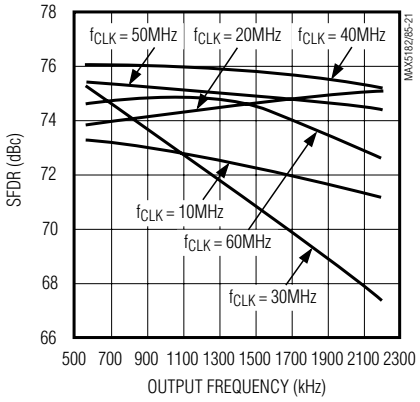
Typical Operating Characteristics (continued)

(AV_{DD} = DV_{DD} = +3V, AGND = DGND = 0, 400Ω differential output, I_{FS} = 1mA, C_L = 5pF, T_A = +25°C, unless otherwise noted.)

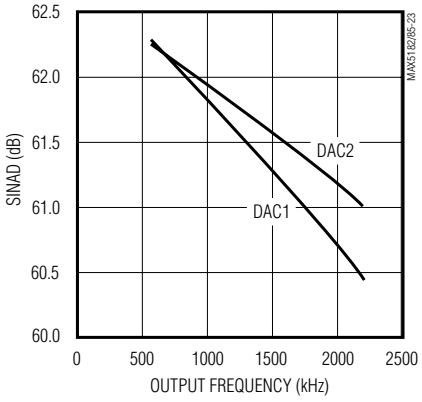
SPURIOUS-FREE DYNAMIC RANGE vs. OUTPUT FREQUENCY AND CLOCK FREQUENCY, DAC1



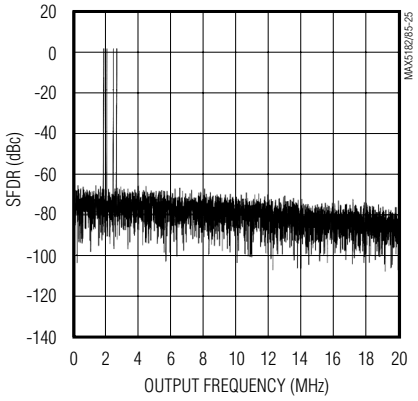
SPURIOUS-FREE DYNAMIC RANGE vs. OUTPUT FREQUENCY AND CLOCK FREQUENCY, DAC2



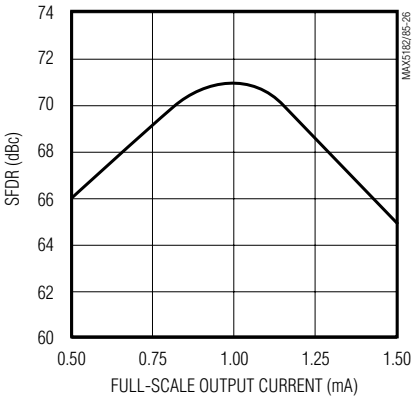
SIGNAL-TO-NOISE PLUS DISTORTION vs. OUTPUT FREQUENCY



MULTITONE SPURIOUS-FREE DYNAMIC RANGE vs. OUTPUT FREQUENCY



SPURIOUS-FREE DYNAMIC RANGE vs. FULL-SCALE OUTPUT CURRENT



Pin Description

PIN	NAME	FUNCTION
1	CREF1	Reference Bias Bypass, DAC1
2	OUT1P	Positive Analog Output, DAC1. Current output for MAX5182; voltage output for MAX5185.
3	OUT1N	Negative Analog Output, DAC1. Current output for MAX5182; voltage output for MAX5185.
4	AGND	Analog Ground
5	AV_{DD}	Analog Positive Supply, +2.7V to +3.3V
6	DACEN	DAC Enable, Digital Input 0: Enter DAC standby mode with PD = DGND 1: Power-up DAC with PD = DGND X: Enter shutdown mode with PD = DV_{DD} (X = don't care)
7	PD	Power-Down Select 0: Enter DAC standby mode (DACEN = DGND) or power-up DAC (DACEN = DV_{DD}) 1: Enter shutdown mode
8	$\overline{CS}$	Active-Low Chip Select
9	CLK	Clock Input
10	N.C.	No Connection. **Do not connect to this pin**.
11	$\overline{REN}$	Active-Low Reference Enable. Connect to DGND to activate the on-chip +1.2V reference.
12–21	D0–D9	Data Bit D0 (LSB) to Data Bit D9 (MSB)
22	DV_{DD}	Digital Supply, +2.7V to +3.3V
23	DGND	Digital Ground
24	REFR	Reference Input
25	REFO	Reference Output
26	OUT2N	Negative Analog Output, DAC2. Current output for MAX5182; voltage output for MAX5185.
27	OUT2P	Positive Analog Output, DAC2. Current output for MAX5182; voltage output for MAX5185.
28	CREF2	Reference Bias Bypass, DAC2

Dual, 10-Bit, 40MHz Current/Voltage Alternate-Phase Output DACs

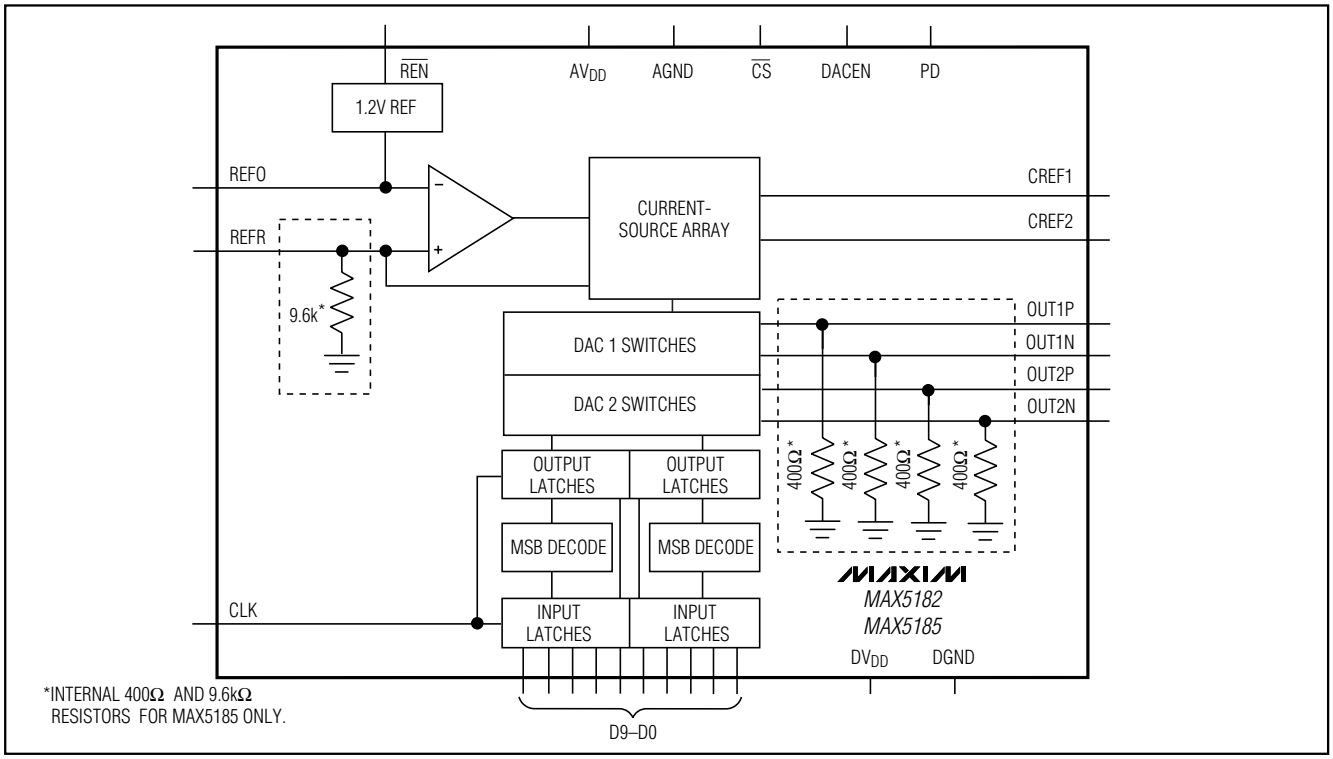


Figure 1. Functional Diagram

Detailed Description

The MAX5182/MAX5185 are dual, 10-bit digital-to-analog converters (DACs) capable of operating with clock speeds up to 40MHz. Each of these dual converters consists of separate input and DAC registers, followed by a current-source array capable of generating up to 1.5mA full-scale output current (Figure 1). An integrated +1.2V voltage reference and control amplifier determine the data converters' full-scale output currents/voltages. Careful reference design ensures close gain matching and excellent drift characteristics. The MAX5185, with its voltage output operation, features matched 400Ω on-chip resistors that convert the current from the current array into a voltage.

Internal Reference and Control Amplifier

The MAX5182/MAX5185 provide an integrated 50ppm/°C, +1.2V, low-noise bandgap reference, which can be disabled and overridden by an external reference voltage. REFO serves either as an input for an external reference or as an output for the integrated reference. If $\overline{REN}$ is connected to DGND, the internal reference is selected and REFO provides a +1.2V output. Due to its limited 10µA output drive capability, the REFO pin must be buffered with an external amplifier if heavier loading is required.

The MAX5182/MAX5185 also employ a control amplifier designed to simultaneously regulate the full-scale output current IFS for both outputs of the ICs. The output current is calculated as follows:

$$I_{FS} = 8 \times I_{REF}$$

where I_{REF} is the reference output current ($I_{REF} = V_{REFO}/R_{SET}$), and I_{FS} is the full-scale output current. R_{SET} is the reference resistor that determines the amplifier's output current (Figure 2) on the MAX5182. This current is mirrored into the current-source array, where it is equally distributed between matched current segments, and summed to valid output current readings for the DACs.

Inside the MAX5185, each output current (DAC1 and DAC2) is converted to an output voltage (V_{OUT1}, V_{OUT2}) with two internal, ground-referenced 400Ω load resistors. Using the internal +1.2V reference voltage, the MAX5185's integrated reference output current resistor (R_{SET} = 9.6kΩ), sets I_{REF} to 125µA and I_{FS} to 1mA.

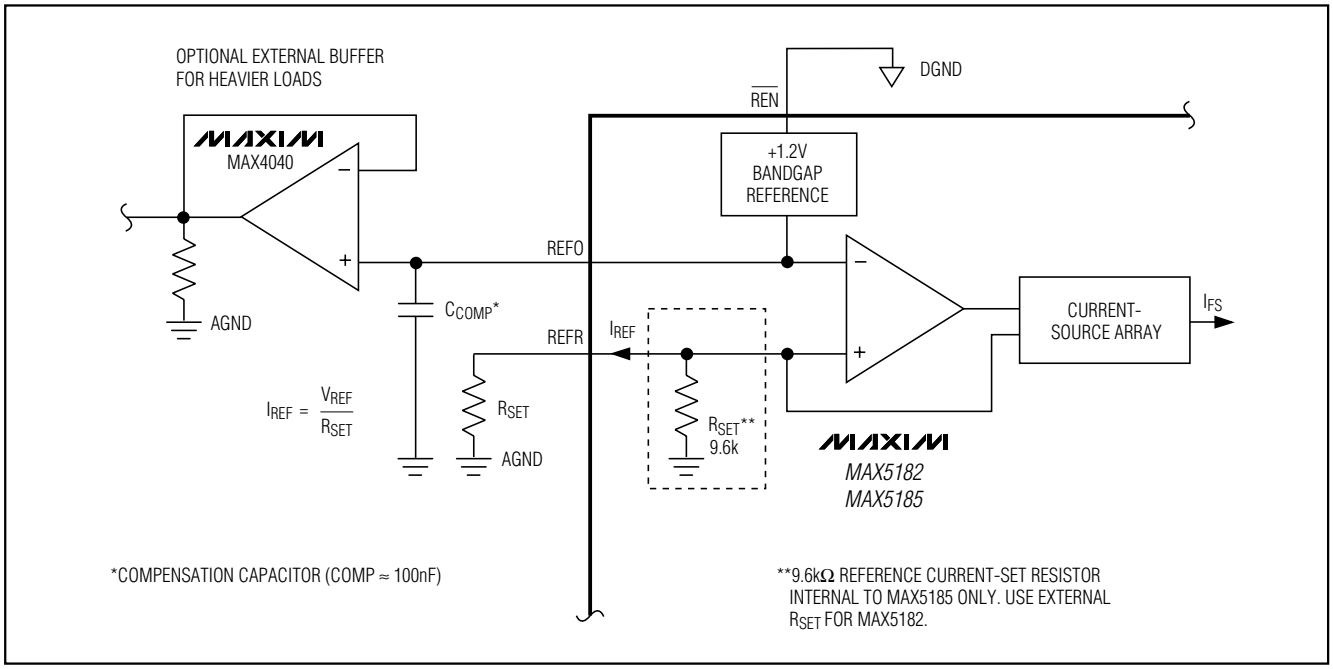


Figure 2. Setting I_{FS} with the Internal +1.2V Reference and the Control Amplifier

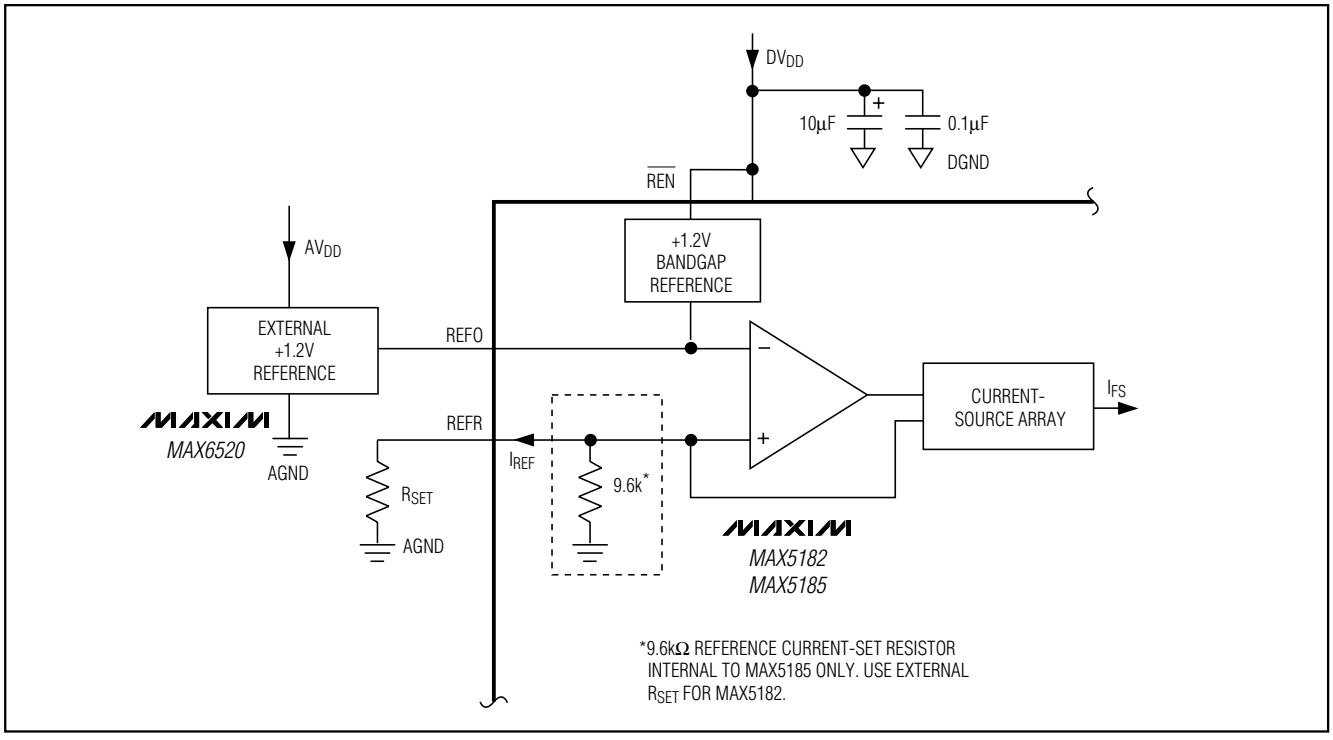


Figure 3. MAX5182/MAX5185 with External Reference

Dual, 10-Bit, 40MHz Current/Voltage Alternate-Phase Output DACs

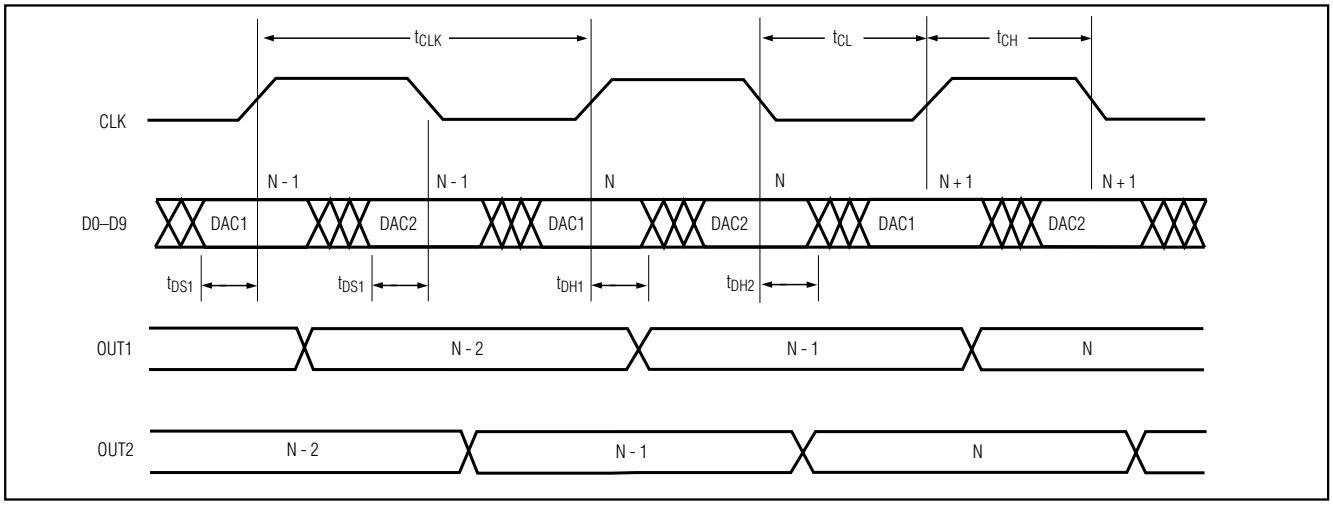


Figure 4. Timing Diagram

Table 1. Power-Down Mode Selection

PD (POWER-DOWN SELECT)	DACEN (DAC ENABLE)	POWER-DOWN MODE	OUTPUT STATE	
0	0	Standby	MAX5182	High-Z
			MAX5185	AGND
0	1	Wake-Up	Last state prior to standby mode	
1	X	Shutdown	MAX5182	High-Z
			MAX5185	AGND

X = Don't care

External Reference

To disable the MAX5182/MAX5185's internal reference, connect REN to DV_{DD}. A temperature-stable, external reference may now be applied to drive the REFO pin (Figure 3) to set the full-scale output. Be sure to choose a reference capable of supplying at least 150µA to drive the bias circuit that generates the cascode current for the current array. For improved accuracy and drift performance, chose a fixed output voltage reference such as the +1.2V, 25ppm/°C MAX6520 bandgap reference.

Standby Mode

To enter the lower power standby mode, connect digital inputs PD and DACEN to DGND. In standby, both the reference and the control amplifier are active, with the current array inactive. To exit this condition, DACEN must be pulled high with PD held at DGND. The MAX5182/MAX5185 typically require 50µs to wake up and let both outputs and reference settle.

Shutdown Mode

For lowest power consumption, the MAX5182/MAX5185 provide a power-down mode in which the reference, control amplifier, and current array are inactive and the DACs supply current is reduced to 1µA. To enter this mode, connect PD to DV_{DD}. To return to active mode, connect PD to DGND and DACEN to DV_{DD}. About 50µs are required for the devices to leave the shutdown mode and to settle their outputs to the values prior to shutdown. Table 1 lists the power-down mode selection.

Timing Information

Both internal DAC cells write to their outputs in alternate phase (Figure 4). The input latch of the first DAC (DAC1) is loaded after the clock signal transitions high. When the clock signal transitions low, the input latch of the second DAC (DAC2) is loaded. The contents of the first input latch are shifted into the DAC1 register on the rising edge of the clock; the contents of the second input latch are shifted into the input register of DAC2 on the falling edge of the clock. Both outputs are updated on alternate phases of the clock.

Outputs

The MAX5182 outputs are designed to supply 1mA full-scale output currents into 400Ω loads in parallel with a 5pF capacitive load. The MAX5185 features integrated 400Ω resistors that restore the array currents into proportional, differential voltages of 400mV. These differential output voltages can then be used to drive a balun transformer or a low-distortion, high-speed operational amplifier to convert the differential voltage into a single-ended voltage.

Applications Information

Static and Dynamic Performance Definitions

Integral Nonlinearity

Integral nonlinearity (INL) (Figure 5a) is the deviation of the values on an actual transfer function from either a best-straight-line fit (closest approximation to the actual transfer curve) or a line drawn between the endpoints of the transfer function, once offset and gain errors have been nullified. For a DAC, the deviations are measured every single step.

Differential Nonlinearity

Differential nonlinearity (DNL) (Figure 5b) is the difference between an actual step height and the ideal value of 1LSB. A DNL error specification of less than 1LSB guarantees no missing codes and a monotonic transfer function.

Offset Error

Offset error (Figure 5c) is the difference between the ideal and the actual offset point. For a DAC, the offset point is the step value when the digital input is zero. This error affects all codes by the same amount and can usually be compensated by trimming.

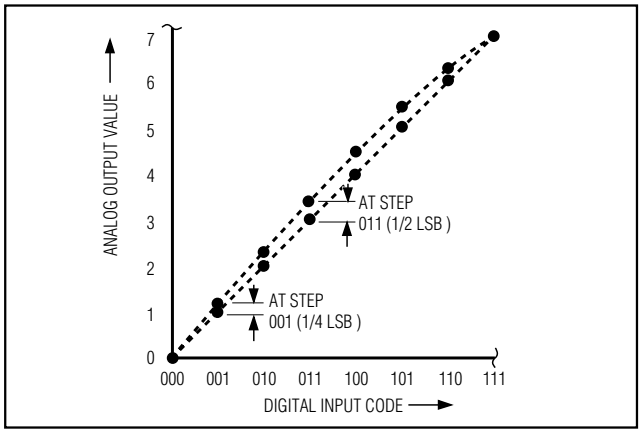


Figure 5a. Integral Nonlinearity

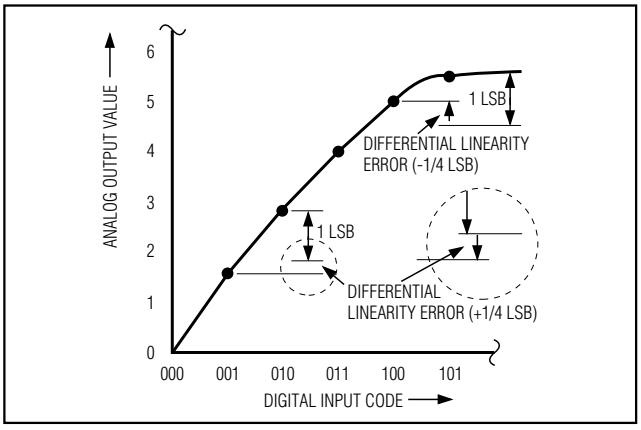


Figure 5b. Differential Nonlinearity

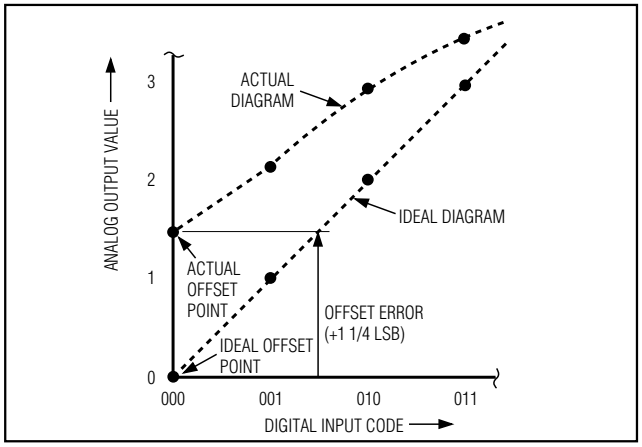


Figure 5c. Offset Error

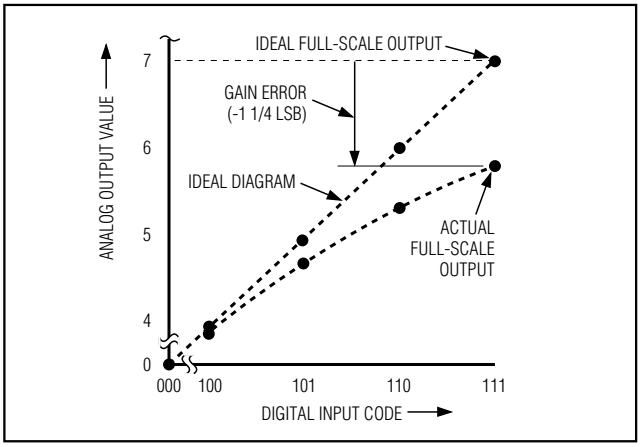


Figure 5d. Gain Error

Dual, 10-Bit, 40MHz Current/Voltage Alternate-Phase Output DACs

Gain Error

Gain error (Figure 5d) is the difference between the ideal and the actual full-scale output voltage on the transfer curve, after nullifying the offset error. This error alters the slope of the transfer function and corresponds to the same percentage error in each step.

Settling Time

Settling time is the amount of time required from the start of a transition until the DAC output settles its new output value to within the converter's specified accuracy.

Digital Feedthrough

Digital feedthrough is the noise generated on a DAC's output when any digital input transitions. Proper board layout and grounding will significantly reduce this noise, but there will always be some feedthrough caused by the DAC itself.

Total Harmonic Distortion

Total harmonic distortion (THD) is the ratio of the RMS sum of the input signal's first four harmonics to the fundamental itself. This is expressed as:

$$THD = 20 \times \log \left(\frac{\sqrt{V_2^2 + V_3^2 + V_4^2 + V_5^2}}{V_1} \right)$$

where V_1 is the fundamental amplitude, and V_2 through V_5 are the amplitudes of the 2nd- through 5th-order harmonics.

Spurious-Free Dynamic Range

Spurious-free dynamic range (SFDR) is the ratio of RMS amplitude of the fundamental (maximum signal component) to the RMS value of the next-largest distortion component.

Differential to Single-Ended Conversion

The MAX4108 low-distortion, high-input bandwidth amplifier may be used to generate a voltage from the MAX5182's current array output. The differential voltage across OUT1P (or OUT2P) and OUT1N (or OUT2N) is converted into a single-ended voltage by designing an appropriate operational amplifier configuration as shown in Figure 6.

Grounding and Power-Supply Decoupling

Grounding and power-supply decoupling strongly influence the performance of the MAX5182/MAX5185. Unwanted digital crosstalk may couple through the input, reference, power-supply, and ground connections, which may affect dynamic specifications like signal-to-noise ratio or SFDR. In addition, electromagnetic interference (EMI) can either couple into or be generated by the MAX5182/MAX5185. Therefore, grounding and power-supply decoupling guidelines for high-speed, high-frequency applications should be closely followed.

First, a multilayer PC board with separate ground and power-supply planes is recommended. High-speed signals should run on controlled impedance lines directly above the ground plane. Since the MAX5182/MAX5185 have separate analog and digital ground buses (AGND and DGND, respectively), the PC board should also have separate analog and digital ground sections with only one point connecting the two. Digital signals should run above the digital ground, and plane and analog signals should run above the analog ground plane.

Both devices have two power-supply inputs: analog V_{DD} (AV_{DD}) and digital V_{DD} (DV_{DD}). Each AV_{DD} input should be decoupled with parallel 10µF and 0.1µF ceramic chip capacitors as close to the pin as possible. Their opposite ends should have the shortest possible connection to the ground plane. The DV_{DD} pins should also have separate 10µF and 0.1µF capacitors, again adjacent to their respective pins. Try to minimize the analog load capacitance for proper operation. For best performance, it is recommended to bypass CREF1 and CREF2 with low-ESR 0.1µF capacitors to AV_{DD}.

The power-supply voltages should also be decoupled at the point they enter the PC board with large tantalum or electrolytic capacitors. Ferrite beads with additional decoupling capacitors forming a pi network could also improve performance.

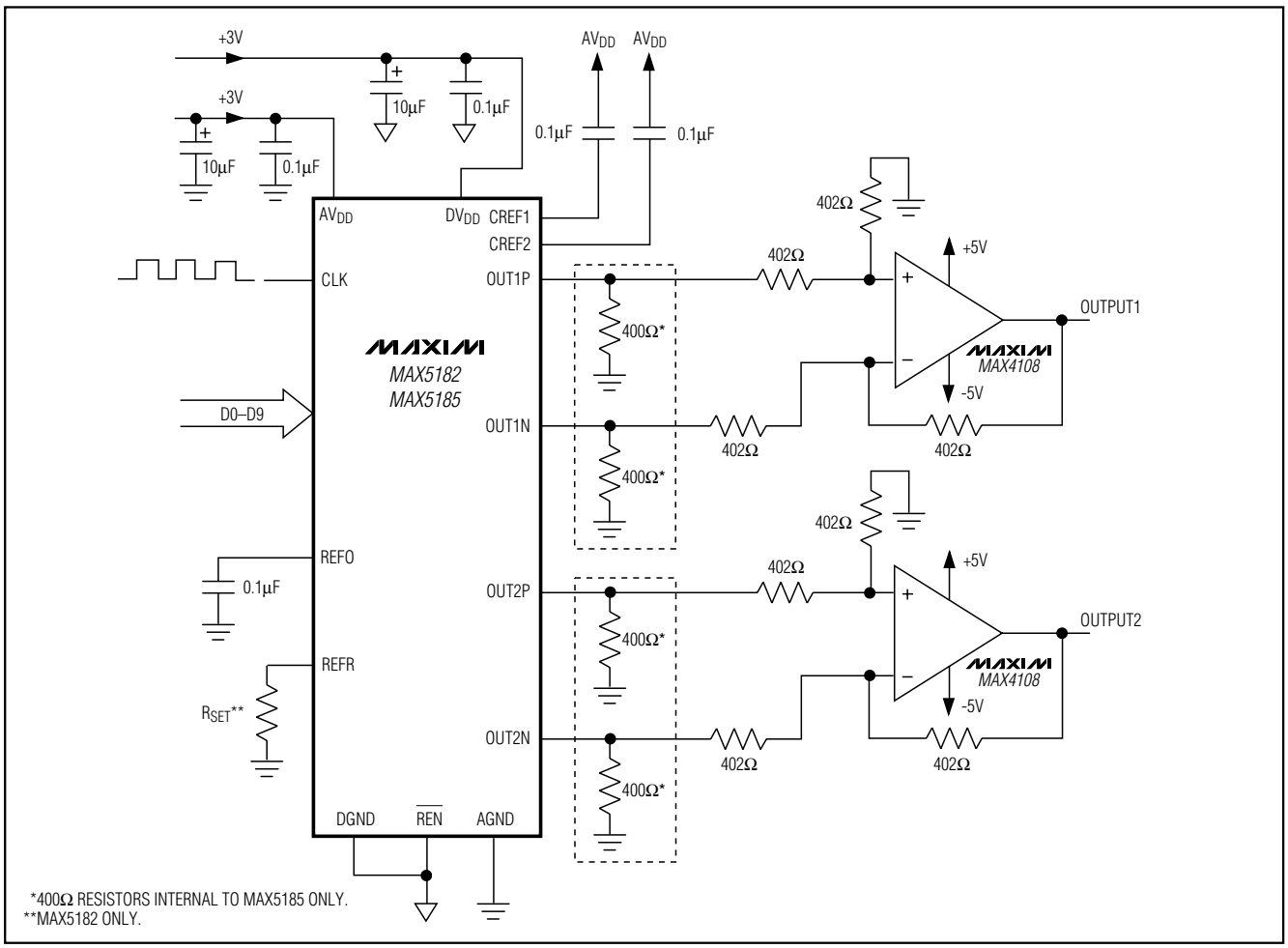


Figure 6. Differential to Single-Ended Conversion Using a Low-Distortion Amplifier

Chip Information

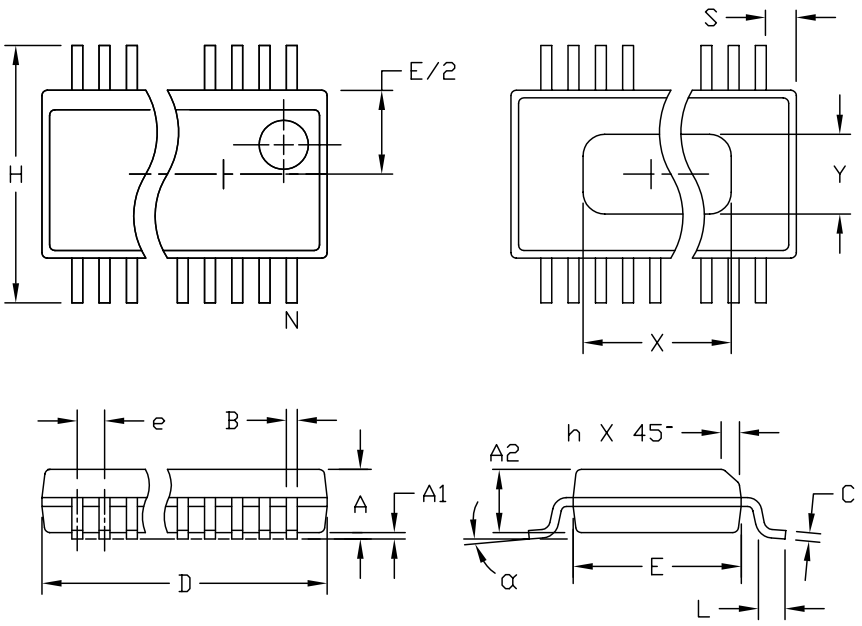
TRANSISTOR COUNT: 9464

SUBSTRATE CONNECTED TO AGND

Dual, 10-Bit, 40MHz Current/Voltage Alternate-Phase Output DACs

Package Information

QSOP EPS



DIM	INCHES MIN	INCHES MAX	MILLIMETERS MIN	MILLIMETERS MAX
A	.061	.068	1.55	1.73
A1	.004	.0098	0.102	0.249
A2	.055	.061	1.40	1.55
B	.008	.012	0.20	0.31
C	.0075	.0098	0.191	0.249
D	SEE VARIATIONS			
E	.150	.157	3.81	3.99
e	.025 BSC		0.635 BSC	
H	.230	.244	5.84	6.20
h	.010	.016	0.25	0.41
L	.016	.035	0.41	0.89
N	SEE VARIATIONS			
X	SEE VARIATIONS			
Y	.071	.087	1.803	2.209
α	0°	8°	0°	8°

VARIATIONS:

	INCHES MIN.	INCHES MAX.	MILLIMETERS MIN.	MILLIMETERS MAX.	N	
D	.189	.196	4.80	4.98	16	AA
S	.0020	.0070	0.05	0.18		
X	.107	.123	2.72	3.12		
D	.337	.344	8.56	8.74	20	AB
S	.0500	.0550	1.270	1.397		
D	.337	.344	8.56	8.74	24	AC
S	.0250	.0300	0.635	0.762		
D	.386	.393	9.80	9.98	28	AD
S	.0250	.0300	0.635	0.762		
X	.271	.287	6.88	7.29		

NOTES:
1. D & E DO NOT INCLUDE MOLD FLASH OR PROTRUSIONS.
2. MOLD FLASH OR PROTRUSIONS NOT TO EXCEED .006" PER SIDE.
3. HEAT SLUG DIMENSIONS X AND Y APPLY ONLY TO 16 AND 28 LEAD POWER-QSOP PACKAGES.
4. CONTROLLING DIMENSIONS: INCHES.
5. MEETS JEDEC MO137.

MAXIM
PROPRIETARY INFORMATION

TITLE:
PACKAGE OUTLINE, QSOP, .150", .025" LEAD PITCH

APPROVAL	DOCUMENT CONTROL NO.	REV	
	21-0055	C	1/1

Mouser Electronics

Authorized Distributor

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Maxim Integrated:

MAX5182BEEI+ MAX5182BEEI+T MAX5185BEEI+ MAX5185BEEI+T