PRODUCT OVERVIEW

The AD6633 is a multichannel, wide bandwidth DUC with a VersaCREST crest reduction engine. It processes digital baseband input data and generates wideband, real, or complex IF output data. It drives DACs up to any IF sampled at up to 125 MSPS. Up to six wideband modulated carriers per package can be achieved from a single output port. Devices may be connected together for additional channels by using multiple packages. Interpolation, anti-image filtering, all-pass equalization, and NCO tuning functions are combined in a single, cost-effective device that includes the VersaCREST crest factor reduction engine.

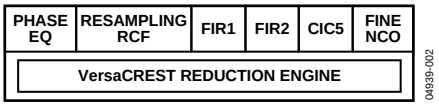

Figure 2. Wideband Channel

Each VersaCREST wideband channel contains a peak-to-average compensation block that reduces PA requirements. By minimizing infrequent peaks in code-division, multiple-access (CDMA) signals, a PA with one-half to one-quarter the previously necessary power capacity can be used. This is done within standard signal quality requirements and significantly lowers system cost.

The input data is time-multiplexed among the active channels for processing through a 20-bit input port. Each channel has a number of elements available to interpolate, resample, and filter the data while tuning to an IF for further upconversion within a radio frequency (RF) system.

An all-pass phase equalizer, designed to comply with IS-95, including cdma2000 standards, is the first available block. A user-configurable, interpolating RAM coefficient filter (RCF) is the first general-purpose filter stage in the channel. It provides multirate processing, including resampling and malleable finite impulse response (FIR) filter characteristics. Further filtering can be accomplished with two additional, fixed-coefficient, FIR, half-band stages. A fifth-order, cascade integrator comb (CIC5) is the final filter stage available.

Each channel has its own 32-bit NCO to upconvert the filtered/interpolated data to a first IF.

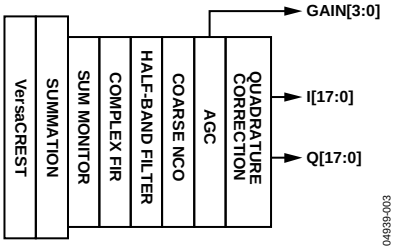

Figure 3. Summation and Post-Sum Blocks

Post-processing after channel summation includes power monitoring, filtering, composite NCO, digital automatic gain control (AGC) output, and quadrature correction stages. The output may be real or complex, and complex output may be parallel on two 18-bit ports or interleaved on one 18-bit port.

Control registers and coefficient values are programmed through a generic 16-bit microprocessor interface or a SPI-/SPORT-compatible serial port. Intel and Motorola microprocessor bus modes are supported.

The AD6633 uses a 3.3 V I/O power supply and a 1.8 V core power supply. Typical power consumption is 75 mW per channel or 1.4 W for the complete device. All inputs and outputs are LVCMOS-compatible and are 5 V tolerant.

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