

# Table of Contents

|        |  |    |
|--------|--|----|
| 1      | Pin Assignments and Reset States                                 | 4  |
| 1.1    | Signal Properties and Multiplexing Summary                       | 4  |
| 1.2    | Power and Ground Supply Summary                                  | 15 |
| 1.3    | Pinout – 144 LQFP  | 17 |
| 1.4    | Pinout – 176 LQFP  | 18 |
| 1.5    | Pinout – 208 PBGA  | 19 |
| 2      | Electrical Characteristics                                       | 20 |
| 2.1    | Maximum Ratings  | 20 |
| 2.2    | Thermal Characteristics  | 21 |
| 2.2.1  | General Notes for Specifications at Maximum Junction Temperature | 21 |
| 2.3    | ESD Characteristics  | 24 |
| 2.4    | DC Electrical Specifications                                     | 25 |
| 2.5    | Operating Current Specifications                                 | 27 |
| 2.6    | I/O Pad Current Specifications                                   | 29 |
| 2.7    | Low Voltage Characteristics                                      | 30 |
| 2.8    | Oscillators Electrical Characteristics                           | 31 |
| 2.9    | FMPLL Electrical Characteristics                                 | 33 |
| 2.10   | eQADC Electrical Characteristics                                 | 34 |
| 2.11   | Flash Memory Electrical Characteristics                          | 35 |
| 2.12   | Pad AC Specifications  | 36 |
| 2.13   | AC Timing  | 37 |
| 2.13.1 | Reset and Boot Configuration Pins                                | 37 |
| 2.13.2 | External Interrupt (IRQ) and Non-Maskable Interrupt (NMI) Pins   | 37 |
| 2.13.3 | JTAG (IEEE 1149.1) Interface                                     | 38 |
| 2.13.4 | Nexus Debug Interface  | 41 |
| 2.13.5 | External Bus Interface (EBI)                                     | 43 |
| 2.13.6 | Enhanced Modular I/O Subsystem (eMIOS)                           | 46 |
| 2.13.7 | Deserial Serial Peripheral Interface (DSPI)                      | 47 |
| 3      | Package Information  | 52 |
| 4      | Product Documentation  | 52 |
| 4.1    | Revision History   | 53 |

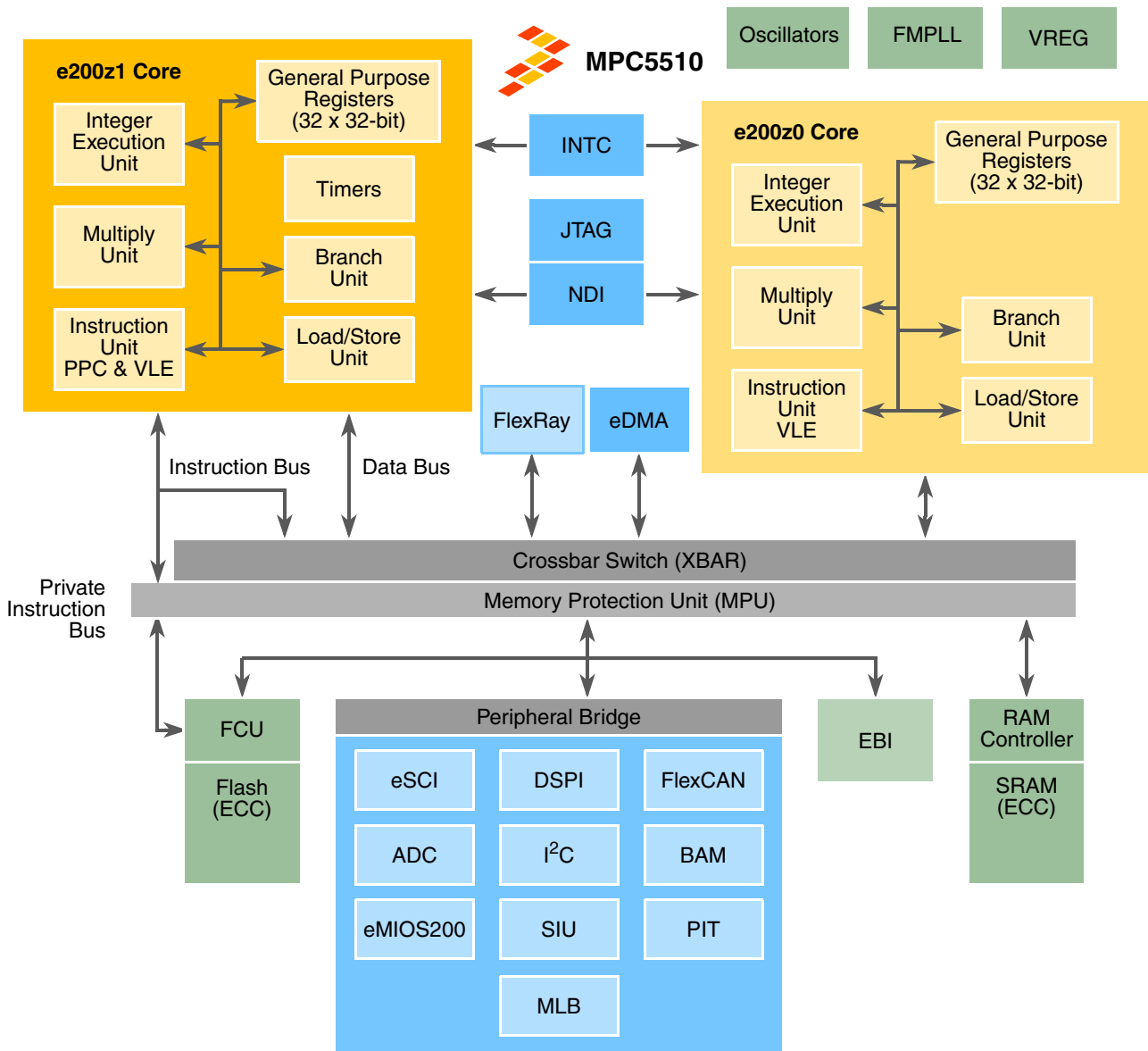
## List of Tables

|           |   |    |
|-----------|---|----|
| Table 1.  | MPC5510 Signal Properties                         | 4  |
| Table 2.  | MPC5510 Power/Ground                              | 15 |
| Table 3.  | Absolute Maximum Ratings                          | 20 |
| Table 4.  | Thermal Characteristics                           | 21 |
| Table 5.  | ESD Ratings                                       | 24 |
| Table 6.  | DC Electrical Specifications                      | 25 |
| Table 7.  | Operating Currents                                | 27 |
| Table 8.  | I/O Pad Average DC Current                        | 29 |
| Table 9.  | Low Voltage Monitors                              | 30 |
| Table 10. | 3.3V High Frequency External Oscillator           | 31 |
| Table 11. | 5V Low Frequency (32 kHz) External Oscillator     | 31 |
| Table 12. | 5V High Frequency (16 MHz) Internal RC Oscillator | 32 |

|           |   |    |
|-----------|---|----|
| Table 13. | 5V Low Frequency (32 kHz) Internal RC Oscillator  | 32 |
| Table 14. | FMPLL Electrical Specifications                   | 33 |
| Table 15. | eQADC Conversion Specifications (Operating)       | 34 |
| Table 16. | Flash Program and Erase Specifications            | 35 |
| Table 17. | Flash EEPROM Module Life (Full Temperature Range) | 35 |
| Table 18. | Pad AC Specifications (VDDE = 3.0V - 5.5V)        | 36 |
| Table 19. | Reset and Boot Configuration Timing               | 37 |
| Table 20. | IRQ/NMI Timing                                    | 37 |
| Table 21. | JTAG Interface Timing                             | 38 |
| Table 22. | Nexus Debug Port Timing                           | 41 |
| Table 23. | External Bus Operation Timing                     | 43 |
| Table 24. | eMIOS Timing                                      | 46 |
| Table 25. | DSPI Timing                                       | 47 |
| Table 26. | Package Information                               | 52 |
| Table 27. | Revision History of MPC5510 Data Sheet            | 53 |

## List of Figures

|            |   |    |
|------------|---|----|
| Figure 1.  | MPC5510 Family Block Diagram                            | 3  |
| Figure 2.  | MPC5510 Pinout – 144 LQFP                               | 17 |
| Figure 3.  | MPC5510 Pinout – 176 LQFP                               | 18 |
| Figure 4.  | MPC5510 Pinout – 208 PBGA                               | 19 |
| Figure 5.  | Pad Output Delay  | 36 |
| Figure 6.  | Reset and Boot Configuration Timing                     | 37 |
| Figure 7.  | IRQ and NMI Timing                                      | 37 |
| Figure 8.  | JTAG Test Clock Input Timing                            | 38 |
| Figure 9.  | JTAG Test Access Port Timing                            | 39 |
| Figure 10. | JTAG JCOMP Timing                                       | 39 |
| Figure 11. | JTAG Boundary Scan Timing                               | 40 |
| Figure 12. | Nexus Output Timing                                     | 41 |
| Figure 13. | Nexus TDI, TMS, TDO Timing                              | 42 |
| Figure 14. | CLKOUT Timing   | 43 |
| Figure 15. | Synchronous Output Timing                               | 44 |
| Figure 16. | Synchronous Input Timing                                | 45 |
| Figure 17. | Address Latch Enable (ALE) Timing                       | 46 |
| Figure 18. | DSPI Classic SPI Timing — Master, CPHA = 0              | 48 |
| Figure 19. | DSPI Classic SPI Timing — Master, CPHA = 1              | 48 |
| Figure 20. | DSPI Classic SPI Timing — Slave, CPHA = 0               | 49 |
| Figure 21. | DSPI Classic SPI Timing — Slave, CPHA = 1               | 49 |
| Figure 22. | DSPI Modified Transfer Format Timing — Master, CPHA = 0 | 50 |
| Figure 23. | DSPI Modified Transfer Format Timing — Master, CPHA = 1 | 50 |
| Figure 24. | DSPI Modified Transfer Format Timing — Slave, CPHA = 0  | 51 |
| Figure 25. | DSPI Modified Transfer Format Timing — Slave, CPHA = 1  | 51 |
| Figure 26. | DSPI PCS Strobe (PCSS) Timing                           | 51 |



**LEGEND**

- |  |   |
|--|---|
| <b>ADC</b> – Analog to Digital Converter modules             | <b>FlexRay</b> – Dual Channel FlexRay controller            |
| <b>BAM</b> – Boot Assist Module                              | <b>FMPLL</b> – Frequency Modulated Phase Locked Loop module |
| <b>EBI</b> – External Bus Interface module                   | <b>I<sup>2</sup>C</b> – Inter IC Controller modules         |
| <b>ECC</b> – Error Correction Code                           | <b>INTC</b> – Interrupt Controller module                   |
| <b>DSPI</b> – Serial Peripherals Interface controller module | <b>JTAG</b> – Joint Test Action Group interface             |
| <b>eDMA</b> – enhanced Direct Memory Controller module       | <b>MLB</b> – Media Local Bus emulation logic                |
| <b>eMIOS200</b> – Timed Input Output module                  | <b>NDI</b> – Nexus Debug Interface module                   |
| <b>eSCI</b> – Serial Communications Interface modules        | <b>PIT</b> – Periodic Interrupt Timer module                |
| <b>FCU</b> – Flash Controller Unit                           | <b>SIU</b> – System Integration module                      |
| <b>FlexCAN</b> – Controller Area Network controller modules  | <b>VREG</b> – Voltage Regulator                             |

**Figure 1. MPC5510 Family Block Diagram**

# 1 Pin Assignments and Reset States

## 1.1 Signal Properties and Multiplexing Summary

Table 1 shows the signal properties for each pin on the MPC5510. For all port pins, which have an associated pad configuration register (SIU\_PCR $n$  register) to control its pin properties, the “Supported Pin Functions” column lists the functions associated with the programming of the SIU\_PCR $n$ [PA] bit field in the following order: GPIO, Function1, Function2 and Function3. If fewer than three functions plus GPIO are supported by a given pin, then the unused functions begin with Function3, then Function2, then Function1. Note that the GPIO number is the same number as the corresponding pad configuration register (SIU\_PCR $n$ ) number.

**Table 1. MPC5510 Signal Properties**

| Pin Name           | GPIO (PCR) Num <sup>1</sup> | Supported Functions <sup>2</sup>     | Description  | I/O Type    | Voltage <sup>3</sup> | Pad <sup>4</sup> Type | Status During Reset <sup>5</sup> | Status After Reset <sup>5</sup> | Package Pin Locations |     |     |
|--------------------|-----------------------------|--------------------------------------|--|-------------|----------------------|-----------------------|----------------------------------|---------------------------------|-----------------------|-----|-----|
|                    |                             |                                      |  |             |                      |                       |                                  |                                 | 144                   | 176 | 208 |
| <b>Port A (16)</b> |                             |                                      |  |             |                      |                       |                                  |                                 |                       |     |     |
| PA0                | 0                           | PA0<br>AN0                           | GPI<br>eQADC Analog Input                                    | I<br>I      | V <sub>DDA</sub>     | AE + IH               | —                                | —                               | 9                     | 9   | E3  |
| PA1                | 1                           | PA1<br>AN1                           | GPI<br>eQADC Analog Input                                    | I<br>I      | V <sub>DDA</sub>     | AE + IH               | —                                | —                               | 8                     | 8   | E2  |
| PA2                | 2                           | PA2<br>AN2                           | GPI<br>eQADC Analog Input                                    | I<br>I      | V <sub>DDA</sub>     | AE + IH               | —                                | —                               | 7                     | 7   | E1  |
| PA3                | 3                           | PA3<br>AN3                           | GPI<br>eQADC Analog Input                                    | I<br>I      | V <sub>DDA</sub>     | AE + IH               | —                                | —                               | 6                     | 6   | D3  |
| PA4                | 4                           | PA4<br>AN4                           | GPI<br>eQADC Analog Input                                    | I<br>I      | V <sub>DDA</sub>     | AE + IH               | —                                | —                               | 5                     | 5   | D2  |
| PA5                | 5                           | PA5<br>AN5                           | GPI<br>eQADC Analog Input                                    | I<br>I      | V <sub>DDA</sub>     | AE + IH               | —                                | —                               | 4                     | 4   | D1  |
| PA6                | 6                           | PA6<br>AN6                           | GPI<br>eQADC Analog Input                                    | I<br>I      | V <sub>DDA</sub>     | AE + IH               | —                                | —                               | 3                     | 3   | C2  |
| PA7                | 7                           | PA7<br>AN7                           | GPI<br>eQADC Analog Input                                    | I<br>I      | V <sub>DDA</sub>     | AE + IH               | —                                | —                               | 2                     | 2   | C1  |
| PA8                | 8                           | PA8<br>AN8/ANW                       | GPI<br>eQADC Analog Input                                    | I<br>I      | V <sub>DDA</sub>     | AE + IH               | —                                | —                               | 143                   | 175 | A3  |
| PA9                | 9                           | PA9<br>AN9/ANX                       | GPI<br>eQADC Analog Input                                    | I<br>I      | V <sub>DDA</sub>     | AE + IH               | —                                | —                               | 142                   | 174 | C4  |
| PA10               | 10                          | PA10<br>AN10/ANY                     | GPI<br>eQADC Analog Input                                    | I<br>I      | V <sub>DDA</sub>     | AE + IH               | —                                | —                               | 140                   | 172 | D5  |
| PA11               | 11                          | PA11<br>AN11/ANZ                     | GPI<br>eQADC Analog Input                                    | I<br>I      | V <sub>DDA</sub>     | AE + IH               | —                                | —                               | 139                   | 171 | C5  |
| PA12               | 12                          | PA12<br>AN12                         | GPI<br>eQADC Analog Input                                    | I<br>I      | V <sub>DDA</sub>     | AE + IH               | —                                | —                               | 138                   | 170 | B5  |
| PA13               | 13                          | PA13<br>AN13                         | GPI<br>eQADC Analog Input                                    | I<br>I      | V <sub>DDA</sub>     | AE + IH               | —                                | —                               | 137                   | 169 | A5  |
| PA14               | 14                          | PA14<br>AN14<br>EXTAL32 <sup>6</sup> | GPI<br>eQADC Analog Input<br>32 kHz Crystal Oscillator Input | I<br>I<br>I | V <sub>DDA</sub>     | AE + IH               | —                                | —                               | 136                   | 167 | D6  |

Table 1. MPC5510 Signal Properties (continued)

| Pin Name           | GPIO (PCR) Num <sup>1</sup> | Supported Functions <sup>2</sup>    | Description  | I/O Type           | Voltage <sup>3</sup> | Pad <sup>4</sup> Type | Status During Reset <sup>5</sup> | Status After Reset <sup>5</sup> | Package Pin Locations |     |     |
|--------------------|-----------------------------|-------------------------------------|--|--------------------|----------------------|-----------------------|----------------------------------|---------------------------------|-----------------------|-----|-----|
|                    |                             |                                     |  |                    |                      |                       |                                  |                                 | 144                   | 176 | 208 |
| PA15               | 15                          | PA15<br>AN15<br>XTAL32 <sup>6</sup> | GPI<br>eQADC Analog Input<br>32 kHz Crystal Oscillator Output                              | I<br>I<br>O        | V <sub>DDE1</sub>    | AE + IH               | —                                | —                               | 135                   | 165 | C6  |
| <b>Port B (16)</b> |                             |                                     |  |                    |                      |                       |                                  |                                 |                       |     |     |
| PB0                | 16                          | PB0<br>AN28<br>eMIOS16<br>PCS_C5    | GPIO<br>eQADC Analog Input <sup>7</sup><br>eMIOS Channel<br>DSPI_C Peripheral Chip Select  | I/O<br>I<br>O<br>O | V <sub>DDE1</sub>    | A + SH                | —                                | —                               | 134                   | 162 | C7  |
| PB1                | 17                          | PB1<br>AN29<br>eMIOS17<br>PCS_C4    | GPIO<br>eQADC Analog Input <sup>7</sup><br>eMIOS Channel<br>DSPI_C Peripheral Chip Select  | I/O<br>I<br>O<br>O | V <sub>DDE1</sub>    | A + SH                | —                                | —                               | 133                   | 161 | D7  |
| PB2                | 18                          | PB2<br>AN30<br>eMIOS18<br>PCS_C3    | GPIO<br>eQADC Analog Input <sup>7</sup><br>eMIOS Channel<br>DSPI_C Peripheral Chip Select  | I/O<br>I<br>O<br>O | V <sub>DDE1</sub>    | A + SH                | —                                | —                               | 132                   | 160 | A8  |
| PB3                | 19                          | PB3<br>AN31<br>PCS_C2               | GPIO<br>eQADC Analog Input <sup>7</sup><br>DSPI_C Peripheral Chip Select                   | I/O<br>I<br>O      | V <sub>DDE1</sub>    | A + SH                | —                                | —                               | 131                   | 159 | B8  |
| PB4                | 20                          | PB4<br>AN32<br>PCS_C1               | GPIO<br>eQADC Analog Input <sup>7</sup><br>DSPI_C Peripheral Chip Select                   | I/O<br>I<br>O      | V <sub>DDE1</sub>    | A + SH                | —                                | —                               | 130                   | 158 | C8  |
| PB5                | 21                          | PB5<br>AN33<br>PCS_C0               | GPIO<br>eQADC Analog Input <sup>7</sup><br>DSPI_C Peripheral Chip Select                   | I/O<br>I<br>I/O    | V <sub>DDE1</sub>    | A + SH                | —                                | —                               | 129                   | 157 | D8  |
| PB6                | 22                          | PB6<br>AN34<br>SCK_C                | GPIO<br>eQADC Analog Input <sup>7</sup><br>DSPI_C Clock                                    | I/O<br>I<br>I/O    | V <sub>DDE1</sub>    | A + SH                | —                                | —                               | 128                   | 156 | A9  |
| PB7                | 23                          | PB7<br>AN35<br>SOUT_C               | GPIO<br>eQADC Analog Input <sup>7</sup><br>DSPI_C Data Output                              | I/O<br>I<br>O      | V <sub>DDE1</sub>    | A + SH                | —                                | —                               | 127                   | 153 | B9  |
| PB8                | 24                          | PB8<br>AN36<br>SIN_C                | GPIO<br>eQADC Analog Input <sup>7</sup><br>DSPI_C Data Input                               | I/O<br>I<br>I      | V <sub>DDE1</sub>    | A + SH                | —                                | —                               | 126                   | 152 | C9  |
| PB9                | 25                          | PB9<br>AN37<br>CNTX_D<br>PCS_B4     | GPIO<br>eQADC Analog Input <sup>7</sup><br>CAN_D Transmit<br>DSPI_B Peripheral Chip Select | I/O<br>I<br>O<br>O | V <sub>DDE1</sub>    | A + SH                | —                                | —                               | 125                   | 151 | D9  |
| PB10               | 26                          | PB10<br>AN38<br>CNRX_D<br>PCS_B3    | GPIO<br>eQADC Analog Input <sup>7</sup><br>CAN_D Receive<br>DSPI_B Peripheral Chip Select  | I/O<br>I<br>I<br>O | V <sub>DDE1</sub>    | A + SH                | —                                | —                               | 124                   | 150 | A10 |
| PB11               | 27                          | PB11<br>AN39<br>eMIOS19<br>PCS_B5   | GPIO<br>eQADC Analog Input <sup>7</sup><br>eMIOS Channel<br>DSPI_B Peripheral Chip Select  | I/O<br>I<br>O<br>O | V <sub>DDE1</sub>    | A + SH                | —                                | —                               | 123                   | 149 | B10 |

Table 1. MPC5510 Signal Properties (continued)

| Pin Name           | GPIO (PCR) Num <sup>1</sup> | Supported Functions <sup>2</sup>    | Description  | I/O Type               | Voltage <sup>3</sup> | Pad <sup>4</sup> Type | Status During Reset <sup>5</sup> | Status After Reset <sup>5</sup> | Package Pin Locations |     |     |
|--------------------|-----------------------------|-------------------------------------|--|------------------------|----------------------|-----------------------|----------------------------------|---------------------------------|-----------------------|-----|-----|
|                    |                             |                                     |  |                        |                      |                       |                                  |                                 | 144                   | 176 | 208 |
| PB12               | 28                          | PB12<br>TXD_G<br>PCS_B4             | GPIO<br>SCI_G Transmit<br>DSPI_B Peripheral Chip Select                              | I/O<br>O<br>O          | V <sub>DDE1</sub>    | SH                    | —                                | —                               | —                     | 164 | A7  |
| PB13               | 29                          | PB13<br>RXD_G<br>PCS_B3             | GPIO<br>SCI_G Receive<br>DSPI_B Peripheral Chip Select                               | I/O<br>I<br>O          | V <sub>DDE1</sub>    | SH                    | —                                | —                               | —                     | 163 | B7  |
| PB14               | 30                          | PB14<br>TXD_H                       | GPIO<br>SCI_H Transmit   | I/O<br>O               | V <sub>DDE1</sub>    | SH                    | —                                | —                               | —                     | 148 | C10 |
| PB15               | 31                          | PB15<br>RXD_H                       | GPIO<br>SCI_H Receive  | I/O<br>I               | V <sub>DDE1</sub>    | SH                    | —                                | —                               | —                     | 147 | A11 |
| <b>Port C (16)</b> |                             |                                     |  |                        |                      |                       |                                  |                                 |                       |     |     |
| PC0                | 32                          | PC0<br>eMIOS0<br>FR_A_TX_EN<br>AD24 | GPIO<br>eMIOS Channel<br>FlexRay Channel A Transmit Enable<br>EBI Muxed Address/Data | I/O<br>I/O<br>O<br>I/O | V <sub>DDE1</sub>    | MH                    | —                                | —                               | 122                   | 146 | B11 |
| PC1                | 33                          | PC1<br>eMIOS1<br>FR_A_TX<br>AD16    | GPIO<br>eMIOS Channel<br>FlexRay Channel A Transmit<br>EBI Muxed Address/Data        | I/O<br>I/O<br>O<br>I/O | V <sub>DDE1</sub>    | MH                    | —                                | —                               | 121                   | 145 | C11 |
| PC2                | 34                          | PC2<br>eMIOS2<br>FR_A_RX<br>TS      | GPIO<br>eMIOS Channel<br>FlexRay Channel A Receive<br>EBI Transfer Start             | I/O<br>I/O<br>I<br>I/O | V <sub>DDE1</sub>    | MH                    | —                                | —                               | 120                   | 144 | D11 |
| PC3                | 35                          | PC3<br>eMIOS3<br>FR_DBG0            | GPIO<br>eMIOS Channel<br>FlexRay Debug   | I/O<br>I/O<br>O        | V <sub>DDE1</sub>    | MH                    | —                                | —                               | 117                   | 141 | A12 |
| PC4                | 36                          | PC4<br>eMIOS4<br>FR_DBG1            | GPIO<br>eMIOS Channel<br>FlexRay Debug   | I/O<br>I/O<br>O        | V <sub>DDE1</sub>    | SH                    | —                                | —                               | 116                   | 140 | B12 |
| PC5                | 37                          | PC5<br>eMIOS5<br>FR_DBG2            | GPIO<br>eMIOS Channel<br>FlexRay Debug   | I/O<br>I/O<br>O        | V <sub>DDE1</sub>    | SH                    | —                                | —                               | 115                   | 139 | C12 |
| PC6                | 38                          | PC6<br>eMIOS6<br>FR_DBG3            | GPIO<br>eMIOS Channel<br>FlexRay Debug   | I/O<br>I/O<br>O        | V <sub>DDE1</sub>    | SH                    | —                                | —                               | 114                   | 138 | D12 |
| PC7                | 39                          | PC7<br>eMIOS7<br>FR_B_RX            | GPIO<br>eMIOS Channel<br>FlexRay Channel B Receive                                   | I/O<br>I/O<br>I        | V <sub>DDE1</sub>    | SH                    | —                                | —                               | 113                   | 137 | A13 |
| PC8                | 40                          | PC8<br>eMIOS8<br>FR_B_TX<br>AD15    | GPIO<br>eMIOS Channel<br>FlexRay Channel B Transmit<br>EBI Muxed Address/Data        | I/O<br>I/O<br>O<br>I/O | V <sub>DDE1</sub>    | MH                    | —                                | —                               | 112                   | 136 | B13 |
| PC9                | 41                          | PC9<br>eMIOS9<br>FR_B_TX_EN<br>AD14 | GPIO<br>eMIOS Channel<br>FlexRay Channel B Transmit Enable<br>EBI Muxed Address/Data | I/O<br>I/O<br>O<br>I/O | V <sub>DDE1</sub>    | MH                    | —                                | —                               | 111                   | 135 | C13 |

Table 1. MPC5510 Signal Properties (continued)

| Pin Name           | GPIO (PCR) Num <sup>1</sup> | Supported Functions <sup>2</sup>              | Description   | I/O Type                | Voltage <sup>3</sup> | Pad <sup>4</sup> Type | Status During Reset <sup>5</sup> | Status After Reset <sup>5</sup> | Package Pin Locations |     |     |
|--------------------|-----------------------------|---|---|-------------------------|----------------------|-----------------------|----------------------------------|---------------------------------|-----------------------|-----|-----|
|                    |                             |   |   |                         |                      |                       |                                  |                                 | 144                   | 176 | 208 |
| PC10               | 42                          | PC10<br>eMIOS10<br>PCS_C5<br>SCK_D            | GPIO<br>eMIOS Channel<br>DSPI_C Peripheral Chip Select<br>DSPI_D Clock                        | I/O<br>I/O<br>O<br>I/O  | V <sub>DDE1</sub>    | SH                    | —                                | —                               | 110                   | 134 | A14 |
| PC11               | 43                          | PC11<br>eMIOS11<br>PCS_C4<br>SOUT_D           | GPIO<br>eMIOS Channel<br>DSPI_C Peripheral Chip Select<br>DSPI_D Serial Out                   | I/O<br>I/O<br>O<br>O    | V <sub>DDE1</sub>    | SH                    | —                                | —                               | 109                   | 133 | B14 |
| PC12               | 44                          | PC12<br>eMIOS12<br>PSC_C3<br>SIN_D            | GPIO<br>eMIOS Channel<br>DSPI_C Peripheral Chip Select<br>DSPI_D Serial In                    | I/O<br>I/O<br>O<br>I    | V <sub>DDE1</sub>    | SH                    | —                                | —                               | 108                   | 132 | B16 |
| PC13               | 45                          | PC13<br>eMIOS13<br>PCS_A5<br>PCS_D0           | GPIO<br>eMIOS Channel<br>DSPI_A Peripheral Chip Select<br>DSPI_D Peripheral Chip Select       | I/O<br>I/O<br>O<br>O    | V <sub>DDE1</sub>    | SH                    | —                                | —                               | 107                   | 131 | C15 |
| PC14               | 46                          | PC14<br>eMIOS14<br>PCS_A4<br>PCS_D1           | GPIO<br>eMIOS Channel<br>DSPI_A Peripheral Chip Select<br>DSPI_D Peripheral Chip Select       | I/O<br>I/O<br>O<br>O    | V <sub>DDE1</sub>    | SH                    | —                                | —                               | 106                   | 130 | C16 |
| PC15               | 47                          | PC15<br>eMIOS15<br>PCS_A3<br>PCS_D2           | GPIO<br>eMIOS Channel<br>DSPI_A Peripheral Chip Select<br>DSPI_D Peripheral Chip Select       | I/O<br>I/O<br>O<br>O    | V <sub>DDE1</sub>    | SH                    | —                                | —                               | 105                   | 129 | D14 |
| <b>Port D (16)</b> |                             |   |   |                         |                      |                       |                                  |                                 |                       |     |     |
| PD0                | 48                          | PD0<br>CNTX_A<br>PCS_D3                       | GPIO<br>CAN_A Transmit<br>DSPI_D Peripheral Chip Select                                       | I/O<br>O<br>O           | V <sub>DDE1</sub>    | SH                    | —                                | —                               | 104                   | 128 | D15 |
| PD1                | 49                          | PD1<br>CNRX_A<br>PCS_D4                       | GPIO<br>CAN_A Receive<br>DSPI_D Peripheral Chip Select  | I/O<br>I<br>O           | V <sub>DDE1</sub>    | SH                    | —                                | —                               | 103                   | 127 | D16 |
| PD2                | 50                          | PD2<br>CNRX_B<br>eMIOS10<br>BOOTCFG<br>PCS_D5 | GPIO<br>CAN_B Receive<br>eMIOS Channel<br>Boot Configuration<br>DSPI_D Peripheral Chip Select | I/O<br>I<br>O<br>I<br>O | V <sub>DDE1</sub>    | SH                    | BOOTCFG<br>(Pulldown)            | GPI<br>(Pulldown)               | 102                   | 126 | E14 |
| PD3                | 51                          | PD3<br>CNTX_B<br>eMIOS11                      | GPIO<br>CAN_B Transmit<br>eMIOS Channel   | I/O<br>O<br>O           | V <sub>DDE1</sub>    | SH                    | —                                | —                               | 101                   | 125 | E15 |
| PD4                | 52                          | PD4<br>CNTX_C<br>eMIOS12                      | GPIO<br>CAN_C Transmit<br>eMIOS Channel   | I/O<br>O<br>O           | V <sub>DDE1</sub>    | SH                    | —                                | —                               | 100                   | 124 | E16 |
| PD5                | 53                          | PD5<br>CNRX_C<br>eMIOS13                      | GPIO<br>CAN_C Receive<br>eMIOS Channel  | I/O<br>I<br>O           | V <sub>DDE1</sub>    | SH                    | —                                | —                               | 99                    | 123 | F13 |

Table 1. MPC5510 Signal Properties (continued)

| Pin Name           | GPIO (PCR) Num <sup>1</sup> | Supported Functions <sup>2</sup>             | Description  | I/O Type                    | Voltage <sup>3</sup> | Pad <sup>4</sup> Type | Status During Reset <sup>5</sup> | Status After Reset <sup>5</sup> | Package Pin Locations |     |     |
|--------------------|-----------------------------|--|--|-----------------------------|----------------------|-----------------------|----------------------------------|---------------------------------|-----------------------|-----|-----|
|                    |                             |  |  |                             |                      |                       |                                  |                                 | 144                   | 176 | 208 |
| PD6                | 54                          | PD6<br>TXD_A<br>eMIOS14                      | GPIO<br>SCI_A Transmit<br>eMIOS Channel  | I/O<br>O<br>O               | V <sub>DDE1</sub>    | SH                    | —                                | —                               | 98                    | 122 | F14 |
| PD7                | 55                          | PD7<br>RXD_A<br>eMIOS15                      | GPIO<br>SCI_A Receive<br>eMIOS Channel   | I/O<br>I<br>O               | V <sub>DDE1</sub>    | SH                    | —                                | —                               | 97                    | 121 | F15 |
| PD8                | 56                          | PD8<br>TXD_B<br>SCL_A                        | GPIO<br>SCI_B Transmit<br>I <sup>2</sup> C Serial Clock Line   | I/O<br>O<br>I/O             | V <sub>DDE1</sub>    | SH                    | —                                | —                               | 94                    | 118 | G13 |
| PD9                | 57                          | PD9<br>RXD_B<br>SDA_A                        | GPIO<br>SCI_B Receive<br>I <sup>2</sup> C Serial Data Line   | I/O<br>I<br>I/O             | V <sub>DDE1</sub>    | SH                    | —                                | —                               | 93                    | 117 | F16 |
| PD10               | 58                          | PD10<br>PCS_B2<br>CNTX_F<br>NMIO             | GPIO<br>DSPI_B Peripheral Chip Select<br>CAN_F Transmit<br>NMI Input for Z1 Core                                       | I/O<br>O<br>O<br>I          | V <sub>DDE1</sub>    | SH                    | —                                | —                               | 92                    | 116 | G14 |
| PD11               | 59                          | PD11<br>PCS_B1<br>CNRX_F<br>NMI1             | GPIO<br>DSPI_B Peripheral Chip Select<br>CAN_F Receive<br>NMI Input for Z0 Core  | I/O<br>O<br>I<br>I          | V <sub>DDE1</sub>    | SH                    | —                                | —                               | 91                    | 115 | G15 |
| PD12               | 60                          | PD12<br>PCS_B0<br>eMIOS9                     | GPIO<br>DSPI_B Peripheral Chip Select<br>eMIOS Channel   | I/O<br>I/O<br>O             | V <sub>DDE1</sub>    | SH                    | —                                | —                               | 90                    | 114 | H14 |
| PD13               | 61                          | PD13<br>SCK_B<br>eMIOS8                      | GPIO<br>DSPI_B Clock<br>eMIOS Channel  | I/O<br>I/O<br>O             | V <sub>DDE1</sub>    | SH                    | —                                | —                               | 89                    | 113 | H15 |
| PD14               | 62                          | PD14<br>SOUT_B<br>eMIOS7                     | GPIO<br>DSPI_B Data Output<br>eMIOS Channel  | I/O<br>O<br>O               | V <sub>DDE1</sub>    | SH                    | —                                | —                               | 88                    | 110 | J14 |
| PD15               | 63                          | PD15<br>SIN_B<br>eMIOS6                      | GPIO<br>DSPI_B Data Input<br>eMIOS Channel   | I/O<br>I<br>O               | V <sub>DDE1</sub>    | SH                    | —                                | —                               | 87                    | 107 | K14 |
| <b>Port E (16)</b> |                             |  |  |                             |                      |                       |                                  |                                 |                       |     |     |
| PE0                | 64                          | PE0<br>PCS_A2<br>eMIOS5<br>MLBCLK            | GPIO<br>DSPI_A Peripheral Chip Select<br>eMIOS Channel<br>MLB Clock  | I/O<br>O<br>O<br>I          | V <sub>DDE1</sub>    | SH                    | —                                | —                               | 86                    | 106 | K16 |
| PE1                | 65                          | PE1<br>PCS_A1<br>eMIOS4<br>MLBSI /<br>MLBSIG | GPIO<br>DSPI_A Peripheral Chip Select<br>eMIOS Channel<br>MLB Signal In (5-pin) /<br>MLB Bi-directional Signal (3-pin) | I/O<br>O<br>O<br>I<br>I/O   | V <sub>DDE1</sub>    | MH                    | —                                | —                               | 85                    | 103 | L14 |
| PE2                | 66                          | PE2<br>PCS_A0<br>eMIOS3<br>MLBDI /<br>MLBDAT | GPIO<br>DSPI_A Peripheral Chip Select<br>eMIOS Channel<br>MLB Data In (5-pin) /<br>MLB Bi-directional Data (3-pin)     | I/O<br>I/O<br>O<br>I<br>I/O | V <sub>DDE1</sub>    | MH                    | —                                | —                               | 84                    | 101 | L15 |

Table 1. MPC5510 Signal Properties (continued)

| Pin Name           | GPIO (PCR) Num <sup>1</sup> | Supported Functions <sup>2</sup>                                   | Description  | I/O Type                         | Voltage <sup>3</sup> | Pad <sup>4</sup> Type | Status During Reset <sup>5</sup> | Status After Reset <sup>5</sup> | Package Pin Locations |     |     |
|--------------------|-----------------------------|--|--|----------------------------------|----------------------|-----------------------|----------------------------------|---------------------------------|-----------------------|-----|-----|
|                    |                             |  |  |                                  |                      |                       |                                  |                                 | 144                   | 176 | 208 |
| PE3                | 67                          | PE3<br>SCK_A<br>eMIOS2<br>MLBSO /<br>MLBSIG_BUFEN                  | GPIO<br>DSPI_A Clock<br>eMIOS Channel<br>MLB Signal Out (5-pin) /<br>MLB Signal Level Shifter Enable (3-pin)   | I/O<br>I/O<br>O<br>O<br>O        | V <sub>DDE1</sub>    | MH                    | —                                | —                               | 83                    | 100 | M13 |
| PE4                | 68                          | PE4<br>SOUT_A<br>eMIOS1<br>MLBDO /<br>MLBDAT_BUFEN                 | GPIO<br>DSPI_A Data Out<br>eMIOS Channel<br>MLB Data Out (5-pin) /<br>MLB Data Level Shifter Enable (3-pin)  | I/O<br>O<br>O<br>O<br>O          | V <sub>DDE1</sub>    | MH                    | —                                | —                               | 82                    | 98  | N14 |
| PE5                | 69                          | PE5<br>SIN_A<br>eMIOS0<br>MLB_SLOT /<br>MLB_SIGOBS /<br>MLB_DATOBS | GPIO<br>DSPI_A Data In<br>eMIOS Channel<br>MLB Slot Debug /<br>MLB Clock Adjust Observe Signal /<br>MLB Clock Adjust Observe Data                      | I/O<br>I<br>O<br>O<br>O<br>O     | V <sub>DDE1</sub>    | MH                    | —                                | —                               | 81                    | 97  | M15 |
| PE6                | 70                          | PE6<br>CLKOUT  | GPIO<br>System Clock Output  | I/O<br>O                         | V <sub>DDE3</sub>    | MH                    | —                                | —                               | 67                    | 83  | P13 |
| PE7                | 71                          | PE7  | GPIO   | I/O                              | V <sub>DDE1</sub>    | SH                    | —                                | —                               | —                     | —   | H13 |
| PE8                | 72                          | PE8  | GPIO   | I/O                              | V <sub>DDE1</sub>    | SH                    | —                                | —                               | —                     | —   | H16 |
| PE9                | 72                          | PE9  | GPIO   | I/O                              | V <sub>DDE1</sub>    | SH                    | —                                | —                               | —                     | —   | J13 |
| PE10               | 74                          | PE10   | GPIO   | I/O                              | V <sub>DDE1</sub>    | SH                    | —                                | —                               | —                     | 112 | J16 |
| PE11               | 75                          | PE11   | GPIO   | I/O                              | V <sub>DDE1</sub>    | SH                    | —                                | —                               | —                     | 111 | J15 |
| PE12               | 76                          | PE12   | GPIO   | I/O                              | V <sub>DDE1</sub>    | SH                    | —                                | —                               | —                     | 109 | K13 |
| PE13               | 77                          | PE13   | GPIO   | I/O                              | V <sub>DDE1</sub>    | SH                    | —                                | —                               | —                     | 108 | L13 |
| PE14               | 78                          | PE14   | GPIO   | I/O                              | V <sub>DDE1</sub>    | SH                    | —                                | —                               | —                     | 102 | L16 |
| PE15               | 79                          | PE15   | GPIO   | I/O                              | V <sub>DDE1</sub>    | SH                    | —                                | —                               | —                     | 99  | M14 |
| <b>Port F (16)</b> |                             |  |  |                                  |                      |                       |                                  |                                 |                       |     |     |
| PF0                | 80                          | PF0<br>RD_W $\overline{R}$<br>EVTI <sup>8</sup>                    | GPIO<br>EBI Read/Write<br>Nexus Event In   | I/O<br>I/O<br>I                  | V <sub>DDE3</sub>    | MH                    | —                                | —                               | 66                    | 82  | N12 |
| PF1                | 81                          | PF1<br>$\overline{T}$ A<br>MLBCLK<br>EVTO <sup>8</sup>             | GPIO<br>EBI Transfer Acknowledge<br>MLB Clock<br>Nexus Event Out   | I/O<br>I/O<br>I<br>O             | V <sub>DDE3</sub>    | MH                    | —                                | —                               | 65                    | 81  | P12 |
| PF2                | 82                          | PF2<br>AD8<br>ADDR8<br>MLBSI /<br>MLBSIG<br>MSEO <sup>8</sup>      | GPIO<br>EBI Muxed Address/Data<br>EBI Non Muxed Address<br>MLB Signal In (5-pin) /<br>MLB Bi-Directional Signal (3-pin)<br>Nexus Message Start/End Out | I/O<br>I/O<br>O<br>I<br>I/O<br>O | V <sub>DDE3</sub>    | MH                    | —                                | —                               | 64                    | 80  | R12 |



Table 1. MPC5510 Signal Properties (continued)

| Pin Name | GPIO (PCR) Num <sup>1</sup> | Supported Functions <sup>2</sup>   | Description   | I/O Type                            | Voltage <sup>3</sup> | Pad <sup>4</sup> Type | Status During Reset <sup>5</sup> | Status After Reset <sup>5</sup> | Package Pin Locations |     |     |
|----------|-----------------------------|--|---|-------------------------------------|----------------------|-----------------------|----------------------------------|---------------------------------|-----------------------|-----|-----|
|          |                             |  |   |                                     |                      |                       |                                  |                                 | 144                   | 176 | 208 |
| PF3      | 83                          | PF3<br>AD9<br>ADDR9<br>MLBDI /<br>MLBDAT<br>MCKO <sup>8</sup>                          | GPIO<br>EBI Muxed Address/Data<br>EBI Non Muxed Address<br>MLB Data In (5-pin) /<br>MLB Bi-directional Data (3-pin)<br>Nexus Message Clock Out                              | I/O<br>I/O<br>O<br>I<br>I/O<br>O    | V <sub>DDE3</sub>    | MH                    | —                                | —                               | 63                    | 79  | T12 |
| PF4      | 84                          | PF4<br>AD10<br>ADDR10<br>MLBSO /<br>MLBSIG_BUFEN<br>MDO0 <sup>8</sup>                  | GPIO<br>EBI Muxed Address/Data<br>EBI Non Muxed Address<br>MLB Signal Out (5-pin) /<br>MLB Signal Level Shifter Enable (3-pin)<br>Nexus Message Data Out                    | I/O<br>I/O<br>O<br>O<br>O<br>O      | V <sub>DDE3</sub>    | MH                    | —                                | —                               | 59                    | 74  | T10 |
| PF5      | 85                          | PF5<br>AD11<br>ADDR11<br>MLBDO /<br>MLBDAT_BUFEN<br>MDO1 <sup>8</sup>                  | GPIO<br>EBI Muxed Address/Data<br>EBI Non Muxed Address<br>MLB Data Out (5-pin) /<br>MLB Data Level Shifter Enable (3-pin)<br>Nexus Message Data Out                        | I/O<br>I/O<br>O<br>O<br>O<br>O      | V <sub>DDE3</sub>    | MH                    | —                                | —                               | 58                    | 72  | R9  |
| PF6      | 86                          | PF6<br>AD12<br>ADDR12<br>MLB_SLOT /<br>MLB_SIGOBS /<br>MLB_DATOBS<br>MDO2 <sup>8</sup> | GPIO<br>EBI Muxed Address/Data<br>EBI Non Muxed Address<br>MLB Slot Debug /<br>MLB Clock Adjust Observe Signal /<br>MLB Clock Adjust Observe Data<br>Nexus Message Data Out | I/O<br>I/O<br>O<br>O<br>O<br>O<br>O | V <sub>DDE3</sub>    | MH                    | —                                | —                               | 57                    | 68  | T8  |
| PF7      | 87                          | PF7<br>AD13<br>ADDR13<br>MDO3 <sup>8</sup>   | GPIO<br>EBI Muxed Address/Data<br>EBI Non Muxed Address<br>Nexus Message Data Out   | I/O<br>I/O<br>O<br>O                | V <sub>DDE3</sub>    | MH                    | —                                | —                               | 56                    | 66  | P8  |
| PF8      | 88                          | PF8<br>AD14<br>ADDR14<br>MDO4 <sup>8</sup>   | GPIO<br>EBI Muxed Address/Data<br>EBI Non Muxed Address<br>Nexus Message Data Out   | I/O<br>I/O<br>O<br>O                | V <sub>DDE2</sub>    | MH                    | —                                | —                               | 55                    | 65  | N8  |
| PF9      | 89                          | PF9<br>AD15<br>ADDR15<br>MDO5 <sup>8</sup>   | GPIO<br>EBI Muxed Address/Data<br>EBI Non Muxed Address<br>Nexus Message Data Out   | I/O<br>I/O<br>O<br>O                | V <sub>DDE2</sub>    | MH                    | —                                | —                               | 54                    | 64  | T7  |
| PF10     | 90                          | PF10<br>$\overline{CS1}$<br>TXD_C<br>MDO6 <sup>8</sup>                                 | GPIO<br>EBI Chip Select<br>SCI_C Transmit<br>Nexus Message Data Out   | I/O<br>O<br>O<br>O                  | V <sub>DDE2</sub>    | MH                    | —                                | —                               | 52                    | 62  | R7  |
| PF11     | 91                          | PF11<br>$\overline{CS0}$<br>RXD_C<br>MDO7 <sup>8</sup>                                 | GPIO<br>EBI Chip Select<br>SCI_C Receive<br>Nexus Message Data Out  | I/O<br>O<br>I<br>O                  | V <sub>DDE2</sub>    | MH                    | —                                | —                               | 51                    | 61  | P7  |
| PF12     | 92                          | PF12<br>$\overline{TS}$<br>TXD_D<br>ALE  | GPIO<br>EBI Transfer Start<br>SCI_D Transmit<br>EBI Address Latch Enable  | I/O<br>I/O<br>O<br>O                | V <sub>DDE2</sub>    | MH                    | —                                | —                               | 50                    | 60  | N7  |

Table 1. MPC5510 Signal Properties (continued)

| Pin Name           | GPIO (PCR) Num <sup>1</sup> | Supported Functions <sup>2</sup>           | Description  | I/O Type                 | Voltage <sup>3</sup> | Pad <sup>4</sup> Type | Status During Reset <sup>5</sup> | Status After Reset <sup>5</sup> | Package Pin Locations |     |     |
|--------------------|-----------------------------|--|--|--------------------------|----------------------|-----------------------|----------------------------------|---------------------------------|-----------------------|-----|-----|
|                    |                             |  |  |                          |                      |                       |                                  |                                 | 144                   | 176 | 208 |
| PF13               | 93                          | PF13<br>$\overline{OE}$<br>RXD_D           | GPIO<br>EBI Output Enable<br>SCI_D Receive                                       | I/O<br>O<br>I            | V <sub>DDE2</sub>    | MH                    | —                                | —                               | 49                    | 59  | R6  |
| PF14               | 94                          | PF14<br>$\overline{WE0}$<br>BDIP<br>CNTX_D | GPIO<br>EBI Write Enable<br>EBI Burst Data In Progress<br>CAN_D Transmit         | I/O<br>O<br>O<br>O       | V <sub>DDE2</sub>    | MH                    | —                                | —                               | 45                    | 55  | P6  |
| PF15               | 95                          | PF15<br>$\overline{WE1}$<br>TEA<br>CNRX_D  | GPIO<br>EBI Write Enable<br>EBI Transfer Error Acknowledge<br>CAN_D Receive      | I/O<br>O<br>I/O<br>I     | V <sub>DDE2</sub>    | MH                    | —                                | —                               | 44                    | 54  | N6  |
| <b>Port G (16)</b> |                             |  |  |                          |                      |                       |                                  |                                 |                       |     |     |
| PG0                | 96                          | PG0<br>AD16<br>eMIOS16                     | GPIO<br>EBI Muxed Address/Data<br>eMIOS Channel                                  | I/O<br>I/O<br>I/O        | V <sub>DDE2</sub>    | MH                    | —                                | —                               | 43                    | 51  | P5  |
| PG1                | 97                          | PG1<br>AD17<br>eMIOS17<br>SIN_C            | GPIO<br>EBI Muxed Address/Data<br>eMIOS Channel<br>DSPI_C Serial In              | I/O<br>I/O<br>I/O<br>I   | V <sub>DDE2</sub>    | MH                    | —                                | —                               | 42                    | 50  | T4  |
| PG2                | 98                          | PG2<br>AD18<br>eMIOS18<br>SOUT_C           | GPIO<br>EBI Muxed Address/Data<br>eMIOS Channel<br>DSPI_C Serial Out             | I/O<br>I/O<br>I/O<br>O   | V <sub>DDE2</sub>    | MH                    | —                                | —                               | 41                    | 49  | R4  |
| PG3                | 99                          | PG3<br>AD19<br>eMIOS19<br>SCK_C            | GPIO<br>EBI Muxed Address/Data<br>eMIOS Channel<br>DSPI_C Serial Clock           | I/O<br>I/O<br>I/O<br>I/O | V <sub>DDE2</sub>    | MH                    | —                                | —                               | 40                    | 48  | P4  |
| PG4                | 100                         | PG4<br>AD20<br>eMIOS20<br>PCS_C0           | GPIO<br>EBI Muxed Address/Data<br>eMIOS Channel<br>DSPI_C Peripheral Chip Select | I/O<br>I/O<br>I/O<br>I/O | V <sub>DDE2</sub>    | MH                    | —                                | —                               | 39                    | 47  | T3  |
| PG5                | 101                         | PG5<br>AD21<br>eMIOS21                     | GPIO<br>EBI Muxed Address/Data<br>eMIOS Channel                                  | I/O<br>I/O<br>I/O        | V <sub>DDE2</sub>    | MH                    | —                                | —                               | 38                    | 46  | R3  |
| PG6                | 102                         | PG6<br>AD22<br>eMIOS22                     | GPIO<br>EBI Muxed Address/Data<br>eMIOS Channel                                  | I/O<br>I/O<br>I/O        | V <sub>DDE2</sub>    | MH                    | —                                | —                               | 37                    | 45  | T2  |
| PG7                | 103                         | PG7<br>AD23<br>eMIOS23<br>RXD_C            | GPIO<br>EBI Muxed Address/Data<br>eMIOS Channel<br>SCI_C Receive                 | I/O<br>I/O<br>I/O<br>I   | V <sub>DDE2</sub>    | MH                    | —                                | —                               | 36                    | 44  | R1  |
| PG8                | 104                         | PG8<br>AD24<br>PCS_A4                      | GPIO<br>EBI Muxed Address/Data<br>DSPI_A Peripheral Chip Select                  | I/O<br>I/O<br>O          | V <sub>DDE2</sub>    | MH                    | —                                | —                               | 35                    | 43  | P2  |

Table 1. MPC5510 Signal Properties (continued)

| Pin Name           | GPIO (PCR) Num <sup>1</sup> | Supported Functions <sup>2</sup> | Description   | I/O Type             | Voltage <sup>3</sup> | Pad <sup>4</sup> Type | Status During Reset <sup>5</sup> | Status After Reset <sup>5</sup> | Package Pin Locations |     |     |
|--------------------|-----------------------------|----------------------------------|---|----------------------|----------------------|-----------------------|----------------------------------|---------------------------------|-----------------------|-----|-----|
|                    |                             |                                  |   |                      |                      |                       |                                  |                                 | 144                   | 176 | 208 |
| PG9                | 105                         | PG9<br>AD25<br>PCS_A3<br>TXD_C   | GPIO<br>EBI Muxed Address/Data<br>DSPI_A Peripheral Chip Select<br>SCI_C Transmit           | I/O<br>I/O<br>O<br>O | V <sub>DDE2</sub>    | MH                    | —                                | —                               | 34                    | 42  | N3  |
| PG10               | 106                         | PG10<br>AD26<br>PCS_A2           | GPIO<br>EBI Muxed Address/Data<br>DSPI_A Peripheral Chip Select                             | I/O<br>I/O<br>O      | V <sub>DDE2</sub>    | MH                    | —                                | —                               | 30                    | 38  | N2  |
| PG11               | 107                         | PG11<br>AD27<br>PCS_A1           | GPIO<br>EBI Muxed Address/Data<br>DSPI_A Peripheral Chip Select                             | I/O<br>I/O<br>O      | V <sub>DDE2</sub>    | MH                    | —                                | —                               | 29                    | 37  | N1  |
| PG12               | 108                         | PG12<br>AD28<br>PCS_A0           | GPIO<br>EBI Muxed Address/Data<br>DSPI_A Peripheral Chip Select                             | I/O<br>I/O<br>I/O    | V <sub>DDE2</sub>    | MH                    | —                                | —                               | 28                    | 36  | M4  |
| PG13               | 109                         | PG13<br>AD29<br>SCK_A            | GPIO<br>EBI Muxed Address/Data<br>DSPI_A Clock  | I/O<br>I/O<br>I/O    | V <sub>DDE2</sub>    | MH                    | —                                | —                               | 27                    | 35  | M3  |
| PG14               | 110                         | PG14<br>AD30<br>SOUT_A           | GPIO<br>EBI Muxed Address/Data<br>DSPI_A Data Out   | I/O<br>I/O<br>O      | V <sub>DDE2</sub>    | MH                    | —                                | —                               | 26                    | 34  | M2  |
| PG15               | 111                         | PG15<br>AD31<br>SIN_A            | GPIO<br>EBI Muxed Address/Data<br>DSPI_A Data In  | I/O<br>I/O<br>I      | V <sub>DDE2</sub>    | MH                    | —                                | —                               | 25                    | 33  | M1  |
| <b>Port H (16)</b> |                             |                                  |   |                      |                      |                       |                                  |                                 |                       |     |     |
| PH0                | 112                         | PH0<br>AN27<br>eMIOS20<br>SCL_A  | GPIO<br>eQADC Analog Input <sup>7</sup><br>eMIOS Channel<br>I <sup>2</sup> C_A Serial Clock | I/O<br>I<br>O<br>I/O | V <sub>DDE2</sub>    | A + SH                | —                                | —                               | 24                    | 32  | L3  |
| PH1                | 113                         | PH1<br>AN26<br>eMIOS21<br>SDA_A  | GPIO<br>eQADC Analog Input <sup>7</sup><br>eMIOS Channel<br>I <sup>2</sup> C_A Serial Data  | I/O<br>I<br>O<br>I/O | V <sub>DDE2</sub>    | A + SH                | —                                | —                               | 23                    | 31  | L2  |
| PH2                | 114                         | PH2<br>AN25<br>eMIOS22<br>CS3    | GPIO<br>eQADC Analog Input <sup>7</sup><br>eMIOS Channel<br>EBI Chip Select                 | I/O<br>I<br>O<br>O   | V <sub>DDE2</sub>    | A + MH                | —                                | —                               | 22                    | 30  | L1  |
| PH3                | 115                         | PH3<br>AN24<br>eMIOS23<br>CS2    | GPIO<br>eQADC Analog Input <sup>7</sup><br>eMIOS Channel<br>EBI Chip Select                 | I/O<br>I<br>O<br>O   | V <sub>DDE2</sub>    | A + MH                | —                                | —                               | 21                    | 29  | K4  |
| PH4                | 116                         | PH4<br>AN23<br>TXD_E<br>MA2      | GPIO<br>eQADC Analog Input <sup>7</sup><br>SCI_E Transmit<br>eQADC External Mux Address     | I/O<br>I<br>O<br>O   | V <sub>DDE2</sub>    | A + SH                | —                                | —                               | 20                    | 28  | K3  |
| PH5                | 117                         | PH5<br>AN22<br>RXD_E<br>MA1      | GPIO<br>eQADC Analog Input <sup>7</sup><br>SCI_E Receive<br>eQADC External Mux Address      | I/O<br>I<br>I<br>O   | V <sub>DDE2</sub>    | A + SH                | —                                | —                               | 19                    | 24  | J3  |

Table 1. MPC5510 Signal Properties (continued)

| Pin Name           | GPIO (PCR) Num <sup>1</sup> | Supported Functions <sup>2</sup> | Description   | I/O Type           | Voltage <sup>3</sup> | Pad <sup>4</sup> Type | Status During Reset <sup>5</sup> | Status After Reset <sup>5</sup> | Package Pin Locations |     |     |
|--------------------|-----------------------------|----------------------------------|---|--------------------|----------------------|-----------------------|----------------------------------|---------------------------------|-----------------------|-----|-----|
|                    |                             |                                  |   |                    |                      |                       |                                  |                                 | 144                   | 176 | 208 |
| PH6                | 118                         | PH6<br>AN21<br>TXD_F             | GPIO<br>eQADC Analog Input <sup>7</sup><br>SCI_F Transmit                               | I/O<br>I<br>O      | V <sub>DDE2</sub>    | A + SH                | —                                | —                               | 18                    | 23  | J2  |
| PH7                | 119                         | PH7<br>AN20<br>RXD_F             | GPIO<br>eQADC Analog Input <sup>7</sup><br>SCI_F Receive                                | I/O<br>I<br>I      | V <sub>DDE2</sub>    | A + SH                | —                                | —                               | 17                    | 22  | J1  |
| PH8                | 120                         | PH8<br>AN19<br>CNTX_E<br>MA0     | GPIO<br>eQADC Analog Input <sup>7</sup><br>CAN_E Transmit<br>eQADC External Mux Address | I/O<br>I<br>O<br>O | V <sub>DDE2</sub>    | A + SH                | —                                | —                               | 14                    | 17  | H1  |
| PH9                | 121                         | PH9<br>AN18/ANT<br>CNRX_E        | GPIO<br>eQADC Analog Input <sup>7</sup><br>CAN_E Receive                                | I/O<br>I<br>I      | V <sub>DDE2</sub>    | A + SH                | —                                | —                               | 13                    | 14  | G2  |
| PH10               | 122                         | PH10<br>AN17/ANS<br>CNRX_F       | GPIO<br>eQADC Analog Input <sup>7</sup><br>CAN_F Receive                                | I/O<br>I<br>I      | V <sub>DDE2</sub>    | A + SH                | —                                | —                               | 12                    | 12  | F4  |
| PH11               | 123                         | PH11<br>AN16/ANR<br>CNTX_F       | GPIO<br>eQADC Analog Input <sup>7</sup><br>CAN_F Transmit                               | I/O<br>I<br>O      | V <sub>DDE2</sub>    | A + SH                | —                                | —                               | 11                    | 11  | F3  |
| PH12               | 124                         | PH12<br>PCS_D5                   | GPIO<br>DSPI_D Peripheral Chip Select   | I/O<br>O           | V <sub>DDE2</sub>    | SH                    | —                                | —                               | —                     | —   | F2  |
| PH13               | 125                         | PH13                             | GPIO  | I/O                | V <sub>DDE2</sub>    | SH                    | —                                | —                               | —                     | —   | F1  |
| PH14               | 126                         | PH14<br>WE2                      | GPIO<br>EBI Write Enable  | I/O<br>O           | V <sub>DDE2</sub>    | MH                    | —                                | —                               | —                     | 53  | T5  |
| PH15               | 127                         | PH15<br>WE3                      | GPIO<br>EBI Write Enable  | I/O<br>O           | V <sub>DDE2</sub>    | MH                    | —                                | —                               | —                     | 52  | R5  |
| <b>Port J (16)</b> |                             |                                  |   |                    |                      |                       |                                  |                                 |                       |     |     |
| PJ0                | 128                         | PJ0<br>AD0                       | GPIO<br>EBI Muxed Address/Data  | I/O<br>I/O         | V <sub>DDE3</sub>    | MH                    | —                                | —                               | —                     | —   | N11 |
| PJ1                | 129                         | PJ1<br>AD1                       | GPIO<br>EBI Muxed Address/Data  | I/O<br>I/O         | V <sub>DDE3</sub>    | MH                    | —                                | —                               | —                     | —   | P11 |
| PJ2                | 130                         | PJ2<br>AD2                       | GPIO<br>EBI Muxed Address/Data  | I/O<br>I/O         | V <sub>DDE3</sub>    | MH                    | —                                | —                               | —                     | —   | N10 |
| PJ3                | 131                         | PJ3<br>AD3                       | GPIO<br>EBI Muxed Address/Data  | I/O<br>I/O         | V <sub>DDE3</sub>    | MH                    | —                                | —                               | —                     | —   | R10 |
| PJ4                | 132                         | PJ4<br>AD4                       | GPIO<br>EBI Muxed Address/Data  | I/O<br>I/O         | V <sub>DDE3</sub>    | MH                    | —                                | —                               | —                     | 75  | P10 |
| PJ5                | 133                         | PJ5<br>AD5                       | GPIO<br>EBI Muxed Address/Data  | I/O<br>I/O         | V <sub>DDE3</sub>    | MH                    | —                                | —                               | —                     | 73  | T9  |
| PJ6                | 134                         | PJ6<br>AD6                       | GPIO<br>EBI Muxed Address/Data  | I/O<br>I/O         | V <sub>DDE3</sub>    | MH                    | —                                | —                               | —                     | 69  | P9  |
| PJ7                | 135                         | PJ7<br>AD7                       | GPIO<br>EBI Muxed Address/Data  | I/O<br>I/O         | V <sub>DDE3</sub>    | MH                    | —                                | —                               | —                     | 67  | R8  |

Table 1. MPC5510 Signal Properties (continued)

| Pin Name                      | GPIO (PCR) Num <sup>1</sup> | Supported Functions <sup>2</sup> | Description   | I/O Type   | Voltage <sup>3</sup> | Pad <sup>4</sup> Type | Status During Reset <sup>5</sup>    | Status After Reset <sup>5</sup> | Package Pin Locations |     |     |     |
|-------------------------------|-----------------------------|----------------------------------|---|------------|----------------------|-----------------------|-------------------------------------|---------------------------------|-----------------------|-----|-----|-----|
|                               |                             |                                  |   |            |                      |                       |                                     |                                 | 144                   | 176 | 208 |     |
| PJ8                           | 136                         | PJ8<br>PCS_D4                    | GPIO<br>DSPI_D Peripheral Chip Select                 | I/O<br>I/O | V <sub>DDE2</sub>    | SH                    | —                                   | —                               | —                     | 27  | K2  |     |
| PJ9                           | 137                         | PJ9<br>PCS_D3                    | GPIO<br>DSPI_D Peripheral Chip Select                 | I/O<br>I/O | V <sub>DDE2</sub>    | SH                    | —                                   | —                               | —                     | 26  | K1  |     |
| PJ10                          | 138                         | PJ10<br>PCS_D2                   | GPIO<br>DSPI_D Peripheral Chip Select                 | I/O<br>I/O | V <sub>DDE2</sub>    | SH                    | —                                   | —                               | —                     | 25  | J4  |     |
| PJ11                          | 139                         | PJ11<br>PCS_D1                   | GPIO<br>DSPI_D Peripheral Chip Select                 | I/O<br>I/O | V <sub>DDE2</sub>    | SH                    | —                                   | —                               | —                     | 19  | H3  |     |
| PJ12                          | 140                         | PJ12<br>PCS_D0                   | GPIO<br>DSPI_D Peripheral Chip Select                 | I/O<br>I/O | V <sub>DDE2</sub>    | SH                    | —                                   | —                               | —                     | 18  | H2  |     |
| PJ13                          | 141                         | PJ13<br>SCK_D                    | GPIO<br>DSPI_D Clock                                  | I/O<br>I/O | V <sub>DDE2</sub>    | SH                    | —                                   | —                               | —                     | 16  | G4  |     |
| PJ14                          | 142                         | PJ14<br>SOUT_D                   | GPIO<br>DSPI_D Serial Out                             | I/O<br>O   | V <sub>DDE2</sub>    | SH                    | —                                   | —                               | —                     | 15  | G3  |     |
| PJ15                          | 143                         | PJ15<br>SIN_D                    | GPIO<br>DSPI_D Serial In                              | I/O<br>I   | V <sub>DDE2</sub>    | SH                    | —                                   | —                               | —                     | 13  | G1  |     |
| <b>Port K (2)</b>             |                             |                                  |   |            |                      |                       |                                     |                                 |                       |     |     |     |
| PK0                           | 144                         | PK0<br>EXTAL32                   | GPIO<br>32 kHz Crystal Oscillator Input               | I<br>I     | V <sub>DDA</sub>     | AE + IH               | —                                   | —                               | —                     | 168 | B6  |     |
| PK1                           | 145                         | PK1<br>XTAL32                    | GPIO<br>32 kHz Crystal Oscillator Output              | I<br>O     | V <sub>DDA</sub>     | AE + IH               | —                                   | —                               | —                     | 166 | A6  |     |
| <b>Miscellaneous Pins (9)</b> |                             |                                  |   |            |                      |                       |                                     |                                 |                       |     |     |     |
| EXTAL                         | —                           | EXTAL<br>EXTCLK                  | Main Crystal Oscillator Input<br>External Clock Input | I<br>I     | V <sub>DDSYN</sub>   | AE                    | EXTAL                               |                                 |                       | 75  | 91  | N16 |
| XTAL                          | —                           | XTAL                             | Main Crystal Oscillator Output                        | O          | V <sub>DDSYN</sub>   | AE                    | XTAL                                |                                 |                       | 74  | 90  | P16 |
| TMS                           | —                           | TMS                              | JTAG Test Mode Select Input                           | I          | V <sub>DDE3</sub>    | SH                    | TMS (Pull Up)                       |                                 |                       | 72  | 88  | T15 |
| TCK                           | —                           | TCK                              | JTAG Test Clock Input                                 | I          | V <sub>DDE3</sub>    | IH                    | TCK (Pull Down)                     |                                 |                       | 71  | 87  | R14 |
| TDO                           | —                           | TDO                              | JTAG Test Data Output                                 | O          | V <sub>DDE3</sub>    | MH                    | TDO (Pull Up <sup>9</sup> )         |                                 |                       | 70  | 86  | T14 |
| TDI                           | —                           | TDI                              | JTAG Test Data Input                                  | I          | V <sub>DDE3</sub>    | IH                    | TDI (Pull Up)                       |                                 |                       | 69  | 85  | R13 |
| JCOMP                         | —                           | JCOMP                            | JTAG Compliancy                                       | I          | V <sub>DDE3</sub>    | IH                    | JCOMP (Pull Down)                   |                                 |                       | 68  | 84  | T13 |
| TEST <sup>10</sup>            | —                           | TEST                             | Test Mode Select                                      | I          | V <sub>DDE3</sub>    | IH                    | TEST                                |                                 |                       | 62  | 78  | R11 |
| $\overline{\text{RESET}}$     | —                           | $\overline{\text{RESET}}$        | External Reset  | I/O        | V <sub>DDE2</sub>    | SH                    | $\overline{\text{RESET}}$ (Pull Up) |                                 |                       | 10  | 10  | E4  |

<sup>1</sup> The GPIO number is the same as the corresponding pad configuration register (SIU\_PCR*n*) number.

<sup>2</sup> This column lists the functions associated with the programming of the SIU\_PCR*n*[PA] bit in the following order: GPIO, function 1, function 2, and function 3. The unused functions by a given pin begin with function 3, then function 2, then function 1.

<sup>3</sup> These are nominal voltages. Each segment provides the power and ground for the given set of I/O pins.

<sup>4</sup> Pad types: SH - Bi-directional slow speed pad with input hysteresis; MH - Bi-directional medium speed pad with input hysteresis; IH - Input only pad with input hysteresis; AE/A - Analog pad.

<sup>5</sup> A dash for the function in this column denotes the input and output buffer are turned off.

- <sup>6</sup> Port A[14:15]—EXTAL32 and XTAL32 functions only apply on the 144LQFP. These functions are on PortK[0:1] for the 176LQFP and 208BGA. In the 176 LQFP and 208 BGA packages, activity on PA14 should be minimized if the 32kHz XTAL is enabled.
- <sup>7</sup> This analog input pin has reduced analog-to-digital conversion accuracy compared to PA0–PA15. See eQADC spec #11 (Total Unadjusted Error for single ended conversions with calibration) for further notes on this.
- <sup>8</sup> The NEXUS function is selected when the JTAG TAP controller is enabled via the JCOMP pin and the appropriate bits in the NP PCR register. The value of the PA field in the associated PCR register has no effect on the pin function when the NEXUS function is selected.
- <sup>9</sup> Pullup is enabled only when JCOMP is negated.
- <sup>10</sup> Always connect the TEST pin to Ground (V<sub>SS</sub>).

## 1.2 Power and Ground Supply Summary

Table 2. MPC5510 Power/Ground

| Pin Name                          | Function Description             | Voltage <sup>1</sup> | Package Pin Locations |                     |   |
|-----------------------------------|----------------------------------|----------------------|-----------------------|---------------------|---|
|                                   |                                  |                      | 144                   | 176                 | 208   |
| V <sub>DDR</sub>                  | Voltage Regulator Supply         | 5.0 V                | 46                    | 56                  | T6  |
| V <sub>DDA</sub>                  | Analog Power                     | 5.0 V                | 144                   | 176                 | A2  |
| V <sub>RH</sub> <sup>2</sup>      | eQADC Voltage Reference High     | 5.0 V                |                       |                     | B3  |
| V <sub>SSA</sub>                  | Analog Ground                    | –                    | 141                   | 173                 | A4  |
| V <sub>RL</sub> <sup>3</sup>      | eQADC Voltage Reference Low      | –                    |                       |                     | B4  |
| REFBYPC                           | eQADC Reference Bypass Capacitor | V <sub>SSA</sub>     | 1                     | 1                   | B1  |
| V <sub>PP</sub> <sup>4</sup>      | Flash Program/Erase Power        | 5.0 V                | 78                    | 94                  | P15   |
| V <sub>DDSYN</sub> <sup>5</sup>   | Clock Synthesizer Power          | 3.3 V                | 73                    | 89                  | R16   |
| V <sub>SSSYN</sub>                | Clock Synthesizer Ground         | –                    | 76                    | 92                  | M16   |
| V <sub>DDE1</sub>                 | External I/O Power               | 3.3 V –<br>5.0 V     | 96,119                | 105,120,<br>143,155 | A15,D10,E13,<br>G16,K15   |
| V <sub>DDE2</sub>                 |                                  |                      | 16,33,48              | 21,41,58            | H4,L4,N5,P1   |
| V <sub>DDE3</sub>                 |                                  |                      | 61                    | 71,77               | N9,T11  |
| V <sub>SSE1</sub>                 | External I/O Ground              | –                    | 95,118                | 104,119,<br>142,154 | Shorted to V <sub>SS</sub> in<br>the package                        |
| V <sub>SSE2</sub>                 |                                  |                      | 15,32,47              | 20,40,57            | Shorted to V <sub>SS</sub> in<br>the package                        |
| V <sub>SSE3</sub>                 |                                  |                      | 60                    | 70,76               | Shorted to V <sub>SS</sub> in<br>the package                        |
| V <sub>DD33</sub> <sup>5</sup>    | 3.3 V I/O Power                  | 3.3 V                | 77                    | 93                  | N15   |
| V <sub>FLASH</sub> <sup>5,6</sup> | Flash Read Power                 |                      |                       |                     |   |
| V <sub>DD</sub> <sup>5</sup>      | Internal Logic Power             | 1.5 V                | 31,53,79              | 39,63,95            | A1,A16,B2,B15,<br>R2,R15,T1,T16                                     |
| V <sub>DDF</sub> <sup>5</sup>     | Flash Internal Logic Power       |                      |                       |                     | 79  |
| V <sub>SS</sub>                   | Ground                           | –                    | 80                    | 96                  | C3,C14,D4,D13,<br>G7-G10,H7-H10,<br>J7-J10,K7-K10,<br>N4,N13,P3,P14 |
| V <sub>SSF</sub>                  | Flash Internal Logic Ground      |                      |                       |                     | Shorted to V <sub>SS</sub> in<br>the package                        |

<sup>1</sup> These are nominal voltages.

<sup>2</sup> V<sub>RH</sub> is shorted to V<sub>DDA</sub> in the 144LQFP and 176 LQFP packages.

## Pin Assignments and Reset States

- <sup>3</sup>  $V_{RL}$  is shorted to  $V_{SSA}$  in the 144LQFP and 176 LQFP packages.
- <sup>4</sup>  $V_{PP}$  requires 5V for program/erase operations, but may be 0-5V otherwise.  $V_{PP}$  should not go high or low when the device is in Sleep mode.
- <sup>5</sup> Voltage generated from internal voltage regulator and no external connection or load allowed except the required bypass capacitors.
- <sup>6</sup>  $V_{FLASH}$  is shorted to  $V_{DD33}$  in the package.

# 1.3 Pinout – 144 LQFP

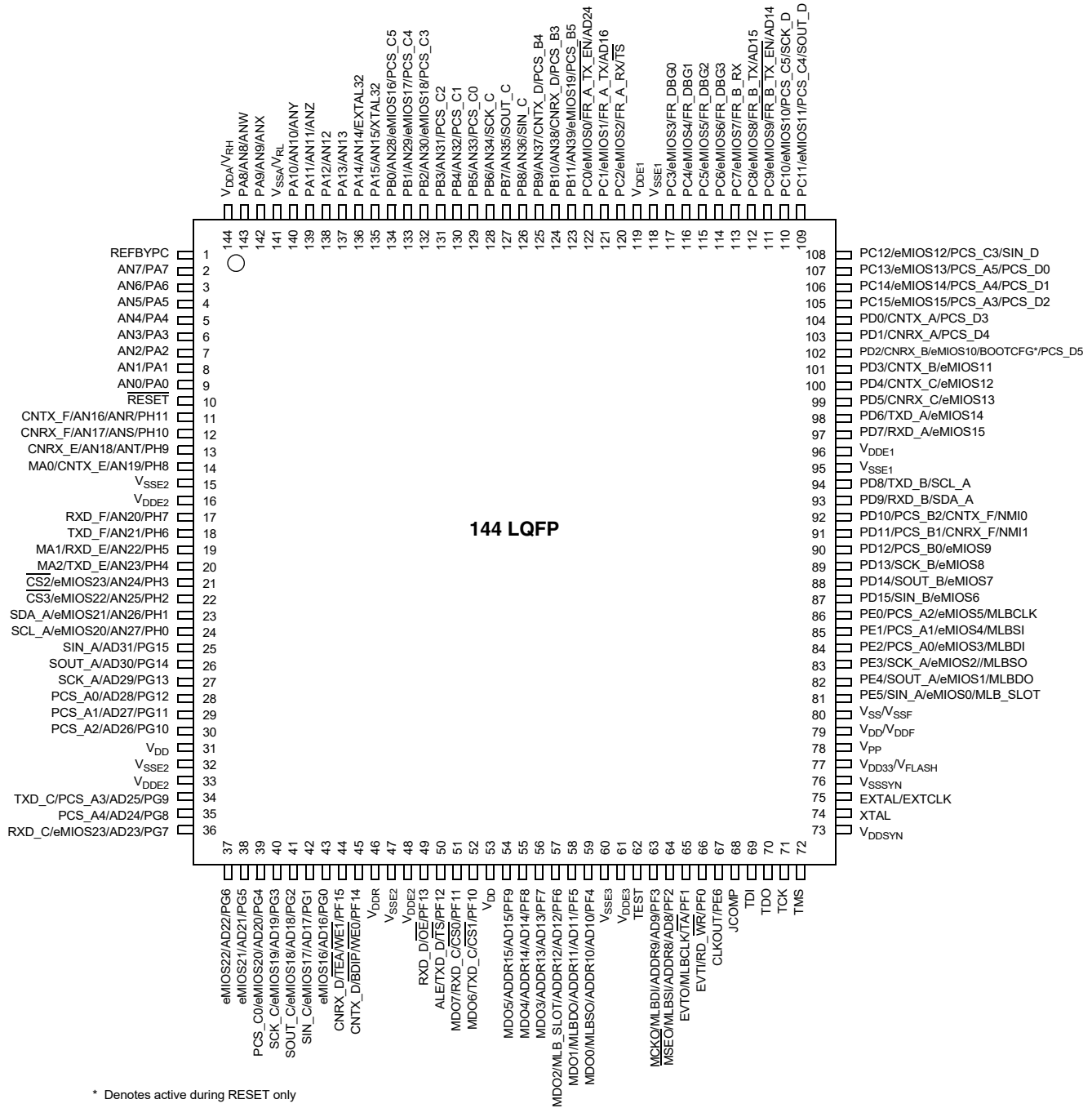


Figure 2. MPC5510 Pinout – 144 LQFP



# 1.4 Pinout – 176 LQFP

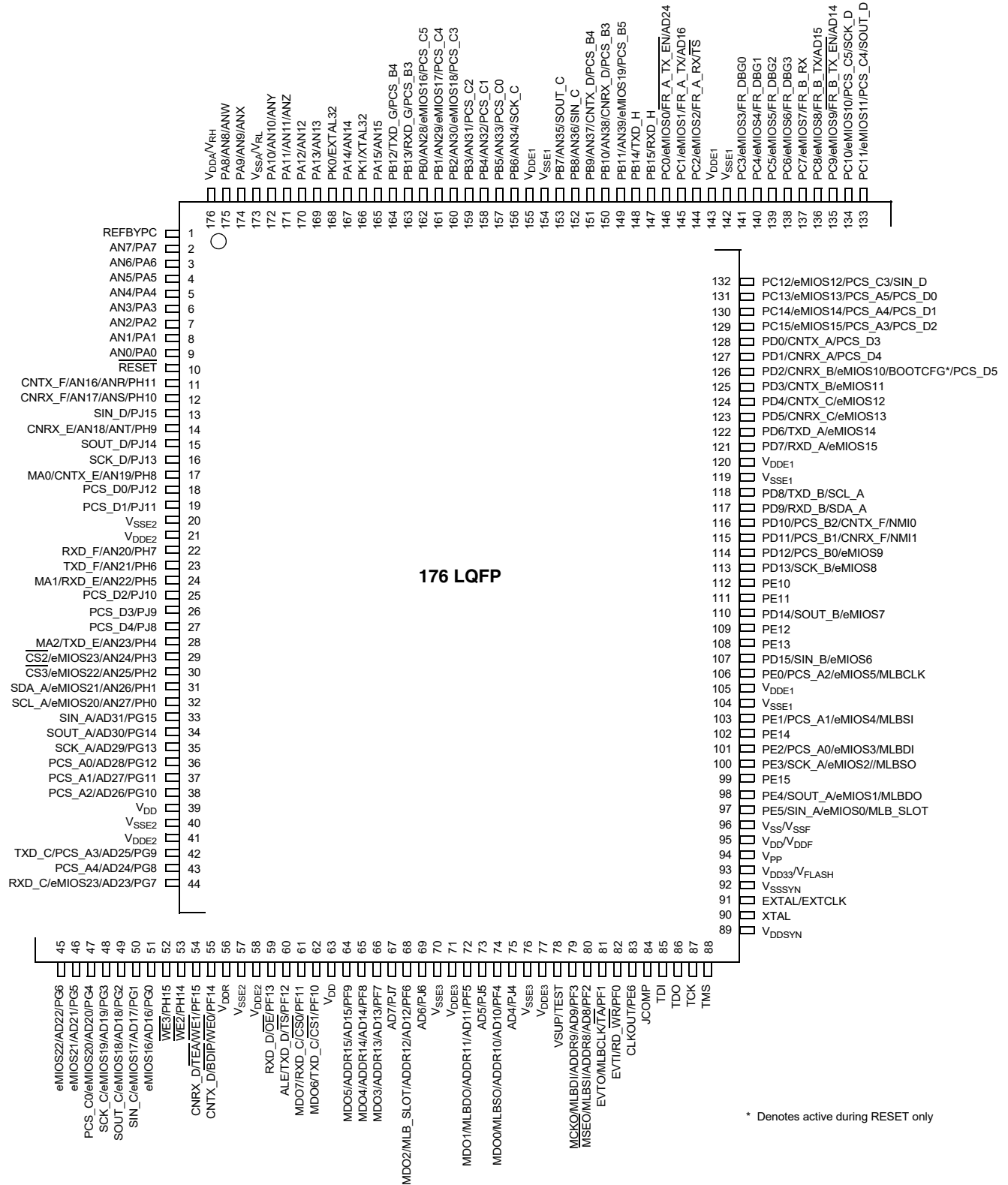


Figure 3. MPC5510 Pinout – 176 LQFP

# 1.5 Pinout – 208 PBGA

|                 | 1                 | 2                | 3               | 4                 | 5   | 6                | 7    | 8   | 9                 | 10                | 11                | 12  | 13              | 14              | 15                | 16                 |                 |                 |                 |                 |                 |                 |                 |                 |                 |                 |                 |                 |                   |     |     |     |   |
|-----------------|-------------------|------------------|-----------------|-------------------|---|------------------|------|-----|-------------------|-------------------|-------------------|-----|-----------------|-----------------|-------------------|--------------------|-----------------|-----------------|-----------------|-----------------|-----------------|-----------------|-----------------|-----------------|-----------------|-----------------|-----------------|-----------------|-------------------|-----|-----|-----|---|
| A               | V <sub>DD</sub>   | V <sub>DDA</sub> | PA8             | V <sub>SSA</sub>  | PA13  | PK1              | PB12 | PB2 | PB6               | PB10              | PB15              | PC3 | PC7             | PC10            | V <sub>DDE1</sub> | V <sub>DD</sub>    | A               |                 |                 |                 |                 |                 |                 |                 |                 |                 |                 |                 |                   |     |     |     |   |
| B               | REF BYPC          | V <sub>DD</sub>  | V <sub>RH</sub> | V <sub>RL</sub>   | PA12  | PK0              | PB13 | PB3 | PB7               | PB11              | PC0               | PC4 | PC8             | PC11            | V <sub>DD</sub>   | PC12               | B               |                 |                 |                 |                 |                 |                 |                 |                 |                 |                 |                 |                   |     |     |     |   |
| C               | PA7               | PA6              | V <sub>SS</sub> | PA9               | PA11  | PA15             | PB0  | PB4 | PB8               | PB14              | PC1               | PC5 | PC9             | V <sub>SS</sub> | PC13              | PC14               | C               |                 |                 |                 |                 |                 |                 |                 |                 |                 |                 |                 |                   |     |     |     |   |
| D               | PA5               | PA4              | PA3             | V <sub>SS</sub>   | PA10  | PA14             | PB1  | PB5 | PB9               | V <sub>DDE1</sub> | PC2               | PC6 | V <sub>SS</sub> | PC15            | PD0               | PD1                | D               |                 |                 |                 |                 |                 |                 |                 |                 |                 |                 |                 |                   |     |     |     |   |
| E               | PA2               | PA1              | PA0             | RESET             | <div style="text-align: center;"> <p><b>208 PBGA Ball Map</b><br/>(as viewed from top through the package)</p> <table border="1" style="margin: auto;"> <tr><td>V<sub>SS</sub></td><td>V<sub>SS</sub></td><td>V<sub>SS</sub></td><td>V<sub>SS</sub></td></tr> <tr><td>V<sub>SS</sub></td><td>V<sub>SS</sub></td><td>V<sub>SS</sub></td><td>V<sub>SS</sub></td></tr> <tr><td>V<sub>SS</sub></td><td>V<sub>SS</sub></td><td>V<sub>SS</sub></td><td>V<sub>SS</sub></td></tr> <tr><td>V<sub>SS</sub></td><td>V<sub>SS</sub></td><td>V<sub>SS</sub></td><td>V<sub>SS</sub></td></tr> </table> </div> |                  |      |     |                   |                   |                   |     | V <sub>SS</sub> | V <sub>SS</sub> | V <sub>SS</sub>   | V <sub>SS</sub>    | V <sub>SS</sub> | V <sub>SS</sub> | V <sub>SS</sub> | V <sub>SS</sub> | V <sub>SS</sub> | V <sub>SS</sub> | V <sub>SS</sub> | V <sub>SS</sub> | V <sub>SS</sub> | V <sub>SS</sub> | V <sub>SS</sub> | V <sub>SS</sub> | V <sub>DDE1</sub> | PD2 | PD3 | PD4 | E |
| V <sub>SS</sub> | V <sub>SS</sub>   | V <sub>SS</sub>  | V <sub>SS</sub> |                   |   |                  |      |     |                   |                   |                   |     |                 |                 |                   |                    |                 |                 |                 |                 |                 |                 |                 |                 |                 |                 |                 |                 |                   |     |     |     |   |
| V <sub>SS</sub> | V <sub>SS</sub>   | V <sub>SS</sub>  | V <sub>SS</sub> |                   |   |                  |      |     |                   |                   |                   |     |                 |                 |                   |                    |                 |                 |                 |                 |                 |                 |                 |                 |                 |                 |                 |                 |                   |     |     |     |   |
| V <sub>SS</sub> | V <sub>SS</sub>   | V <sub>SS</sub>  | V <sub>SS</sub> |                   |   |                  |      |     |                   |                   |                   |     |                 |                 |                   |                    |                 |                 |                 |                 |                 |                 |                 |                 |                 |                 |                 |                 |                   |     |     |     |   |
| V <sub>SS</sub> | V <sub>SS</sub>   | V <sub>SS</sub>  | V <sub>SS</sub> |                   |   |                  |      |     |                   |                   |                   |     |                 |                 |                   |                    |                 |                 |                 |                 |                 |                 |                 |                 |                 |                 |                 |                 |                   |     |     |     |   |
| F               | PH13              | PH12             | PH11            | PH10              |   |                  |      |     |                   |                   |                   |     | PD5             | PD6             | PD7               | PD9                | F               |                 |                 |                 |                 |                 |                 |                 |                 |                 |                 |                 |                   |     |     |     |   |
| G               | PJ15              | PH9              | PJ14            | PJ13              |   |                  |      |     |                   |                   |                   |     | PD8             | PD10            | PD11              | V <sub>DDE1</sub>  | G               |                 |                 |                 |                 |                 |                 |                 |                 |                 |                 |                 |                   |     |     |     |   |
| H               | PH8               | PJ12             | PJ11            | V <sub>DDE2</sub> |   |                  |      |     |                   |                   |                   |     | PE7             | PD12            | PD13              | PE8                | H               |                 |                 |                 |                 |                 |                 |                 |                 |                 |                 |                 |                   |     |     |     |   |
| J               | PH7               | PH6              | PH5             | PJ10              |   |                  |      |     |                   |                   |                   |     | PE9             | PD14            | PE11              | PE10               | J               |                 |                 |                 |                 |                 |                 |                 |                 |                 |                 |                 |                   |     |     |     |   |
| K               | PJ9               | PJ8              | PH4             | PH3               |   |                  |      |     |                   |                   |                   |     | PE12            | PD15            | V <sub>DDE1</sub> | PE0                | K               |                 |                 |                 |                 |                 |                 |                 |                 |                 |                 |                 |                   |     |     |     |   |
| L               | PH2               | PH1              | PH0             | V <sub>DDE2</sub> |   |                  |      |     |                   |                   |                   |     | PE13            | PE1             | PE2               | PE14               | L               |                 |                 |                 |                 |                 |                 |                 |                 |                 |                 |                 |                   |     |     |     |   |
| M               | PG15              | PG14             | PG13            | PG12              |   |                  |      |     |                   |                   |                   |     | PE3             | PE15            | PE5               | V <sub>SSSYN</sub> | M               |                 |                 |                 |                 |                 |                 |                 |                 |                 |                 |                 |                   |     |     |     |   |
| N               | PG11              | PG10             | PG9             | V <sub>SS</sub>   | V <sub>DDE2</sub>   | PF15             | PF12 | PF8 | V <sub>DDE3</sub> | PJ2               | PJ0               | PF0 | V <sub>SS</sub> | PE4             | V <sub>DD33</sub> | EXTAL              | N               |                 |                 |                 |                 |                 |                 |                 |                 |                 |                 |                 |                   |     |     |     |   |
| P               | V <sub>DDE2</sub> | PG8              | V <sub>SS</sub> | PG3               | PG0   | PF14             | PF11 | PF7 | PJ6               | PJ4               | PJ1               | PF1 | PE6             | V <sub>SS</sub> | V <sub>PP</sub>   | XTAL               | P               |                 |                 |                 |                 |                 |                 |                 |                 |                 |                 |                 |                   |     |     |     |   |
| R               | PG7               | V <sub>DD</sub>  | PG5             | PG2               | PH15  | PF13             | PF10 | PJ7 | PF5               | PJ3               | TEST              | PF2 | TDI             | TCK             | V <sub>DD</sub>   | V <sub>DDSYN</sub> | R               |                 |                 |                 |                 |                 |                 |                 |                 |                 |                 |                 |                   |     |     |     |   |
| T               | V <sub>DD</sub>   | PG6              | PG4             | PG1               | PH14  | V <sub>DDR</sub> | PF9  | PF6 | PJ5               | PF4               | V <sub>DDE3</sub> | PF3 | JCOMP           | TDO             | TMS               | V <sub>DD</sub>    | T               |                 |                 |                 |                 |                 |                 |                 |                 |                 |                 |                 |                   |     |     |     |   |

Figure 4. MPC5510 Pinout – 208 PBGA

## 2 Electrical Characteristics

This section contains detailed information on power considerations, DC/AC electrical characteristics, and AC timing specifications for the MCU.

### 2.1 Maximum Ratings

Table 3. Absolute Maximum Ratings<sup>1</sup>

| Num | Characteristic  | Symbol                                       | Min                  | Max <sup>2</sup>  | Unit |
|-----|---|--|----------------------|-------------------|------|
| 1   | 5.0V Voltage Regulator Reference Voltage  | $V_{DDR}$                                    | -0.3                 | 6.5               | V    |
| 2   | 5.0V Analog Supply Voltage (reference to $V_{SSA}$ )  | $V_{DDA}$                                    | -0.3                 | 6.5               | V    |
| 3   | 5.0V Flash Program/Erase Voltage  | $V_{PP}$                                     | -0.3                 | 6.5               | V    |
| 4   | 3.3V – 5.0V External I/O Supply Voltage <sup>3</sup>  | $V_{DDE1}^4$<br>$V_{DDE2}^4$<br>$V_{DDE3}^4$ | -0.3<br>-0.3<br>-0.3 | 6.5<br>6.5<br>6.5 | V    |
| 5   | DC Input Voltage <sup>5</sup>   | $V_{IN}$                                     | -1.0 <sup>6</sup>    | 6.5 <sup>7</sup>  | V    |
| 6   | $V_{REF}$ Differential Voltage  | $V_{RH} - V_{RL}$                            | -0.3                 | 5.5               | V    |
| 7   | $V_{RH}$ to $V_{DDA}$ Differential Voltage  | $V_{RH} - V_{DDA}$                           | -5.5                 | 5.5               | V    |
| 8   | $V_{RL}$ to $V_{SSA}$ Differential Voltage  | $V_{RL} - V_{SSA}$                           | -0.3                 | 0.3               | V    |
| 9   | $V_{DDR}$ to $V_{DDA}$ Differential Voltage   | $V_{DDR} - V_{DDA}$                          | - $V_{DDA}$          | 0.3               | V    |
| 10  | Maximum DC Digital Input Current <sup>8</sup> (per pin, applies to all digital MH, SH, and IH pins) | $I_{MAXD}$                                   | -2                   | 2                 | mA   |
| 11  | Maximum DC Analog Input Current <sup>9</sup> (per pin, applies to all analog AE and A pins)         | $I_{MAXA}$                                   | -3                   | 3                 | mA   |
| 12  | Storage Temperature Range   | $T_{STG}$                                    | -55.0                | 150.0             | °C   |
| 13  | Maximum Solder Temperature <sup>10</sup>  | $T_{SDR}$                                    | —                    | 260.0             | °C   |
| 14  | Moisture Sensitivity Level <sup>11</sup>  | MSL  | —                    | 3                 |      |

<sup>1</sup> Functional operating conditions are given in the DC electrical specifications. Absolute maximum ratings are stress ratings only, and functional operation at the maxima is not guaranteed. Stress beyond the listed maxima may affect device reliability or cause permanent damage to the device.

<sup>2</sup> Absolute maximum voltages are currently maximum burn-in voltages. Absolute maximum specifications for device stress have not yet been determined.

<sup>3</sup> All functional non-supply I/O pins are clamped to  $V_{SS}$  and  $V_{DDE}$ .

<sup>4</sup>  $V_{DDE1}$ ,  $V_{DDE2}$ , and  $V_{DDE3}$  are separate power segments and may be powered independently with no differential voltage constraints between the power segments.

<sup>5</sup> AC signal over and undershoot of the input voltages of up to +/- 2.0 volts is permitted for a cumulative duration of 60 hours over the complete lifetime of the device (injection current does not need to be limited for this duration).

<sup>6</sup> Internal structures will hold the input voltage above -1.0 volt if the injection current limit of 2mA is met.

<sup>7</sup> Internal structures hold the input voltage below this maximum voltage on all pads powered by  $V_{DDE}$  supplies, if the maximum injection current specification is met (2 mA for all pins) and  $V_{DDE}$  is within Operating Voltage specifications.

<sup>8</sup> Total injection current for all pins (including both digital and analog) must not exceed 25mA.

<sup>9</sup> Total injection current for all analog input pins must not exceed 15mA.

<sup>10</sup> Solder profile per CDF-AEC-Q100.

<sup>11</sup> Moisture sensitivity per JEDEC test method A112.

## 2.2 Thermal Characteristics

Table 4. Thermal Characteristics

| Num | Characteristic   | Symbol            | Unit | Value      |          |          |
|-----|--|-------------------|------|------------|----------|----------|
|     |  |                   |      | 208 MAPBGA | 176 LQFP | 144 LQFP |
| 1   | Junction to Ambient <sup>1, 2</sup><br>Natural Convection<br>(Single layer board)    | R <sub>θJA</sub>  | °C/W | 44         | 38       | 43       |
| 2   | Junction to Ambient <sup>1, 3</sup><br>Natural Convection<br>(Four layer board 2s2p) | R <sub>θJA</sub>  | °C/W | 27         | 31       | 34       |
| 3   | Junction to Ambient <sup>1, 3</sup><br>(@200 ft./min., Single layer board)           | R <sub>θJMA</sub> | °C/W | 35         | 30       | 34       |
| 4   | Junction to Ambient <sup>1, 3</sup><br>(@200 ft./min., Four layer board 2s2p)        | R <sub>θJMA</sub> | °C/W | 24         | 25       | 28       |
| 5   | Junction to Board <sup>4</sup>   | R <sub>θJB</sub>  | °C/W | 16         | 20       | 22       |
| 6   | Junction to Case <sup>5</sup>  | R <sub>θJC</sub>  | °C/W | 8          | 6        | 7        |
| 7   | Junction to Package Top <sup>6</sup><br>Natural Convection                           | Ψ <sub>JT</sub>   | °C/W | 2          | 2        | 2        |

<sup>1</sup> Junction temperature is a function of on-chip power dissipation, package thermal resistance, mounting site (board) temperature, ambient temperature, air flow, power dissipation of other components on the board, and board thermal resistance.

<sup>2</sup> Per SEMI G38-87 and JEDEC JESD51-2 with the single layer board horizontal.

<sup>3</sup> Per JEDEC JESD51-6 with the board horizontal.

<sup>4</sup> Thermal resistance between the die and the printed circuit board per JEDEC JESD51-8. Board temperature is measured on the top surface of the board near the package.

<sup>5</sup> Indicates the average thermal resistance between the die and the case top surface as measured by the cold plate method (MIL SPEC-883 Method 1012.1) with the cold plate temperature used for the case temperature.

<sup>6</sup> Thermal characterization parameter indicating the temperature difference between package top and the junction temperature per JEDEC JESD51-2.

### 2.2.1 General Notes for Specifications at Maximum Junction Temperature

An estimation of the chip junction temperature, T<sub>J</sub>, can be obtained from the equation:

$$T_J = T_A + (R_{\theta JA} \times P_D) \quad \text{Eqn. 1}$$

where:

$$T_A = \text{ambient temperature for the package (°C)} \quad \text{Eqn. 2}$$

$$R_{\theta JA} = \text{junction to ambient thermal resistance (°C/W)} \quad \text{Eqn. 3}$$

$$P_D = \text{power dissipation in the package (W)} \quad \text{Eqn. 4}$$

The supplied thermal resistances are provided based on JEDEC JESD51 series of standards to provide consistent values for estimations and comparisons. The difference between the values determined on the single-layer (1s) board and on the four-layer board with two signal layers and a power and a ground plane (2s2p) clearly demonstrate that the effective thermal resistance of

## Electrical Characteristics

the component is not a constant. It depends on the construction of the application board (number of planes), the effective size of the board which cools the component, how well the component is thermally and electrically connected to the planes, and the power being dissipated by adjacent components.

Connect all the ground and power balls to the respective planes with one via per ball. Using fewer vias to connect the package to the planes reduces the thermal performance. Thinner planes also reduce the thermal performance. When the clearance between through vias leave the planes virtually disconnected, the thermal performance is also greatly reduced.

As a general rule, the value obtained on a single layer board is appropriate for the tightly packed printed circuit board. The value obtained on the board with the internal planes is usually appropriate if the application board has one oz (35 micron nominal thickness) internal planes, the components are well separated, and the overall power dissipation on the board is less than 0.02 W/cm<sup>2</sup>.

The thermal performance of any component depends strongly on the power dissipation of surrounding components. In addition, the ambient temperature varies widely within the application. For many natural convection and especially closed box applications, the board temperature at the perimeter (edge) of the package is approximately the same as the local air temperature near the device. Specifying the local ambient conditions explicitly as the board temperature provides a more precise description of the local ambient conditions that determine the temperature of the device.

At a known board temperature, the junction temperature is estimated using the following equation:

$$T_J = T_B + (R_{\theta JB} \times P_D) \quad \text{Eqn. 5}$$

where:

$$T_J = \text{junction temperature (}^\circ\text{C)} \quad \text{Eqn. 6}$$

$$T_B = \text{board temperature at the package perimeter (}^\circ\text{C/W)} \quad \text{Eqn. 7}$$

$$R_{\theta JB} = \text{junction to board thermal resistance (}^\circ\text{C/W) per JESD51-8} \quad \text{Eqn. 8}$$

$$P_D = \text{power dissipation in the package (W)} \quad \text{Eqn. 9}$$

When the heat loss from the package case to the air can be ignored, acceptable predictions of junction temperature can be made. The application board should be similar to the thermal test condition, with the component soldered to a board with internal planes.

Historically, the thermal resistance has frequently been expressed as the sum of a junction to case thermal resistance and a case to ambient thermal resistance:

$$R_{\theta JA} = R_{\theta JC} + R_{\theta CA} \quad \text{Eqn. 10}$$

where:

$$R_{\theta JA} = \text{junction to ambient thermal resistance (}^\circ\text{C/W)} \quad \text{Eqn. 11}$$

$$R_{\theta JC} = \text{junction to case thermal resistance (}^\circ\text{C/W)} \quad \text{Eqn. 12}$$

$$R_{\theta CA} = \text{case to ambient thermal resistance (}^\circ\text{C/W)} \quad \text{Eqn. 13}$$

$R_{\theta JC}$  is device related and cannot be influenced by the user. The user controls the thermal environment to change the case to ambient thermal resistance,  $R_{\theta CA}$ . For instance, the user can change the air flow around the device, add a heat sink, change the mounting arrangement on printed circuit board, or change the thermal dissipation on the printed circuit board surrounding the

device. This description is most useful for packages with heat sinks where some 90% of the heat flow is through the case to the heat sink to ambient. For most packages, a better model is required.

A more accurate two-resistor thermal model can be constructed from the junction to board thermal resistance and the junction to case thermal resistance. The junction to case covers the situation where a heat sink will be used or where a substantial amount of heat is dissipated from the top of the package. The junction to board thermal resistance describes the thermal performance when most of the heat is conducted to the printed circuit board. This model can be used for either hand estimations or for a computational fluid dynamics (CFD) thermal model.

To determine the junction temperature of the device in the application after prototypes are available, the Thermal Characterization Parameter ( $\Psi_{JT}$ ) can be used to determine the junction temperature with a measurement of the temperature at the top center of the package case using the following equation:

$$T_J = T_T + (\Psi_{JT} \times P_D) \quad \text{Eqn. 14}$$

where:

$$T_T = \text{thermocouple temperature on top of the package (}^\circ\text{C)} \quad \text{Eqn. 15}$$

$$\Psi_{JT} = \text{thermal characterization parameter (}^\circ\text{C/W)} \quad \text{Eqn. 16}$$

$$P_D = \text{power dissipation in the package (W)} \quad \text{Eqn. 17}$$

The thermal characterization parameter is measured per JESD51-2 specification using a 40-gauge type T thermocouple epoxied to the top center of the package case. The thermocouple should be positioned so that the thermocouple junction rests on the package. A small amount of epoxy is placed over the thermocouple junction and over about 1 mm of wire extending from the junction. The thermocouple wire is placed flat against the package case to avoid measurement errors caused by cooling effects of the thermocouple wire.

## References:

Semiconductor Equipment and Materials International  
805 East Middlefield Rd  
Mountain View, CA 94043  
(415) 964-5111

MIL-SPEC and EIA/JESD (JEDEC) specifications are available from Global Engineering Documents at 800-854-7179 or 303-397-7956.

JEDEC specifications are available on the WEB at <http://www.jedec.org>.

1. C.E. Triplett and B. Joiner, "An Experimental Characterization of a 272 PBGA Within an Automotive Engine Controller Module," Proceedings of SemiTherm, San Diego, 1998, pp. 47–54.
2. G. Kromann, S. Shidore, and S. Addison, "Thermal Modeling of a PBGA for Air-Cooled Applications," Electronic Packaging and Production, pp. 53–58, March 1998.
3. B. Joiner and V. Adams, "Measurement and Simulation of Junction to Board Thermal Resistance and Its Application in Thermal Modeling," Proceedings of SemiTherm, San Diego, 1999, pp. 212–220.

## 2.3 ESD Characteristics

Table 5. ESD Ratings<sup>1, 2</sup>

| Characteristic                            | Symbol | Value             | Unit   |
|---|--------|-------------------|--------|
| ESD for Human Body Model (HBM)            |        | 2000              | V      |
| HBM Circuit Description                   | R1     | 1500              | Ohm    |
|   | C      | 100               | pF     |
| ESD for Field Induced Charge Model (FDCM) |        | 500 (all pins)    | V      |
|   |        | 750 (corner pins) |        |
| Number of Pulses per pin:                 |        |                   |        |
| Positive Pulses (HBM)                     | —      | 1                 | —      |
| Negative Pulses (HBM)                     | —      | 1                 | —      |
| Interval of Pulses                        | —      | 1                 | second |

<sup>1</sup> All ESD testing is in conformity with CDF-AEC-Q100 Stress Test Qualification for Automotive Grade Integrated Circuits.

<sup>2</sup> A device will be defined as a failure if after exposure to ESD pulses the device no longer meets the device specification requirements. Complete DC parametric and functional testing shall be performed per applicable device specification at room temperature followed by hot temperature, unless specified otherwise in the device specification

## 2.4 DC Electrical Specifications

Table 6. DC Electrical Specifications

| Num | Characteristic   | Symbol   | Min  | Max  | Unit     |
|-----|--|--|--|--|----------|
| 1a  | <b>C parts</b><br>Operating junction temperature range<br>Operating ambient temperature range <sup>1</sup>             | $T_J$<br>$T_A$                                   | -40<br>-40                                     | 105<br>85                                      | °C<br>°C |
| 1b  | <b>V parts</b><br>Operating junction temperature range<br>Operating ambient temperature range <sup>1</sup>             | $T_J$<br>$T_A$                                   | -40<br>-40                                     | 120<br>105                                     | °C<br>°C |
| 1c  | <b>M parts<sup>2</sup></b><br>Operating junction temperature range<br>Operating ambient temperature range <sup>1</sup> | $T_J$<br>$T_A$                                   | -40<br>-40                                     | 145<br>125                                     | °C<br>°C |
| 2   | 5.0V Voltage Regulator Reference Voltage   | $V_{DDR}$  | 4.5  | 5.25   | V        |
| 3   | 5.0V Analog Supply Voltage   | $V_{DDA}$  | 4.5  | 5.25   | V        |
| 4   | 5.0V Flash Program/Erase Voltage <sup>3</sup>  | $V_{PP}$   | 4.5  | 5.25   | V        |
| 5   | 3.3V – 5.0V External I/O Supply Voltage  | $V_{DDE1}^{4,5}$<br>$V_{DDE2}^4$<br>$V_{DDE3}^4$ | 3.0<br>3.0<br>3.0                              | 5.5<br>5.5<br>5.5                              | V        |
| 6   | Pad (SH/MH/IH) Input High Voltage  | $V_{IH}$   | $0.65 \times V_{DDE}$                          | $V_{DDE} + 0.3$                                | V        |
| 7   | Pad (SH/MH/IH) Input Low Voltage   | $V_{IL}$   | $V_{SS} - 0.3$                                 | $0.35 \times V_{DDE}$                          | V        |
| 8   | Pad (SH/MH/IH) Input Hysteresis  | $V_{HYS}$  | $0.1 \times V_{DDE}$                           | $0.2 \times V_{DDE}$                           | V        |
| 9   | Analog (AE/A) Input Voltage  | $V_{INDC}$                                       | $V_{SSA} - 0.3$                                | $V_{DDA} + 0.3$<br>see note <sup>5</sup>       | V        |
| 10  | Slow/Medium I/O Output High Voltage<br>$I_{OH} = -1.0$ mA<br>$I_{OH} = -0.2$ mA  | $V_{OH}$   | $0.80 \times V_{DDE}$<br>$0.95 \times V_{DDE}$ | —  | V        |
| 11  | Slow/Medium I/O Output Low Voltage<br>$I_{OL} = 1.0$ mA<br>$I_{OH} = 0.2$ mA   | $V_{OL}$   | —  | $0.20 \times V_{DDE}$<br>$0.05 \times V_{DDE}$ | V        |
| 12  | Input Capacitance (Digital Pins: Pad type MH,SH, IH with no A or AE)   | $C_{IN}$   | —  | 7  | pF       |
| 13  | Input Capacitance (Analog Pins: Pad type A, AE, and AE+IH)   | $C_{IN\_A}$                                      | —  | 10   | pF       |
| 14  | Input Capacitance (Shared digital and analog pins: A with SH or MH)  | $C_{IN\_M}$                                      | —  | 12   | pF       |
| 15  | Slow/Medium I/O Weak Pull Up/Down Absolute Current <sup>6</sup>  | $I_{ACT}$  | 10   | 170  | μA       |
| 16  | I/O Input Leakage Current <sup>7</sup>   | $I_{INACT\_D}$                                   | -1.5   | 1.5  | μA       |
| 17  | DC Injection Current (per pin)   | $I_{IC}$   | -2.0   | 2.0  | mA       |
| 18  | Analog Input Current, Channel Off <sup>8</sup> (Analog pins AE and AE+IH)  | $I_{INACT\_A}$                                   | -200   | 200  | nA       |
| 19  | Analog Input Current (Shared digital and analog pins: A with SH or MH)   | $I_{INACT\_AD}$                                  | -1.5   | 1.5  | μA       |
| 20  | $V_{RH}$ to $V_{DDA}$ Differential Voltage   | $V_{RH} - V_{DDA}$                               | -100   | 100  | mV       |



## Electrical Characteristics

**Table 6. DC Electrical Specifications (continued)**

| Num | Characteristic  | Symbol               | Min  | Max | Unit |
|-----|---|----------------------|------|-----|------|
| 21  | $V_{RL}$ to $V_{SSA}$ Differential Voltage  | $V_{RL} - V_{SSA}$   | -100 | 100 | mV   |
| 22  | $V_{SS}$ to $V_{SSA}$ Differential Voltage  | $V_{SS} - V_{SSA}$   | -100 | 100 | mV   |
| 23  | $V_{SSSYN}$ to $V_{SS}$ Differential Voltage                                      | $V_{SSSYN} - V_{SS}$ | -50  | 50  | mV   |
| 24  | $V_{DDR}$ to $V_{DDA}$ Differential Voltage                                       | $V_{DDR} - V_{DDA}$  | -100 | 100 | mV   |
| 25  | Slew rate on $V_{DDA}$ , $V_{DDR}$ , and $V_{DDE}$ power supply pins <sup>9</sup> | Vramp                | 1    | 100 | V/ms |
| 26  | Capacitive Supply Load  | Vload                |      |     | nF   |
|     | VDD   |                      | 800  | —   |      |
|     | VDD33   |                      | 200  | —   |      |
|     | VDDSYN  |                      | 200  |     |      |

<sup>1</sup> Please refer to [Section 2.2.1, “General Notes for Specifications at Maximum Junction Temperature”](#) for more details about the relation between ambient temperature  $T_A$  and device junction temperature  $T_J$ .

<sup>2</sup> M parts can't go above 66 MHz.

<sup>3</sup>  $V_{PP}$  can drop to 0 volts during read-only operations and before entry to Sleep mode, to reduce power consumption.

<sup>4</sup>  $V_{DDE1}$ ,  $V_{DDE2}$ , and  $V_{DDE3}$  are separate power segments and may be powered independently with no differential voltage constraints between the power segments.

<sup>5</sup> If  $V_{DDE1}$  is below  $V_{DDA}$  than the analog input limits (spec #9 (Analog (AE/A) Input Voltage) in [Table 6](#)) will be based on the  $V_{DDE1}$  voltage level.

<sup>6</sup> Absolute value of current, measured at  $V_{IL}$  and  $V_{IH}$ .

<sup>7</sup> Weak pull up/down inactive. Measured at  $V_{DDE} = 5.25$  V. Applies to pad types: SH and MH.

<sup>8</sup> Maximum leakage occurs at maximum operating temperature. Leakage current decreases by approximately one-half for each 8 to 12 °C, in the ambient temperature range of 50 to 125 °C. Applies to pad types: A and AE.

<sup>9</sup> This applies to the ramp up rate from 0.3 volts to 3.0 volts.

## 2.5 Operating Current Specifications

Table 7. Operating Currents

| Num       | Characteristic  | Symbol    | Typ <sup>1</sup><br>25C<br>Ambient                                | Typ <sup>1</sup><br>70C<br>Ambient                              | Max <sup>1</sup><br>-40–145C<br>Junction                           | Unit   |
|-----------|---|-----------|---|---|--|--|
| Equations | $I_{TOTAL} = I_{DDE} + I_{PP} + I_{DDA} + I_{DDR}$<br>$I_{DDE} = I_{DDE1} + I_{DDE2} + I_{DDE3}$  |           |   |   |  |  |
| 1         | $V_{DDE(1,2,3)}$ Current<br>$V_{DDE(1,2,3)}$ @ 3.0V - 5.5V<br>Static <sup>2</sup> , or when in SLEEP or STOP<br>Dynamic <sup>3</sup>  | $I_{DDE}$ | 1<br>Note <sup>3</sup>  | 3<br>Note <sup>3</sup>  | 30<br>Note <sup>3</sup>  | $\mu$ A<br>mA  |
| 2         | $V_{PP}$ Current<br>$V_{PP}$ @ 0V (All modes)<br>$V_{PP}$ @ 5.25V<br>SLEEP mode<br>STOP mode<br>RUN mode  | $I_{PP}$  | 1<br><br>15<br>15<br>1  | 1<br><br>20<br>20<br>1  | 1<br><br>30<br>30<br>25  | $\mu$ A<br>$\mu$ A<br>$\mu$ A<br>mA  |
| 3         | $V_{DDA}$ Current<br>$V_{DDA}$ @ 4.5V - 5.25V<br>RUN mode <sup>4</sup><br>SLEEP/STOP <sup>5</sup> mode with 32KIRC<br>SLEEP/STOP <sup>5</sup> mode with 32KOSC<br>SLEEP/STOP <sup>5</sup> mode with 16MIRC  | $I_{DDA}$ | <br>5<br>12<br>12<br>111  | <br>5<br>16<br>16<br>165  | <br>10<br>26<br>28<br>225  | <br>mA<br>$\mu$ A<br>$\mu$ A<br>$\mu$ A  |
| 4         | $V_{DDR}$ Current<br>$V_{DDR}$ @ 4.5V - 5.25V<br>SLEEP mode<br>with XOSC <sup>6</sup> (additional)<br>with RTC/API (additional)<br>each 8K RAM block (additional)<br>STOP mode<br>with XOSC <sup>6</sup> (additional)<br>RUN mode (Using 16 MHz IRC)<br>RUN mode (Maximum @ 48 MHz) <sup>7</sup><br>RUN mode (Maximum @ 66 MHz) <sup>8</sup><br>RUN mode (Maximum @ 80MHz) <sup>9</sup> | $I_{DDR}$ | <br>20<br>500<br>1<br>0.8<br>170<br>500<br>30<br>50<br>105<br>120 | <br>25<br>600<br>1<br>7<br>600<br>600<br>35<br>75<br>110<br>130 | <br>360<br>900<br>3<br>45<br>1500<br>900<br>40<br>90<br>120<br>135 | <br>$\mu$ A<br>$\mu$ A<br>$\mu$ A<br>$\mu$ A<br>$\mu$ A<br>$\mu$ A<br>mA<br>mA<br>mA<br>mA |

<sup>1</sup> Typ - Nominal voltage levels and functional activity. Max - Maximum voltage levels and functional activity.

<sup>2</sup> Static state of pins is when input pins are disabled or not being toggled and driven to a valid input level, output pins are not toggling or driving against any current loads, and internal pull devices are disabled or not pulling against any current loads.

<sup>3</sup> Dynamic current from pins is application specific and depends on active pull devices, switching outputs, output capacitive and current loads, and switching inputs. Refer to [Table 8](#) for more information.

<sup>4</sup> RUN mode is a typical application with the ADC, 16MIRC, 32KIRC running.

<sup>5</sup> SLEEP/STOP mode means that only the listed peripherals are on. All others are disabled.

<sup>6</sup> XOSC: optionally enabled in SLEEP and STOP modes (oscillator remains running from crystal but XOSC clock output disabled).

<sup>7</sup> RUN mode condition includes PLL selected as source of system clock, XOSC enabled with 40MHz crystal, all peripherals enabled, both cores running, and running a typical application using both SRAM and flash.

## Electrical Characteristics

- <sup>8</sup> RUN mode condition includes PLL selected as source of system clock, XOSC enabled with 40MHz crystal; all peripheral and cores enabled and running a typical application using both SRAM and flash. Be sure to calculate the junction temperature, as the maximum current at maximum ambient temperature can exceed the maximum junction temperature.
- <sup>9</sup> RUN mode condition includes PLL selected as source of system clock, XOSC enabled with 40MHz crystal, all peripheral and cores enabled and running a typical application using both SRAM and flash. Only for 208 MAPBGA and only 120C junction or lower. Be sure to calculate the junction temperature, as the maximum current at maximum ambient temperature can exceed the maximum junction temperature

## 2.6 I/O Pad Current Specifications

The power consumption of an I/O segment depends on the usage of the pins on a particular segment. The power consumption is the sum of all output pin currents for a particular segment. The output pin current can be calculated from [Table 8](#) based on the voltage, frequency, and load on the pin. Use linear scaling to calculate pin currents for voltage, frequency, and load parameters that fall outside the values given in [Table 8](#).

**Table 8. I/O Pad Average DC Current<sup>1</sup>**

| Num | Pad Type                | Symbol              | Frequency (MHz) | Load <sup>2</sup> (pF) | Voltage (V) | Slew Rate Control | Current (mA) |
|-----|-------------------------|---------------------|-----------------|------------------------|-------------|-------------------|--------------|
| 1   | Slow<br>(Pad Type SH)   | I <sub>DRV_SH</sub> | 25              | 50                     | 5.25        | 11                | 8.0          |
| 2   |                         |                     | 10              | 50                     | 5.25        | 01                | 3.2          |
| 3   |                         |                     | 2               | 50                     | 5.25        | 00                | 0.7          |
| 4   |                         |                     | 2               | 200                    | 5.25        | 00                | 2.4          |
| 5   | Medium<br>(Pad Type MH) | I <sub>DRV_MH</sub> | 50              | 50                     | 5.25        | 11                | 17.3         |
| 6   |                         |                     | 20              | 50                     | 5.25        | 01                | 6.5          |
| 7   |                         |                     | 3.33            | 50                     | 5.25        | 00                | 1.1          |
| 8   |                         |                     | 3.33            | 200                    | 5.25        | 00                | 3.9          |

<sup>1</sup> These values are estimated from simulation and are not tested. Currents apply to output pins only.

<sup>2</sup> All loads are lumped.

## 2.7 Low Voltage Characteristics

Table 9. Low Voltage Monitors

| Num | Characteristic  | Symbol                                     | Min          | Typical      | Max          | Unit |
|-----|---|--|--------------|--------------|--------------|------|
| 1   | Power-on-Reset Assert Level <sup>1</sup>  | V <sub>POR</sub>                           | —            | 0.70         | —            | V    |
| 2   | Low Voltage Monitor 1.5V <sup>1</sup><br>Assert Level<br>De-assert Level                | V <sub>LV15A</sub><br>V <sub>LV15D</sub>   | —<br>—       | 1.40<br>1.45 | —<br>—       | V    |
| 3   | Low Voltage Monitor 3.3V <sup>2</sup><br>Assert Level<br>De-assert Level                | V <sub>LV33A</sub><br>V <sub>LV33D</sub>   | —<br>—       | 3.05<br>3.10 | —<br>—       | V    |
| 4   | Low Voltage Monitor Synthesizer <sup>3</sup><br>Assert Level<br>De-assert Level         | V <sub>LVSYNA</sub><br>V <sub>LVSYND</sub> | —<br>—       | 3.05<br>3.10 | —<br>—       | V    |
| 5   | Low Voltage Monitor 5.0V Low Threshold <sup>4</sup><br>Assert Level<br>De-assert Level  | V <sub>LV5LA</sub><br>V <sub>LV5LD</sub>   | 3.30<br>3.35 | 3.35<br>3.40 | 3.40<br>3.45 | V    |
| 6   | Low Voltage Monitor 5.0V <sup>4</sup><br>Assert Level<br>De-assert Level                | V <sub>LV5A</sub><br>V <sub>LV5D</sub>     | 4.50<br>4.55 | 4.55<br>4.60 | 4.70<br>4.75 | V    |
| 7   | Low Voltage Monitor 5.0V High Threshold <sup>4</sup><br>Assert Level<br>De-assert Level | V <sub>LV5HA</sub><br>V <sub>LV5HD</sub>   | 4.70<br>4.75 | 4.75<br>4.80 | 4.80<br>4.85 | V    |

<sup>1</sup> Monitors V<sub>DD</sub>

<sup>2</sup> Monitors V<sub>DD33</sub>

<sup>3</sup> Monitors V<sub>DDSYN</sub>

<sup>4</sup> Monitors V<sub>DDA</sub>

## 2.8 Oscillators Electrical Characteristics

**Table 10. 3.3V High Frequency External Oscillator<sup>1</sup>**

| Num | Characteristic  | Symbol         | Min. Value                                  | Max. Value  | Unit |
|-----|---|----------------|---|---|------|
| 1   | Frequency Range <sup>2</sup>  | $f_{ref}$      | 4 <sup>3</sup>                              | 40  | MHz  |
| 2   | Duty Cycle of reference   | $t_{dc}$       | 40  | 60  | %    |
| 3   | EXTAL Input High Voltage<br>External crystal mode <sup>4</sup><br>External clock mode | $V_{IHEXT}$    | $V_{XTAL} + 0.4$<br>$0.65 \times V_{DDSYN}$ | $V_{DDSYN} + 0.3$<br>$V_{DDSYN} + 0.3$                      | V    |
| 4   | EXTAL Input Low Voltage<br>External crystal mode <sup>4</sup><br>External clock mode  | $V_{ILEXT}$    | $V_{DDSYN} - 0.3$<br>$V_{DDSYN} - 0.3$      | $V_{XTAL} - 0.4$<br>$0.35 \times V_{DDSYN}$                 | V    |
| 5   | XTAL Current <sup>5</sup>   | $I_{XTAL}$     | 2   | 6   | mA   |
| 6   | Total On-chip stray capacitance on XTAL   | $C_{S\_XTAL}$  | —   | 3   | pF   |
| 7   | Total On-chip stray capacitance on EXTAL  | $C_{S\_EXTAL}$ | —   | 3   | pF   |
| 8   | Crystal manufacturer's recommended capacitive load                                    | $C_L$          | See crystal specification                   | See crystal specification                                   | pF   |
| 9   | Discrete load capacitance to be connected to EXTAL                                    | $C_{L\_EXTAL}$ | —   | $2 \times C_L - C_{S\_EXTAL} - C_{PCB\_EXTAL}$ <sup>6</sup> | pF   |
| 10  | Discrete load capacitance to be connected to XTAL                                     | $C_{L\_XTAL}$  | —   | $2 \times C_L - C_{S\_XTAL} - C_{PCB\_XTAL}$ <sup>5</sup>   | pF   |
| 11  | Startup Time  | $t_{startup}$  | —   | 10  | ms   |

<sup>1</sup> Oscillator circuit performance is highly dependent on application requirements and board layout. Therefore, NXP strongly recommends selecting appropriate values for oscillator circuit components based on a board characterization performed by the crystal manufacturer. Application note AN12442, provides an example method for analyzing oscillator circuit functionality.

<sup>2</sup> Since this is an amplitude controlled oscillator the use of overtone oscillators is not recommended. Only use fundamental frequency oscillators.

<sup>3</sup> When PLL frequency modulation is active, reference frequencies less than 8MHz will distort the modulated waveform and the effects of this on emissions is not characterized.

<sup>4</sup> This parameter is meant for those who do not use quartz crystals or resonators, but CAN osc, in crystal mode. In that case,  $V_{extal} - V_{xtal} \geq 400\text{mV}$  criteria has to be met for oscillator's comparator to produce output clock.

<sup>5</sup>  $I_{xtal}$  is the oscillator bias current out of the XTAL pin with both EXTAL and XTAL pins grounded.

<sup>6</sup>  $C_{PCB\_EXTAL}$  and  $C_{PCB\_XTAL}$  are the measured PCB stray capacitances on EXTAL and XTAL, respectively

**Table 11. 5V Low Frequency (32 kHz) External Oscillator<sup>1</sup>**

| Num | Characteristic                                     | Symbol        | Min. Value                | Max. Value                | Unit          |
|-----|--|---------------|---------------------------|---------------------------|---------------|
| 1   | Frequency Range                                    | $f_{ref32}$   | 32                        | 38                        | kHz           |
| 2   | Duty Cycle of reference                            | $t_{dc32}$    | 40                        | 60                        | %             |
| 3   | XTAL32 Current <sup>2</sup>                        | $I_{XTAL32}$  | 0.5                       | 3                         | $\mu\text{A}$ |
| 4   | Crystal manufacturer's recommended capacitive load | $C_{L32}$     | See crystal specification | See crystal specification | pF            |
| 5   | Startup Time                                       | $t_{startup}$ | —                         | 2                         | s             |

## Electrical Characteristics

- <sup>1</sup> Oscillator circuit performance is highly dependent on application requirements and board layout. Therefore, NXP strongly recommends selecting appropriate values for oscillator circuit components based on board characterization performed by the crystal manufacturer. Application note AN12442, provides an example method for analyzing oscillator circuit functionality.
- <sup>2</sup>  $I_{\text{xtal32}}$  is the oscillator bias current out of the XTAL32 pin with both EXTAL32 and XTAL32 pins grounded.

**Table 12. 5V High Frequency (16 MHz) Internal RC Oscillator**

| Num | Characteristic                                    | Symbol          | Min  | Typ | Max   | Unit |
|-----|---|-----------------|------|-----|-------|------|
| 1   | Frequency before trim <sup>1</sup>                | $F_{\text{ut}}$ | 12.8 | 16  | 22.3  | MHz  |
| 2   | Frequency after loading factory trim <sup>2</sup> | $F_{\text{t}}$  | 15.1 | 16  | 16.9  | MHz  |
| 3   | Application trim resolution <sup>3</sup>          | $T_{\text{s}}$  | —    | —   | ± 0.5 | %    |
| 4   | Application frequency trim step <sup>3</sup>      | $F_{\text{s}}$  | —    | 300 | —     | kHz  |
| 5   | Start up time                                     | $S_{\text{t}}$  | —    | —   | 500   | ns   |

<sup>1</sup> Across process, voltage, and temperature

<sup>2</sup> Across voltage and temperature

<sup>3</sup> Fixed voltage and temperature

**Table 13. 5V Low Frequency (32 kHz) Internal RC Oscillator**

| Num | Characteristic                                    | Symbol            | Min  | Typ  | Max  | Unit |
|-----|---|-------------------|------|------|------|------|
| 1   | Frequency before trim <sup>1</sup>                | $F_{\text{ut32}}$ | 20.8 | 32.0 | 43.2 | kHz  |
| 2   | Frequency after loading factory trim <sup>2</sup> | $F_{\text{t32}}$  | 26   | 32.0 | 38   | kHz  |
| 3   | Application trim resolution <sup>3</sup>          | $T_{\text{s32}}$  | —    | —    | ± 2  | %    |
| 4   | Application frequency trim step <sup>3</sup>      | $F_{\text{s32}}$  | —    | 1    | —    | kHz  |
| 5   | Start up time                                     | $S_{\text{t32}}$  | —    | —    | 100  | μs   |

<sup>1</sup> Across process, voltage, and temperature

<sup>2</sup> Across voltage and temperature

<sup>3</sup> Fixed voltage and temperature

## 2.9 FMPLL Electrical Characteristics

Table 14. FMPLL Electrical Specifications <sup>1</sup>

| Num | Characteristic  | Symbol              | Min. Value | Max. Value                  | Unit                  |
|-----|---|---------------------|------------|-----------------------------|-----------------------|
| 1   | System frequency <sup>2</sup><br>-40 °C ≤ T <sub>J</sub> ≤ 120 °C<br>-40 °C ≤ T <sub>J</sub> ≤ 145 °C | f <sub>sys</sub>    | 375<br>375 | 80000 <sup>3</sup><br>66000 | kHz                   |
| 2   | PLL Reference Frequency (output of predivider)  | f <sub>pllref</sub> | 4          | 10                          | MHz                   |
| 3   | VCO Frequency <sup>4</sup>  | f <sub>vco</sub>    | 192        | 500                         | MHz                   |
| 4   | PLL Frequency <sup>5</sup><br>-40 °C ≤ T <sub>J</sub> ≤ 120 °C<br>-40 °C ≤ T <sub>J</sub> ≤ 145 °C    | f <sub>pll</sub>    | 3<br>3     | 80 <sup>3</sup><br>66       | MHz                   |
| 5   | Loss of Reference Frequency <sup>6</sup>  | f <sub>LOR</sub>    | 100        | 1000                        | kHz                   |
| 6   | Self Clocked Mode Frequency <sup>7</sup>  | f <sub>SCM</sub>    | 13         | 35                          | MHz                   |
| 7   | PLL Lock Time <sup>8</sup>  | t <sub>pll</sub>    | —          | 750                         | μs                    |
| 8   | Frequency un-LOCK Range   | f <sub>UL</sub>     | - 4.0      | 4.0                         | % f <sub>sys</sub>    |
| 9   | Frequency LOCK Range  | f <sub>LCK</sub>    | - 2.0      | 2.0                         | % f <sub>sys</sub>    |
| 10  | CLKOUT Cycle-to-cycle Jitter, <sup>9, 10</sup>  | C <sub>jitter</sub> | - 5        | 5                           | % f <sub>clkout</sub> |
| 10a | CLKOUT Jitter at 10 μs period <sup>9,10, 11</sup>   | C <sub>jitter</sub> | - 0.05     | 0.05                        | % f <sub>clkout</sub> |
| 11  | Frequency Modulation Depth 1% Setting <sup>12,13</sup><br>(f <sub>sys</sub> Max must not be exceeded) | C <sub>mod</sub>    | 0.5        | 2                           | %f <sub>sys</sub>     |
| 12  | Frequency Modulation Depth 2% Setting <sup>12,13</sup><br>(f <sub>sys</sub> Max must not be exceeded) | C <sub>mod</sub>    | 1          | 3                           | %f <sub>sys</sub>     |

<sup>1</sup> V<sub>DDSYN</sub> = 3.0V to 3.6 V, V<sub>SSSYN</sub> = 0 V, TA = TL to TH

<sup>2</sup> The maximum value is without frequency modulation turned on. If frequency modulation is turned on, the maximum value (average frequency) must be de-rated by the percentage of modulation enabled.

<sup>3</sup> 80 MHz is only available in the 208 pin package.

<sup>4</sup> Optimum performance is achieved with the highest VCO frequency feasible based on the highest ERFD that results in the desired PLL frequency.

<sup>5</sup> The VCO frequency range is higher than the maximum allowable PLL frequency. The synthesizer control register 2's enhanced reduced frequency divider (FMPLL\_SYNCR2[ERFD]) in enhanced operation mode must be programmed to divide the VCO frequency within the PLL frequency range.

<sup>6</sup> Loss of reference frequency is the reference frequency detected by the PLL which then transitions into self clocked mode.

<sup>7</sup> Self clocked mode frequency is the frequency that the PLL operates at when the reference frequency falls below f<sub>LOR</sub>.

<sup>8</sup> This specification applies to the period required for the PLL to relock after changing the enhanced multiplication factor divider (EMFD) bits in the synthesizer control register 1 (SYNCR1) in enhanced operation mode.

<sup>9</sup> Jitter is the average deviation from the programmed frequency measured over the specified interval at maximum f<sub>sys</sub>. Measurements are made with the device powered by filtered supplies and clocked by a stable external clock signal. Noise injected into the PLL circuitry via V<sub>DDSYN</sub> and V<sub>SSSYN</sub> and variation in crystal oscillator frequency increase the jitter percentage for a given interval. CLKOUT divider set to divide-by-2.

<sup>10</sup> Values are with frequency modulation disabled. If frequency modulation is enabled, jitter is the sum of C<sub>jitter</sub> + C<sub>mod</sub>.

<sup>11</sup> The PLL % jitter reduces with more cycles. 10 μs was picked for a reference point for LIN (100 Kbits), slower speeds will have even less % jitter.

<sup>12</sup> Modulation depth selected must not result in f<sub>sys</sub> value greater than the f<sub>sys</sub> maximum specified value.

<sup>13</sup> These depth ranges are obtained by filtering the raw cycle-to-cycle clock frequency data to eliminate the presence of the normal clock jitter riding on top of the FM waveform. The allowable modulation rates are 400 kHz to 1 MHz.



## 2.10 eQADC Electrical Characteristics

Table 15. eQADC Conversion Specifications (Operating)

| Num | Characteristic  | Symbol             | Min          | Max             | Unit         |
|-----|---|--------------------|--------------|-----------------|--------------|
| 1   | ADC Clock (ADCLK) Frequency <sup>1</sup>  | F <sub>ADCLK</sub> | 1            | 12              | MHz          |
| 2   | Conversion Cycles   | CC                 | 14+2 (or 16) | 14+128 (or 142) | ADCLK cycles |
| 3   | Stop Mode Recovery Time <sup>2</sup>  | T <sub>SR</sub>    | 20           | —               | μs           |
| 4   | Resolution  | —                  | 1.25         | —               | mV           |
| 5   | INL: 12 MHz ADC Clock <sup>3</sup>  | INL12              | —            | 10              | Counts       |
| 6   | DNL: 12 MHz ADC Clock <sup>3</sup>  | DNL12              | —            | 10              | Counts       |
| 7   | Offset Error with Calibration <sup>3</sup>  | OFFWC              | —            | 10              | Counts       |
| 8   | Full Scale Gain Error with Calibration  | GAINWC             | —            | 10              | Counts       |
| 9   | Disruptive Input Injection Current <sup>4, 5, 6, 7</sup>  | I <sub>INJ</sub>   | —            | ±1              | mA           |
| 10  | Incremental Error due to injection current. All channels have same 10kΩ < R <sub>s</sub> < 100kΩ <sup>8</sup><br>Channel under test has R <sub>s</sub> =10kΩ,<br>I <sub>INJ</sub> =I <sub>INJMAX</sub> ·I <sub>INJMIN</sub> | E <sub>INJ</sub>   | —            | ±6              | Counts       |
| 11  | Total Unadjusted Error for single ended conversions with calibration <sup>3, 9, 10, 11, 12</sup>  | TUE                | —            | ±10             | Counts       |
| 12  | Source Impedance <sup>13</sup>  | R <sub>S</sub>     | —            | 100k            | Ohm          |

<sup>1</sup> Conversion characteristics vary with F<sub>ADCLK</sub> rate. Reduced conversion accuracy occurs at maximum F<sub>ADCLK</sub> rate. The maximum value is based on 800KS/s and the minimum value is based on 20MHz oscillator clock frequency divided by a maximum 16 factor.

<sup>2</sup> The specified value is for the case when the 100nF capacitor is not connected to the REFBYPC pin. When the capacitor is connected to the REFBPYC pin, the recovery time is 10ms.

<sup>3</sup> At V<sub>RH</sub> – V<sub>RL</sub> = 5.12 V, one lsb = 1.25 mV = one count.

<sup>4</sup> Below disruptive current conditions, the channel being stressed has conversion values of 0x3FF for analog inputs greater than V<sub>RH</sub> and 0x000 for values less than V<sub>RL</sub>. This assumes that V<sub>RH</sub> ≤ V<sub>DDA</sub> and V<sub>RL</sub> ≥ V<sub>SSA</sub> due to the presence of the sample amplifier. Other channels are not affected by non-disruptive conditions.

<sup>5</sup> Exceeding limit may cause conversion error on stressed channels and on unstressed channels. Transitions within the limit do not affect device reliability or cause permanent damage.

<sup>6</sup> Input must be current limited to the value specified. To determine the value of the required current-limiting resistor, calculate resistance values using V<sub>POSCLAMP</sub> = V<sub>DDA</sub> + 0.5V and V<sub>NEGCLAMP</sub> = – 0.3 V, then use the larger of the calculated values.

<sup>7</sup> Condition applies to two adjacent pads on the internal pad.

<sup>8</sup> At V<sub>RH</sub> – V<sub>RL</sub> = 5.12 V, one lsb = 1.25 mV = one count. This count error is in addition to the TUE count error.

<sup>9</sup> The TUE specification will always be better than the sum of the INL, DNL, offset, and gain errors due to canceling errors.

<sup>10</sup> TUE includes all internal device error such as internal reference variation (75% Ref, 25% Ref)

<sup>11</sup> Depending on the customer input impedance, the Analog Input Leakage current (DC Electrical specification) may affect the actual TUE measured on analog channels shared digital pins.

<sup>12</sup> It is possible to see up to one additional count added for the 144 pin packages since the VRL and VRH functions are shared with the VSSA and VDDA, respectively. On Analog pins above PA15, the accuracy effects from adjacent digital port pin activity is application dependent because of frequency, level, noise, etc.

<sup>13</sup> If R<sub>S</sub> is greater than 1 k Ohm, be sure to calculate the affect of pin leakage and use the proper sampling time, to ensure that you get the accuracy required.

## 2.11 Flash Memory Electrical Characteristics

Table 16. Flash Program and Erase Specifications<sup>1</sup>

| Num | Characteristic  | Symbol            | Min | Typ | Initial Max <sup>2</sup> | Max <sup>3</sup> | Unit               |
|-----|---|-------------------|-----|-----|--------------------------|------------------|--------------------|
| 1   | Double Word (64 bits) Program Time <sup>4</sup>   | $T_{dwprogram}$   | —   | 10  | —                        | 500              | $\mu$ s            |
| 2   | Page (128 bits) Program Time <sup>4</sup>   | $T_{pprogram}$    | —   | 15  | 44                       | 500              | $\mu$ s            |
| 3   | 16 Kbyte Block Pre-program and Erase Time   | $T_{16kpperase}$  | —   | 325 | 525                      | 5000             | ms                 |
| 4   | 64 Kbyte Block Pre-program and Erase Time   | $T_{64kpperase}$  | —   | 525 | 675                      | 5000             | ms                 |
| 5   | 128 Kbyte Block Pre-program and Erase Time  | $T_{128kpperase}$ | —   | 675 | 1800                     | 7500             | ms                 |
| 6   | Minimum operating frequency for program and erase operations  | —                 | 25  | —   | —                        | —                | MHz                |
| 7   | Wait States Relative to System Frequency<br>PFCRPn[RWSC] = 0b000; PFCRPn[WWSC] = 0b01<br>PFCRPn[RWSC] = 0b001; PFCRPn[WWSC] = 0b01<br>PFCRPn[RWSC] = 0b010; PFCRPn[WWSC] = 0b01 | $T_{rWSC}$        | —   | —   | —                        | 25<br>50<br>80   | MHz                |
| 8   | Recovery Time<br>Stop mode exit or STOP bit negated<br>Sleep mode exit (with CRP_RECPTTR[FASTREC]=1) <sup>5</sup>   | $T_{recover}$     | —   | —   | —                        | 20<br>120        | $\mu$ s<br>$\mu$ s |

<sup>1</sup> Typical program and erase times assume nominal supply values and operation at 25 °C.

<sup>2</sup> Initial factory condition: < 100 program/erase cycles, nominal supply values and operation at 25 °C.

<sup>3</sup> The maximum time is at worst case conditions after the specified number of program/erase cycles. This maximum value is characterized but not guaranteed.

<sup>4</sup> This does not include software overhead.

<sup>5</sup> If CRP\_RECPTTR[FASTREC]=0, then hardware will wait 2340 system clocks before exiting from Sleep mode to account for the flash recovery time. The default system clock source after Sleep is the 16MIRC. A nominal frequency of 16MHz equates to a hardware wait of 146 $\mu$ s.

Table 17. Flash EEPROM Module Life (Full Temperature Range)

| Num | Characteristic  | Symbol    | Min             | Typical <sup>1</sup> | Unit   |
|-----|---|-----------|-----------------|----------------------|--------|
| 1   | Number of Program/Erase cycles per block over the operating temperature range ( $T_J$ )<br>16 Kbyte and 64 Kbyte blocks<br>128 Kbyte blocks | P/E       | 100,000<br>1000 | —<br>100,000         | cycles |
| 2   | Data retention<br>Blocks with 0 – 1,000 P/E cycles<br>Blocks with 1,001 – 100,000 P/E cycles  | Retention | 20<br>5         | —                    | years  |

<sup>1</sup> Typical endurance is evaluated at 25C. Product qualification is performed to the minimum specification. For additional information on the NXP definition of Typical Endurance, please refer to Engineering Bulletin EB619 “Typical Endurance for Nonvolatile Memory.”

## 2.12 Pad AC Specifications

Table 18. Pad AC Specifications (VDDE = 3.0V - 5.5V)<sup>1</sup>

| Num | Pad Type                | SRC | Out Delay <sup>2, 3</sup><br>(ns) | Rise/Fall <sup>3, 4</sup><br>(ns) | Load Drive<br>(pF) |
|-----|-------------------------|-----|-----------------------------------|-----------------------------------|--------------------|
| 1   | Slow (SH)               | 11  | 39                                | 23                                | 50                 |
|     |                         |     | 120                               | 87                                | 200                |
|     |                         | 01  | 101                               | 52                                | 50                 |
|     |                         |     | 188                               | 111                               | 200                |
|     |                         | 00  | 507                               | 248                               | 50                 |
| 597 | 312                     | 200 |                                   |                                   |                    |
| 2   | Medium (MH)             | 11  | 23                                | 12                                | 50                 |
|     |                         |     | 64                                | 44                                | 200                |
|     |                         | 01  | 50                                | 22                                | 50                 |
|     |                         |     | 90                                | 50                                | 200                |
|     |                         | 00  | 261                               | 123                               | 50                 |
| 305 | 156                     | 200 |                                   |                                   |                    |
| 4   | Pull Up/Down (3.6V max) | —   | —                                 | 7500                              | 50                 |
| 5   | Pull Up/Down (5.5V max) | —   | —                                 | 9500                              | 50                 |

<sup>1</sup> These are worst case values that are estimated from simulation and not tested. The values in the table are simulated at VDDE = 3.0V to 5.5V, T<sub>A</sub> = TL to TH.

<sup>2</sup> This parameter is supplied for reference and is not tested. Add a maximum of one system clock to the output delay for delay with respect to system clock.

<sup>3</sup> Delay and rise/fall are measured to 20% or 80% of the respective signal.

<sup>4</sup> This parameter is guaranteed by characterization before qualification rather than 100% tested.

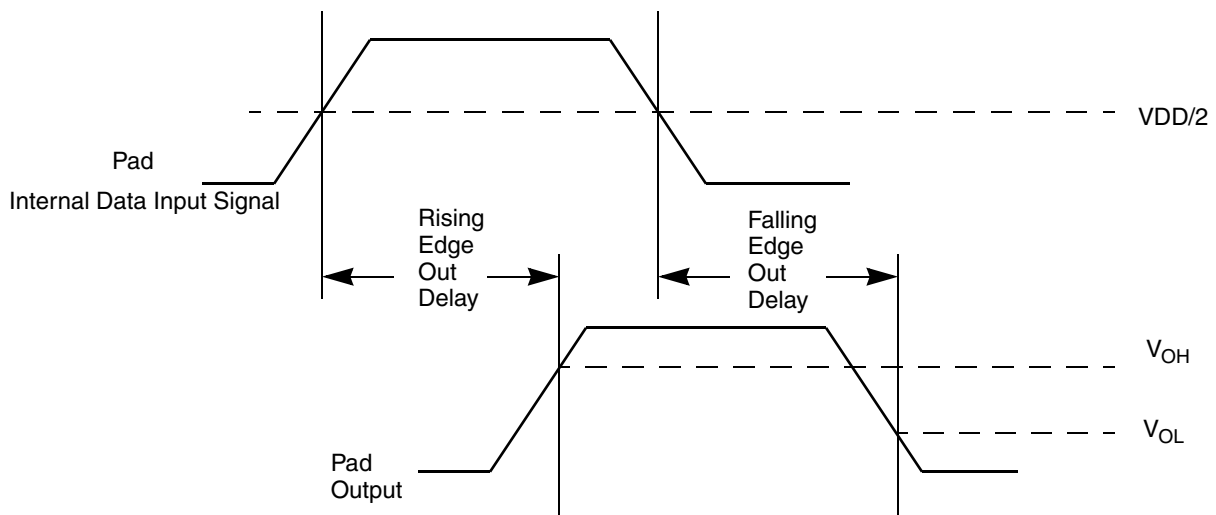


Figure 5. Pad Output Delay

## 2.13 AC Timing

### 2.13.1 Reset and Boot Configuration Pins

Table 19. Reset and Boot Configuration Timing

| Num | Characteristic   | Symbol            | Min | Max | Unit          |
|-----|--|-------------------|-----|-----|---------------|
| 1   | $\overline{\text{RESET}}$ Pulse Width                    | $t_{\text{RPW}}$  | 150 | —   | ns            |
| 2   | BOOTCFG Setup Time after $\overline{\text{RESET}}$ Valid | $t_{\text{RCSU}}$ | —   | 100 | $\mu\text{s}$ |
| 3   | BOOTCFG Hold Time from $\overline{\text{RESET}}$ Valid   | $t_{\text{RCH}}$  | 0   | —   | $\mu\text{s}$ |

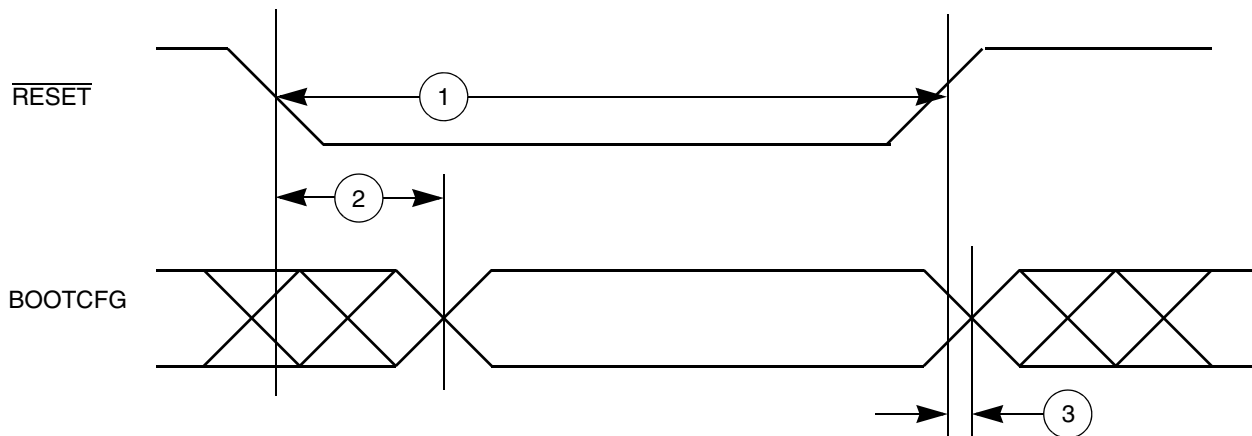


Figure 6. Reset and Boot Configuration Timing

### 2.13.2 External Interrupt (IRQ) and Non-Maskable Interrupt (NMI) Pins

Table 20. IRQ/NMI Timing

| Num | Characteristic                         | Symbol            | Min | Max | Unit             |
|-----|--|-------------------|-----|-----|------------------|
| 1   | IRQ/NMI Pulse Width Low                | $t_{\text{IPWL}}$ | 3   | —   | $t_{\text{SYS}}$ |
| 2   | IRQ/NMI Pulse Width High               | $T_{\text{IPWH}}$ | 3   | —   | $t_{\text{SYS}}$ |
| 3   | IRQ/NMI Edge to Edge Time <sup>1</sup> | $t_{\text{ICYC}}$ | 6   | —   | $t_{\text{SYS}}$ |

<sup>1</sup> Applies when IRQ/NMI pins are configured for rising edge or falling edge events, but not both.

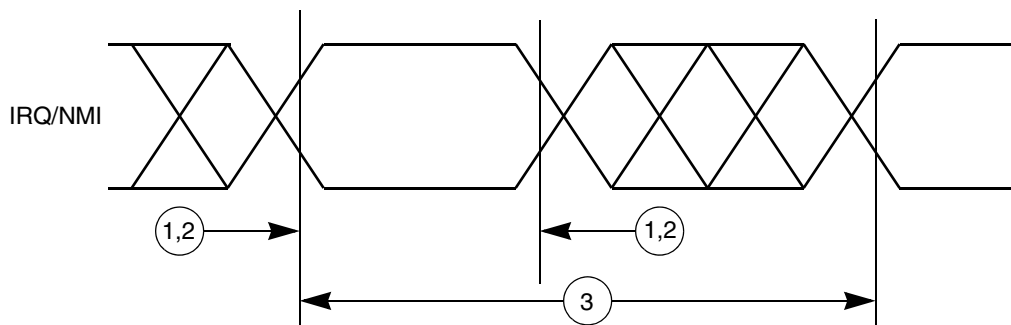


Figure 7. IRQ and NMI Timing

### 2.13.3 JTAG (IEEE 1149.1) Interface

Table 21. JTAG Interface Timing<sup>1</sup>

| Num | Characteristic   | Symbol               | Min | Max | Unit |
|-----|--|----------------------|-----|-----|------|
| 1   | TCK Cycle Time   | $t_{JCYC}$           | 100 | —   | ns   |
| 2   | TCK Clock Pulse Width (Measured at $V_{DDE}/2$ )       | $t_{JDC}$            | 40  | 60  | ns   |
| 3   | TCK Rise and Fall Times (40% – 70%)                    | $t_{TCKRISE}$        | —   | 3   | ns   |
| 4   | TMS, TDI Data Setup Time                               | $t_{TMSS}, t_{TDIS}$ | 5   | —   | ns   |
| 5   | TMS, TDI Data Hold Time                                | $t_{TMSH}, t_{TDIH}$ | 25  | —   | ns   |
| 6   | TCK Low to TDO Data Valid                              | $t_{TDOV}$           | —   | 20  | ns   |
| 7   | TCK Low to TDO Data Invalid                            | $t_{TDOI}$           | 0   | —   | ns   |
| 8   | TCK Low to TDO High Impedance                          | $t_{TDOHZ}$          | —   | 20  | ns   |
| 9   | JCOMP Assertion Time                                   | $t_{JCOMPW}$         | 100 | —   | ns   |
| 10  | JCOMP Setup Time to TCK Low                            | $t_{JCMPS}$          | 40  | —   | ns   |
| 11  | TCK Falling Edge to Output Valid                       | $t_{BSDV}$           | —   | 50  | ns   |
| 12  | TCK Falling Edge to Output Valid out of High Impedance | $t_{BSDVZ}$          | —   | 50  | ns   |
| 13  | TCK Falling Edge to Output High Impedance              | $t_{BSDHZ}$          | —   | 50  | ns   |
| 14  | Boundary Scan Input Valid to TCK Rising Edge           | $t_{BSDST}$          | 50  | —   | ns   |
| 15  | TCK Rising Edge to Boundary Scan Input Invalid         | $t_{BSDHT}$          | 50  | —   | ns   |

<sup>1</sup> These specifications apply to JTAG boundary scan only. JTAG timing specified at  $V_{DDE} = 3.0V$  to  $5.5V$ ,  $T_A = TL$  to  $TH$ , and  $CL = 30pF$  with  $SRC = 0b11$ .

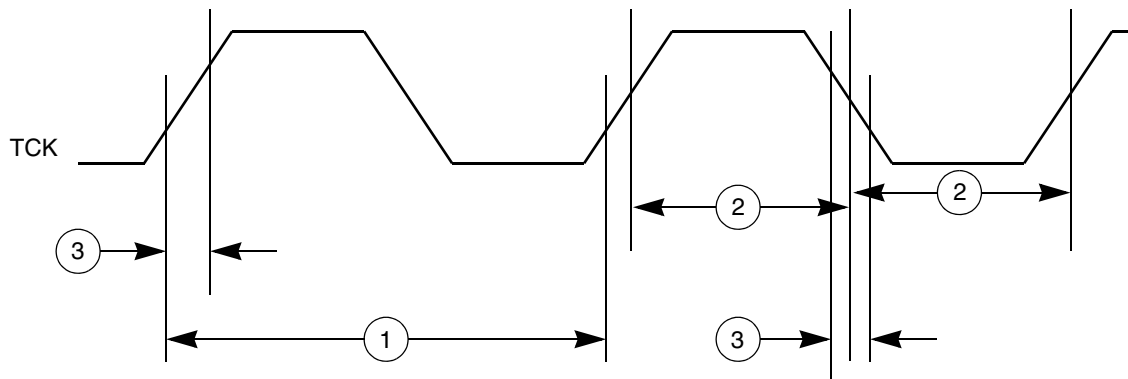


Figure 8. JTAG Test Clock Input Timing

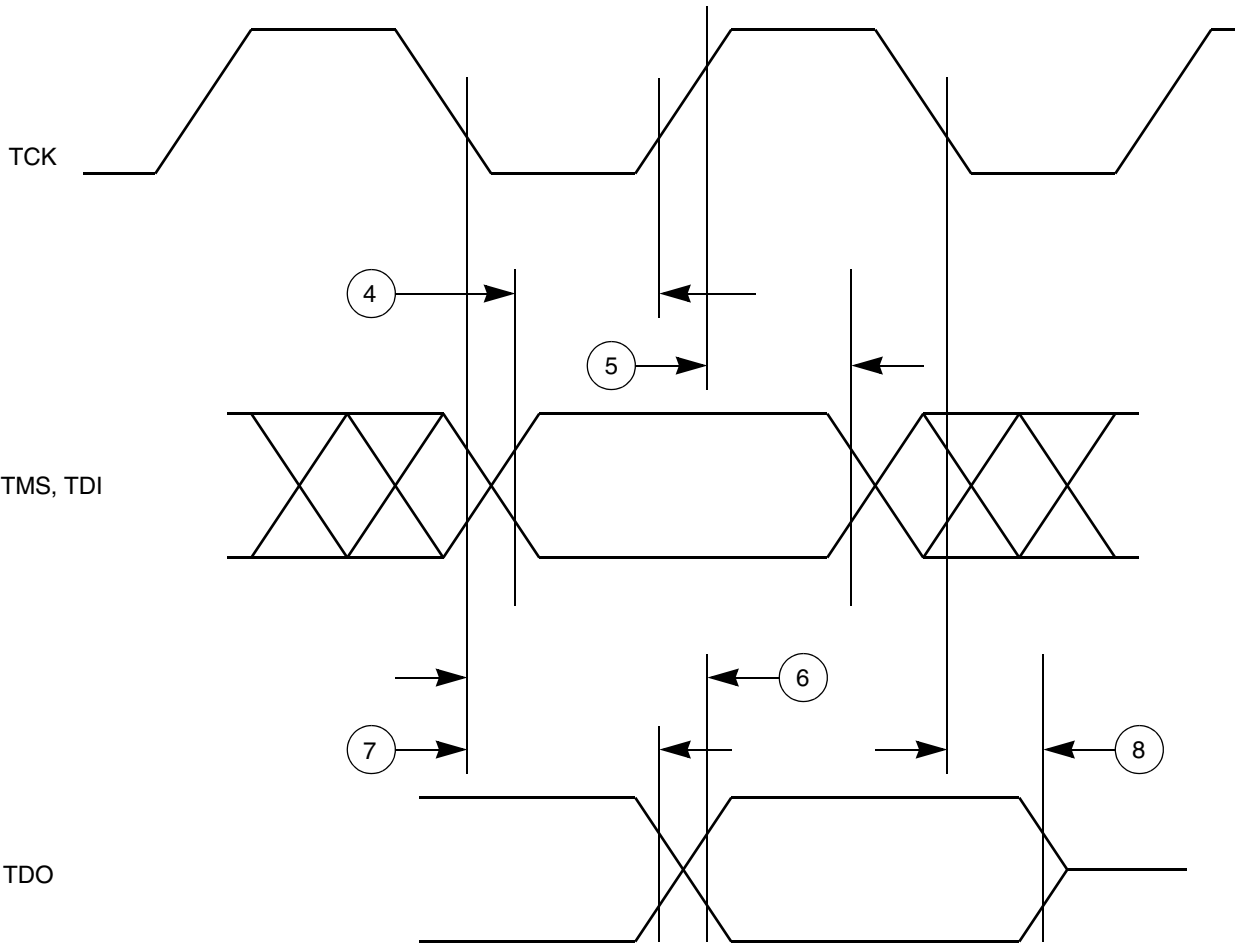


Figure 9. JTAG Test Access Port Timing

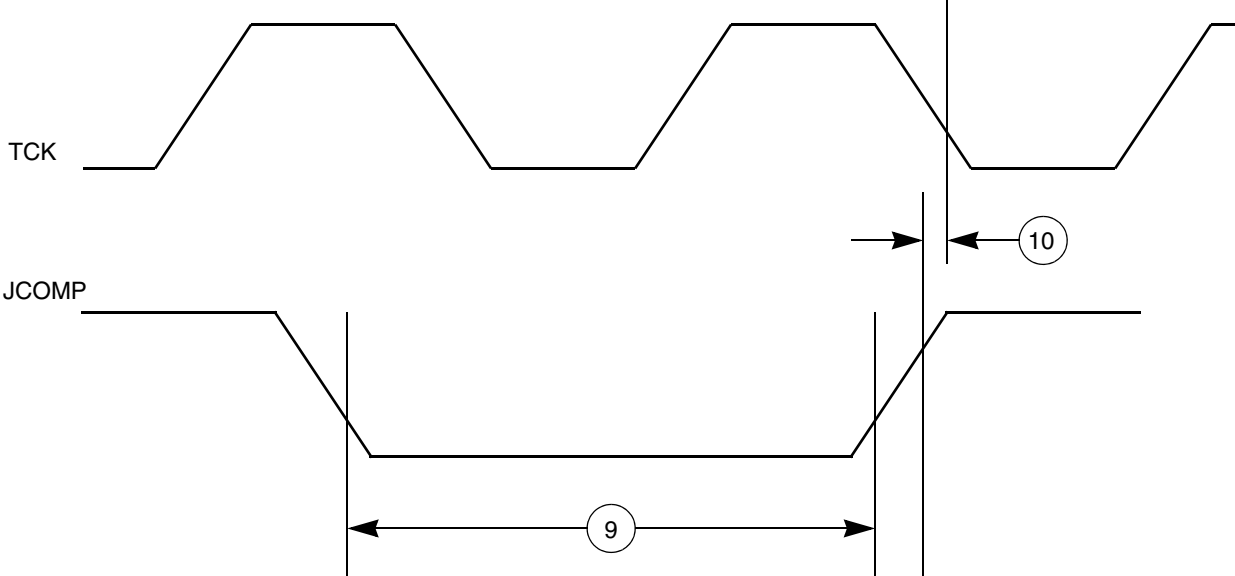


Figure 10. JTAG JCOMP Timing

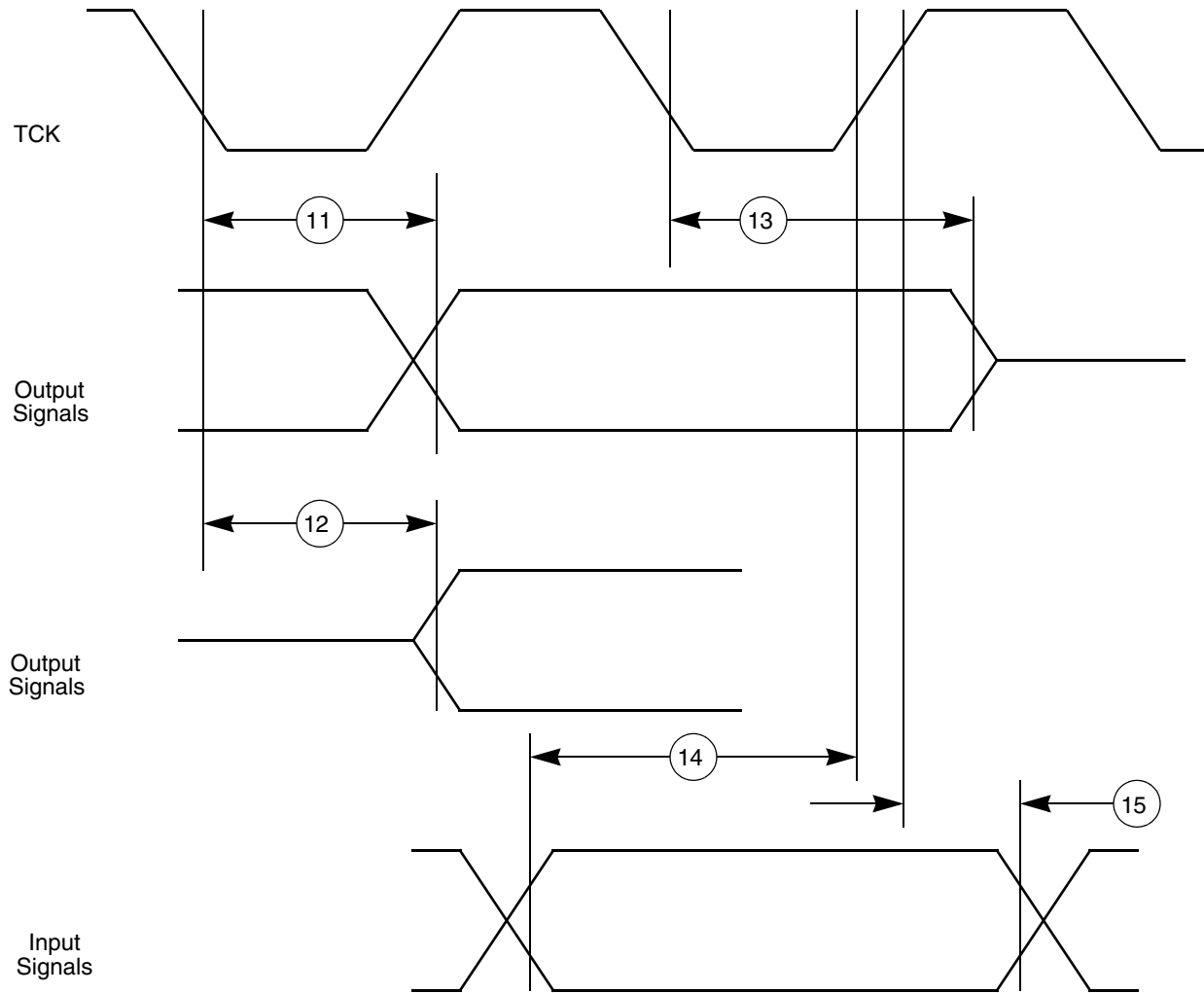


Figure 11. JTAG Boundary Scan Timing

## 2.13.4 Nexus Debug Interface

Table 22. Nexus Debug Port Timing<sup>1</sup>

| Num | Characteristic  | Symbol                  | Min | Max | Unit       |
|-----|---|-------------------------|-----|-----|------------|
| 1   | MCKO Cycle Time                                       | $t_{MCKO}$              | 40  | —   | ns         |
| 2   | MCKO Duty Cycle                                       | $t_{MDC}$               | 40  | 60  | %          |
| 3   | MCKO Low to MDO Data Valid <sup>2</sup>               | $t_{MDOV}$              | -2  | 4.0 | ns         |
| 4   | MCKO Low to $\overline{MSEO}$ Data Valid <sup>2</sup> | $t_{\overline{MSEOV}}$  | -2  | 4.0 | ns         |
| 5   | MCKO Low to $\overline{EVT0}$ Data Valid <sup>2</sup> | $t_{\overline{EVT0V}}$  | -2  | 4.0 | ns         |
| 6   | $\overline{EVTI}$ Pulse Width                         | $t_{\overline{EVTI}PW}$ | 4.0 | —   | $t_{TCYC}$ |
| 7   | $\overline{EVT0}$ Pulse Width                         | $t_{\overline{EVT0}PW}$ | 1   | —   | $t_{MCKO}$ |
| 8   | TCK Cycle Time <sup>3</sup>                           | $t_{TCK}$               | 40  | —   | ns         |
| 9   | TCK Duty Cycle  | $t_{TDC}$               | 40  | 60  | %          |
| 10  | TDI, TMS Data Setup Time                              | $t_{NTDIS}, t_{NTMSS}$  | 8   | —   | ns         |
| 11  | TDI, TMS Data Hold Time                               | $t_{NTDIH}, t_{NTMSH}$  | 4   | —   | ns         |
| 12  | TCK Low to TDO Data Valid                             | $t_{JOV}$               | 0   | 8   | ns         |

<sup>1</sup> JTAG specifications in this table apply when used for debug functionality. All Nexus timing relative to MCKO is measured from 50% of MCKO and 50% of the respective signal. Nexus timing specified at  $V_{DDE} = 3.0V$  to  $5.5V$ ,  $T_A = T_L$  to  $T_H$ , and  $CL = 30pF$  with  $SRC = 0b11$ .

<sup>2</sup> MDO,  $\overline{MSEO}$ , and  $\overline{EVT0}$  data is held valid until next MCKO low cycle.

<sup>3</sup> The system clock frequency needs to be three times faster than the TCK frequency.

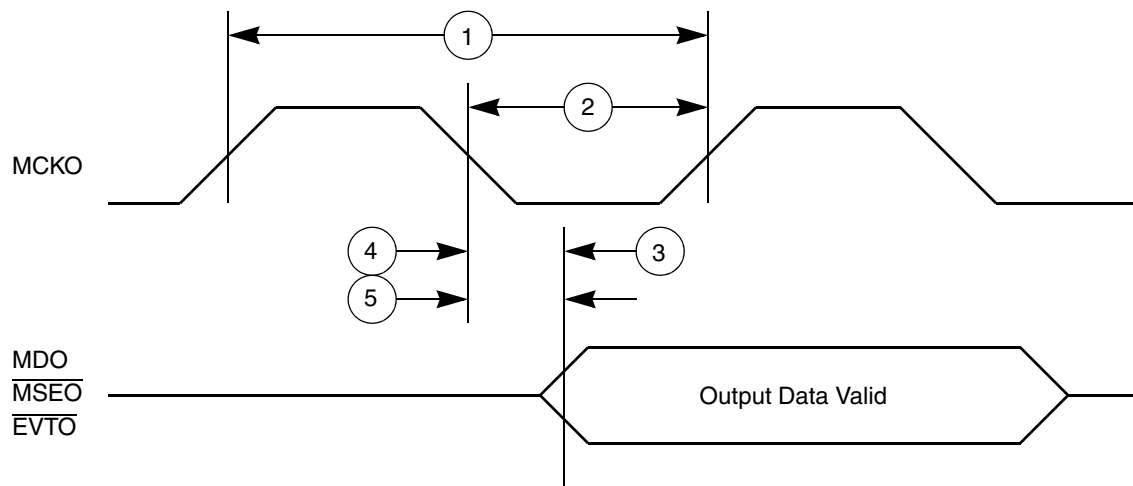


Figure 12. Nexus Output Timing



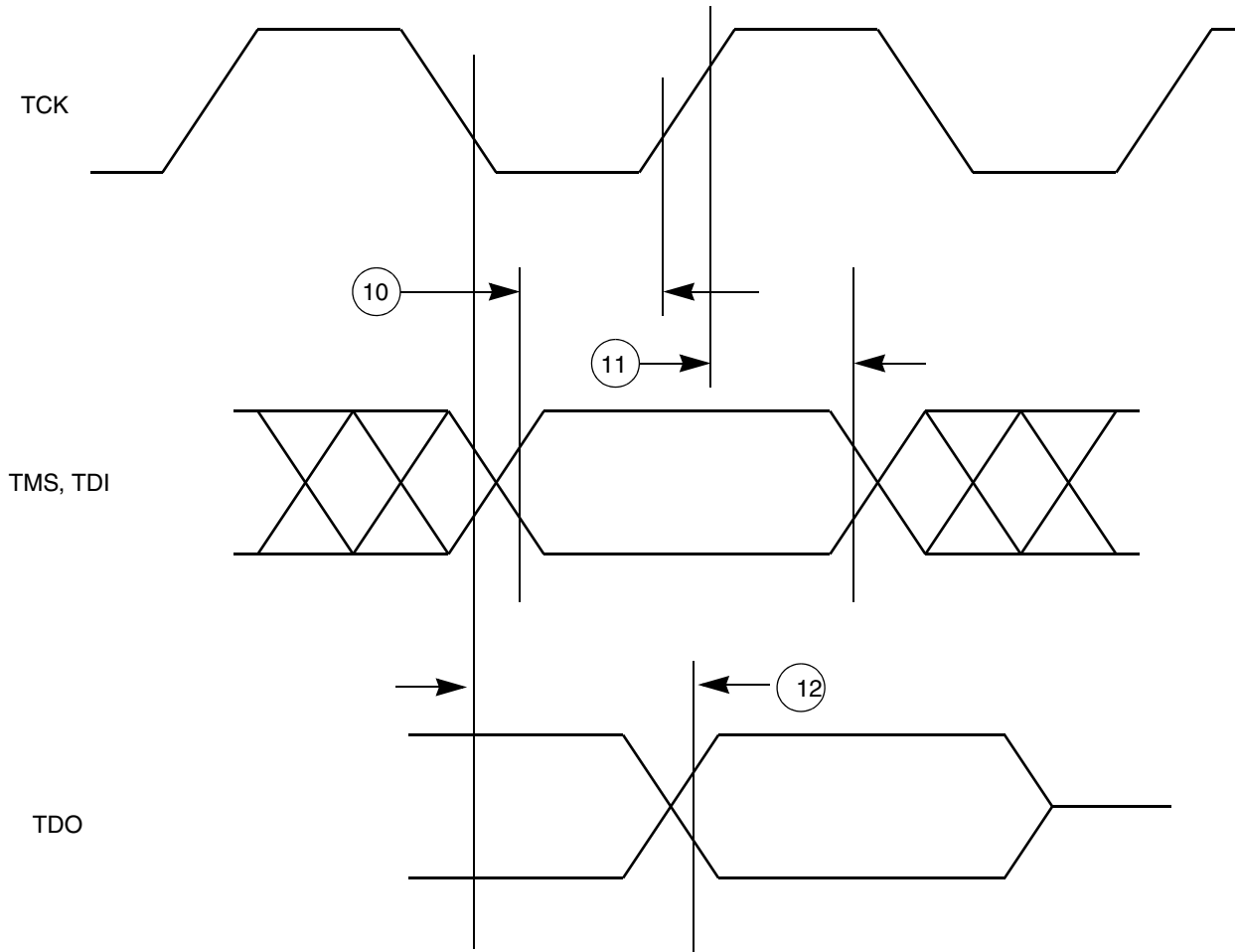


Figure 13. Nexus TDI, TMS, TDO Timing

## 2.13.5 External Bus Interface (EBI)

Table 23. External Bus Operation Timing<sup>1</sup>

| Num | Characteristic  | Symbol       | Min  | Max            | Unit  |
|-----|---|--------------|------|----------------|-------|
| 1   | CLKOUT Period <sup>2</sup>  | $T_C$        | 40.0 | —              | ns    |
| 2   | CLKOUT duty cycle   | $t_{CDC}$    | 45%  | 55%            | $T_C$ |
| 3   | CLKOUT rise time  | $t_{CRT}$    | —    | — <sup>3</sup> | ns    |
| 4   | CLKOUT fall time  | $t_{CFT}$    | —    | — <sup>3</sup> | ns    |
| 5   | CLKOUT Positive Edge to Output Signal Invalid or High Z (Hold Time) | $t_{COH}$    | 2.0  | —              | ns    |
| 6   | CLKOUT Positive Edge to Output Signal Valid (Output Delay)          | $t_{COV}$    | —    | 10.0           | ns    |
| 7   | Input Signal Valid to CLKOUT Posedge (Setup Time)                   | $t_{CIS}$    | 20.0 | —              | ns    |
| 8   | CLKOUT Posedge to Input Signal Invalid (Hold Time)                  | $t_{CIH}$    | 0    | —              | ns    |
| 9   | ALE Pulse Width High Time   | $t_{ALEPWH}$ | 20   | —              | ns    |
| 10  | ALE Fall to AD Invalid  | $t_{ALEAD}$  | 2    | —              | ns    |

<sup>1</sup> EBI timing specified at  $V_{DDE} = 3.0V$  to  $5.5V$ ,  $T_A = T_L$  to  $T_H$ , and  $CL = 50pF$  with  $SIU\_PCRn[Src] = 0b11$ .

<sup>2</sup> Initialize  $SIU\_ECCR[EBDF]$  to meet maximum external bus frequency.

<sup>3</sup> Refer to Medium High Voltage (MH) pad AC specification in [Table 18](#).

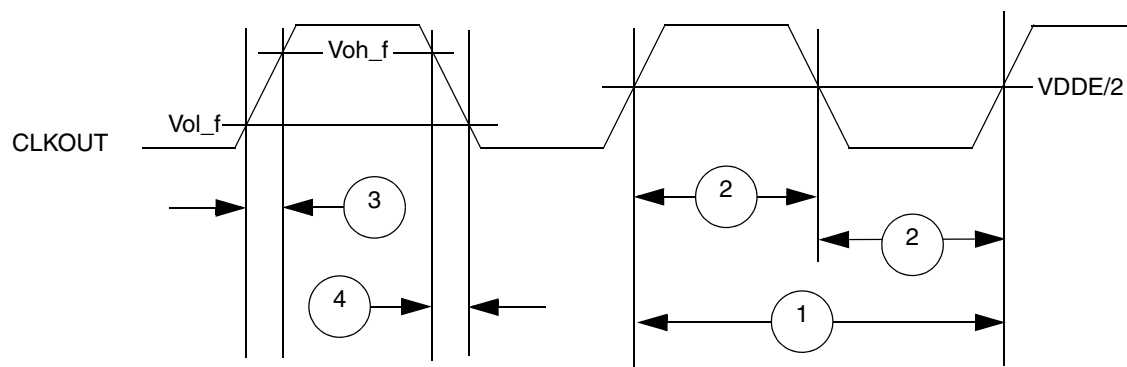


Figure 14. CLKOUT Timing

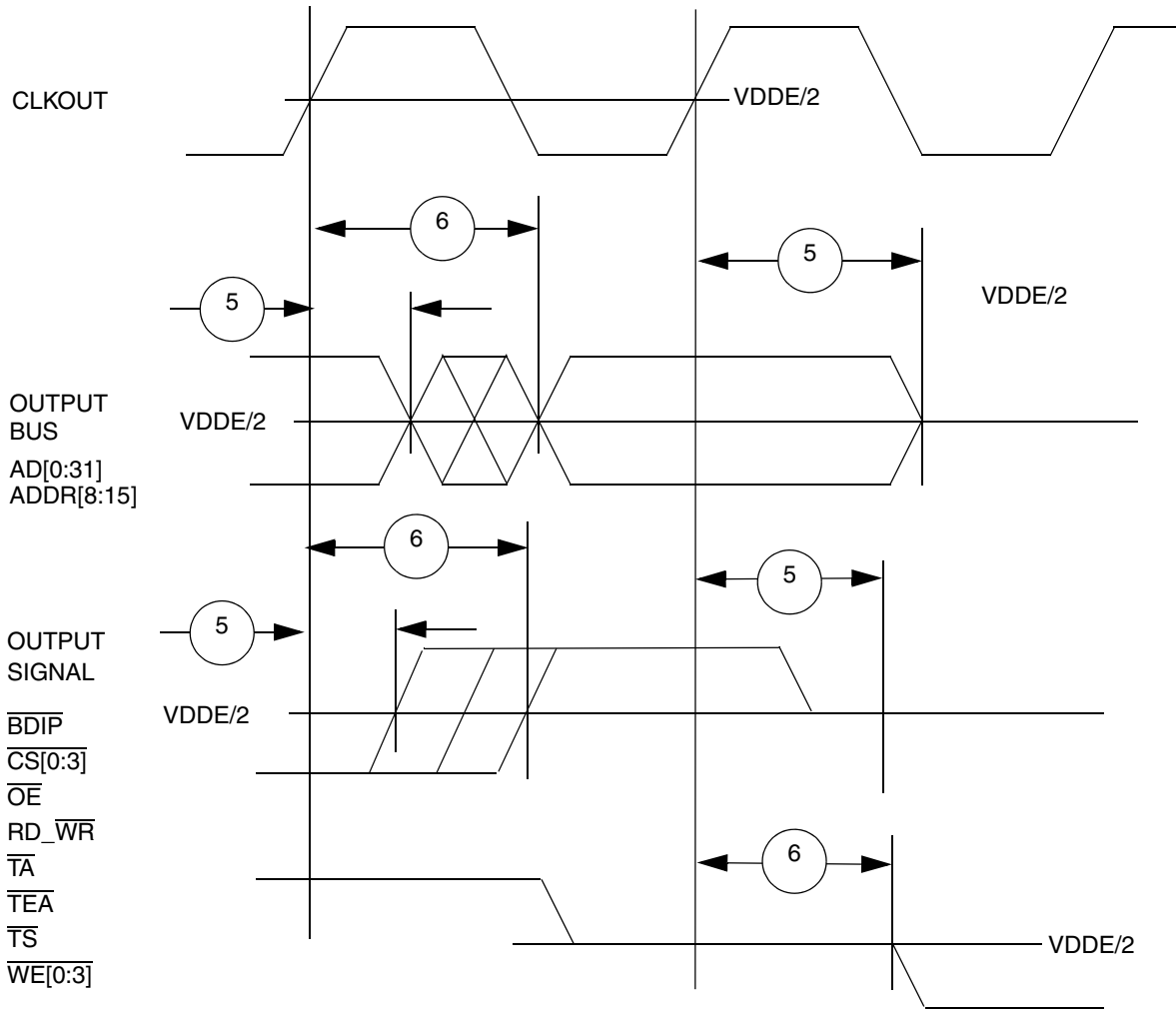


Figure 15. Synchronous Output Timing

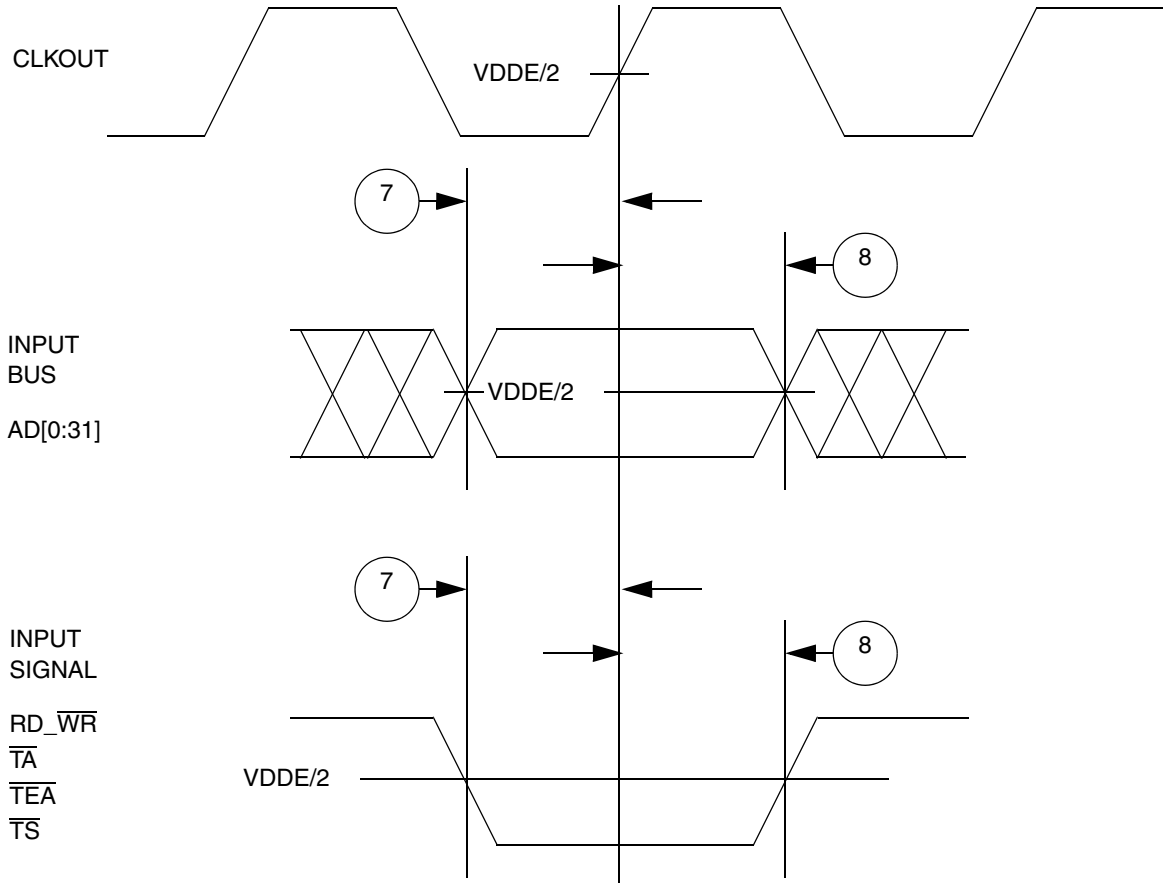


Figure 16. Synchronous Input Timing

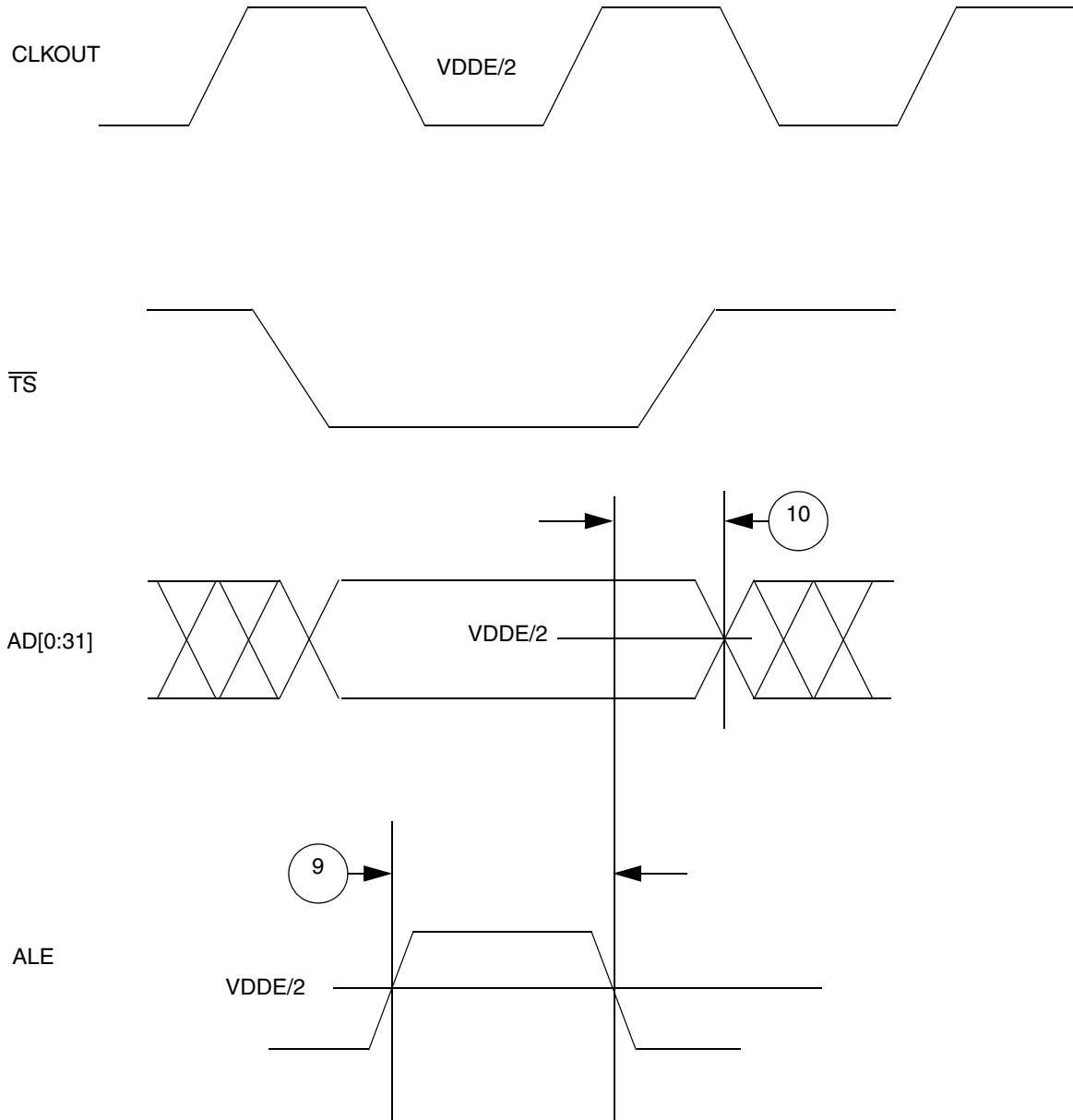


Figure 17. Address Latch Enable (ALE) Timing

### 2.13.6 Enhanced Modular I/O Subsystem (eMIOS)

Table 24. eMIOS Timing

| Num | Characteristic           | Symbol     | Min | Max | Unit      |
|-----|--------------------------|------------|-----|-----|-----------|
| 1   | eMIOS Input Pulse Width  | $t_{MIPW}$ | 4   | —   | $t_{CYC}$ |
| 2   | eMIOS Output Pulse Width | $t_{MOPW}$ | 1   | —   | $t_{CYC}$ |

## 2.13.7 Deserial Serial Peripheral Interface (DSPI)

Table 25. DSPI Timing<sup>1</sup>

| Num | Characteristic   | Symbol     | 66 MHz              |                      | Unit |
|-----|--|------------|---------------------|----------------------|------|
|     |  |            | Min                 | Max                  |      |
| 1   | SCK Cycle Time <sup>2,3</sup>  | $t_{SCK}$  | 60                  | —                    | ns   |
| 2   | PCS to SCK Delay <sup>4</sup>  | $t_{CSC}$  | 20                  | —                    | ns   |
| 3   | After SCK Delay <sup>5</sup>   | $t_{ASC}$  | 20                  | —                    | ns   |
| 4   | SCK Duty Cycle   | $t_{SDC}$  | $t_{SCK}/2$<br>-2ns | $t_{SCK}/2$<br>+ 2ns | ns   |
| 5   | Slave Access Time<br>( $\overline{SS}$ active to SOUT driven)                    | $t_A$      | —                   | 25                   | ns   |
| 6   | Slave SOUT Disable Time<br>( $\overline{SS}$ inactive to SOUT High-Z or invalid) | $t_{DIS}$  | —                   | 25                   | ns   |
| 7   | PCSx to $\overline{PCSS}$ time   | $t_{PCSC}$ | 4                   | —                    | ns   |
| 8   | $\overline{PCSS}$ to PCSx time   | $t_{PASC}$ | 5                   | —                    | ns   |
| 9   | Data Setup Time for Inputs<br>Master (MTFE = 0)                                  | $t_{SUI}$  | 35                  | —                    | ns   |
|     | Slave  |            | 5                   | —                    | ns   |
|     | Master (MTFE = 1, CPHA = 0) <sup>6</sup>   |            | 5                   | —                    | ns   |
|     | Master (MTFE = 1, CPHA = 1)  |            | 35                  | —                    | ns   |
| 10  | Data Hold Time for Inputs<br>Master (MTFE = 0)                                   | $t_{HI}$   | -4                  | —                    | ns   |
|     | Slave  |            | 10                  | —                    | ns   |
|     | Master (MTFE = 1, CPHA = 0) <sup>6</sup>   |            | 26                  | —                    | ns   |
|     | Master (MTFE = 1, CPHA = 1)  |            | -4                  | —                    | ns   |
| 11  | Data Valid (after SCK edge)<br>Master (MTFE = 0)                                 | $t_{SUO}$  | —                   | 15                   | ns   |
|     | Slave  |            | —                   | 35                   | ns   |
|     | Master (MTFE = 1, CPHA=0)  |            | —                   | 30                   | ns   |
|     | Master (MTFE = 1, CPHA=1)  |            | —                   | 15                   | ns   |
| 12  | Data Hold Time for Outputs<br>Master (MTFE = 0)                                  | $t_{HO}$   | -15                 | —                    | ns   |
|     | Slave  |            | 5.5                 | —                    | ns   |
|     | Master (MTFE = 1, CPHA = 0)  |            | 0                   | —                    | ns   |
|     | Master (MTFE = 1, CPHA = 1)  |            | -15                 | —                    | ns   |

<sup>1</sup> DSPI timing specified at VDDE = 3.0V to 5.5V,  $T_A$  = TL to TH, and CL = 50pF with SRC = 0b11.

<sup>2</sup> The minimum SCK Cycle Time restricts the baud rate selection for given system clock rate. These numbers are calculated based on two MPC55xx devices communicating over a DSPI link.

<sup>3</sup> The actual minimum SCK Cycle Time is limited by pad performance.

<sup>4</sup> The maximum value is programmable in DSPI\_CTARx[PSSCK] and DSPI\_CTARx[CSSCK]

<sup>5</sup> The maximum value is programmable in DSPI\_CTARx[PASC] and DSPI\_CTARx[ASC]

<sup>6</sup> This number is calculated assuming the SMPL\_PT bit field in DSPI\_MCR is set to 0b10.

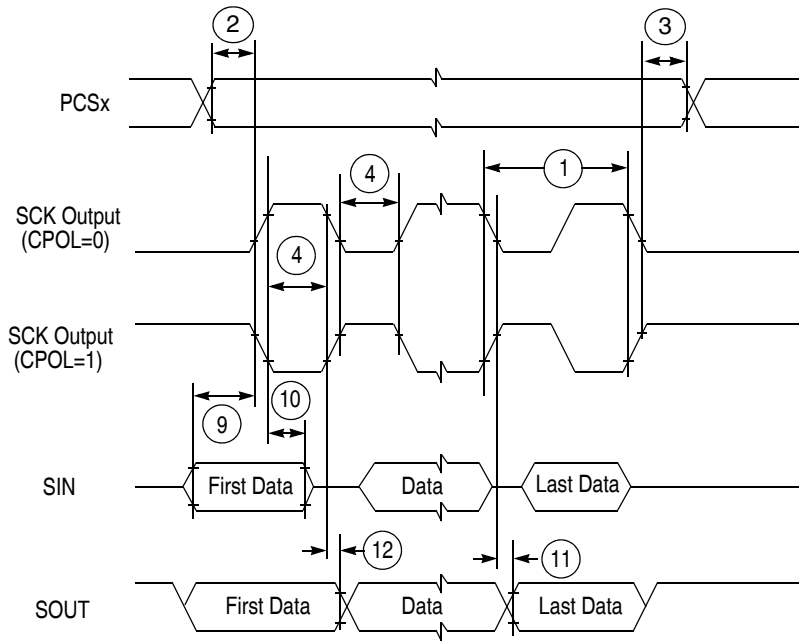


Figure 18. DSPI Classic SPI Timing — Master, CPHA = 0

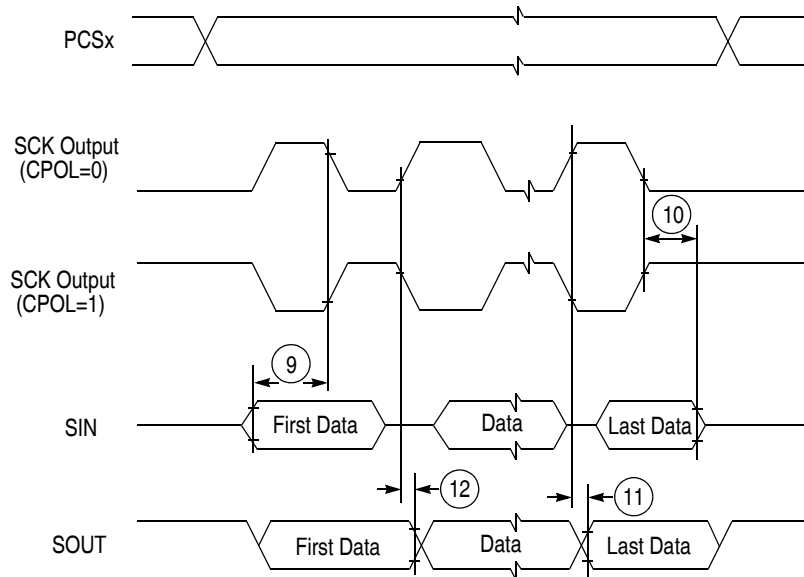


Figure 19. DSPI Classic SPI Timing — Master, CPHA = 1

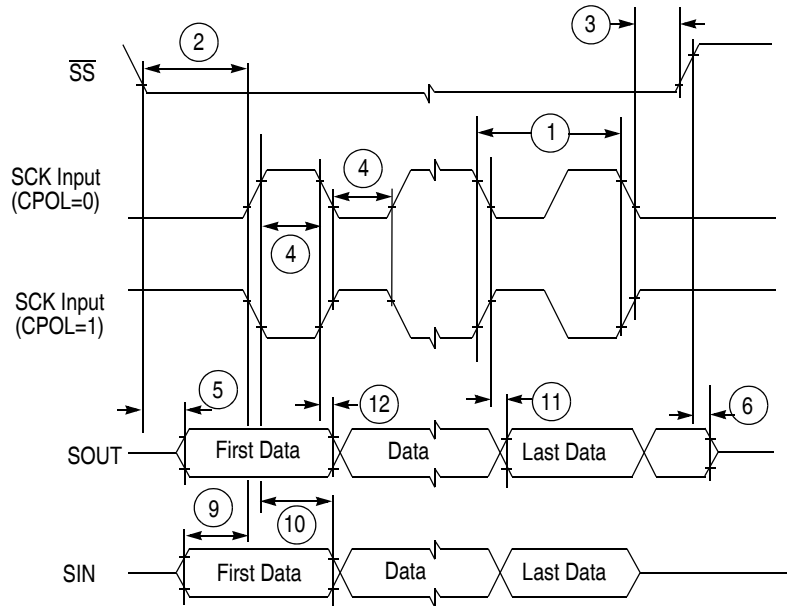


Figure 20. DSPI Classic SPI Timing — Slave, CPHA = 0

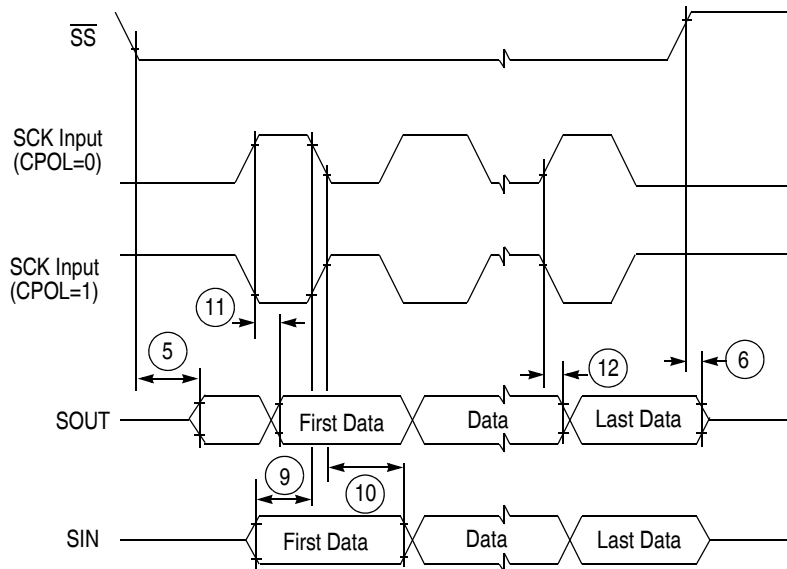


Figure 21. DSPI Classic SPI Timing — Slave, CPHA = 1



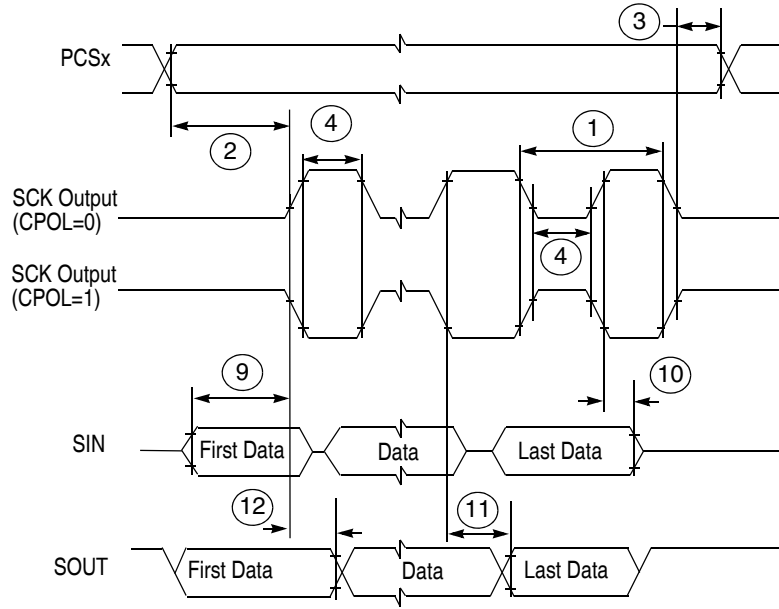


Figure 22. DSPI Modified Transfer Format Timing — Master, CPHA = 0

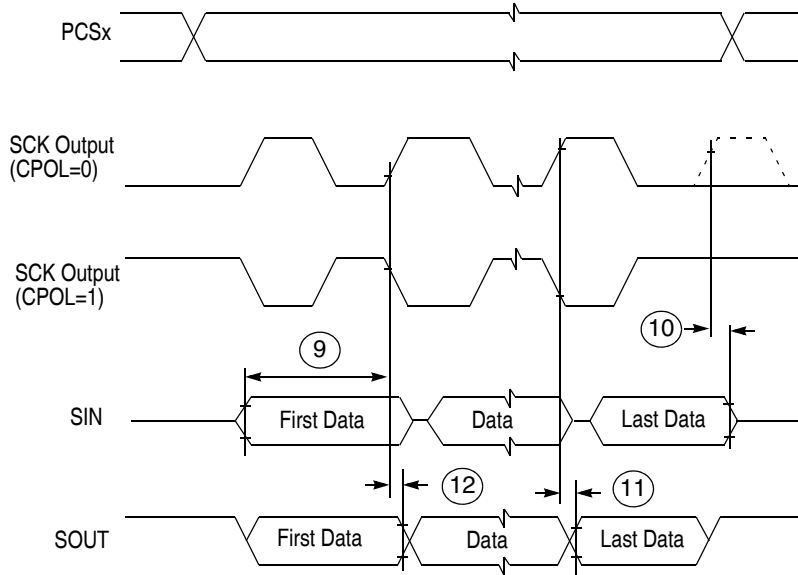


Figure 23. DSPI Modified Transfer Format Timing — Master, CPHA = 1

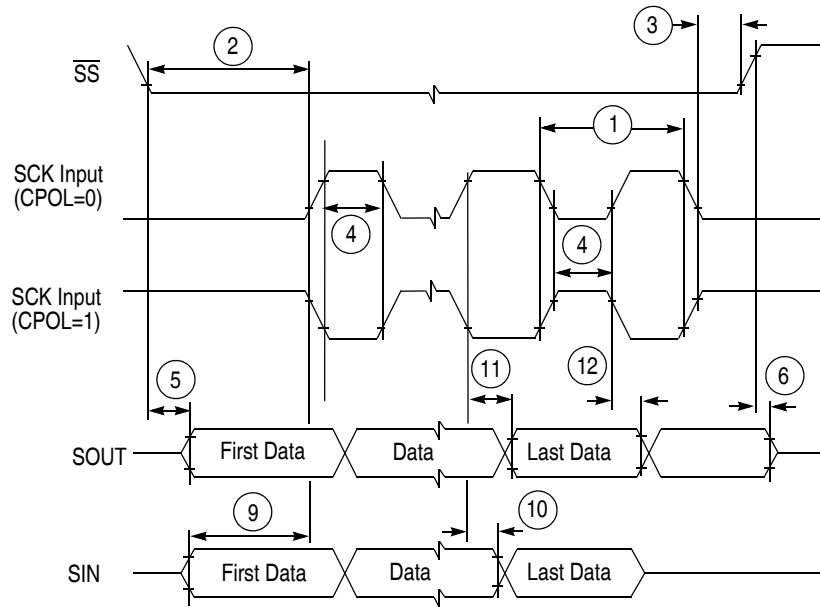


Figure 24. DSPI Modified Transfer Format Timing — Slave, CPHA = 0

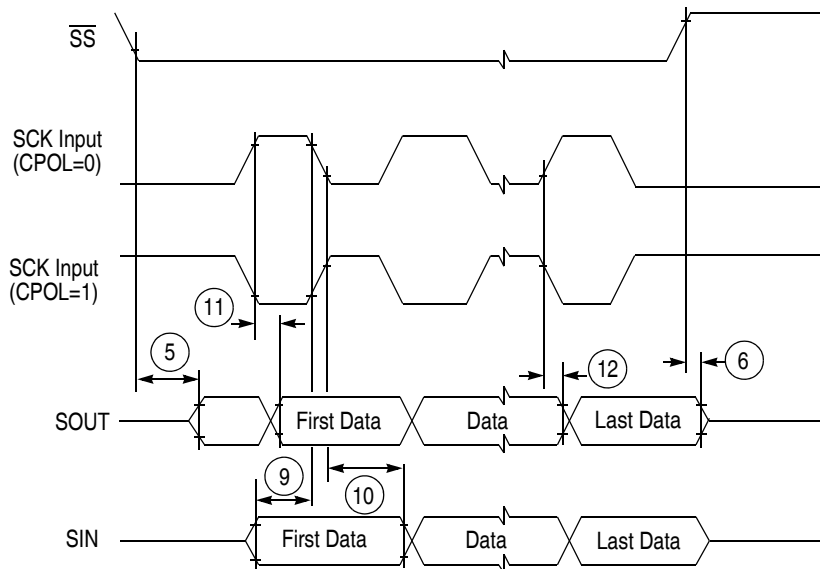


Figure 25. DSPI Modified Transfer Format Timing — Slave, CPHA = 1

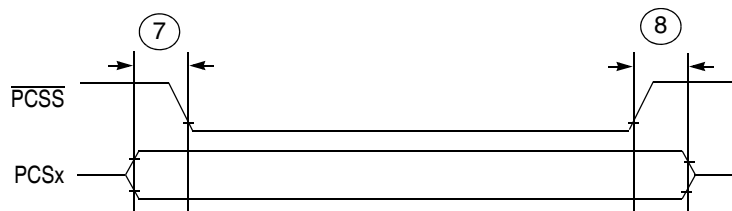


Figure 26. DSPI PCS Strobe ( $\overline{PCSS}$ ) Timing

### 3 Package Information

The latest package outline drawings are available on the product summary pages on our web site: <http://www.nxp.com/powerpc>. The following table lists the package case number per device. Use these numbers in the web page’s “keyword” search engine to find the latest package outline drawings.

**Table 26. Package Information**

| Package    | Package Case Number |
|------------|---------------------|
| 144 LQFP   | 98ASS23177W         |
| 176 LQFP   | 98ASS23479W         |
| 208 MAPBGA | 98ARS23882W         |

### 4 Product Documentation

Documentation is available from a local NXP distributor, a NXP sales office, the NXP Literature Distribution Center, or through the NXP world-wide web address at <http://www.nxp.com/powerpc>.

### 5 Revision History

Table 27 summarizes revisions to this document.

**Table 27. Revision History of MPC5510 Data Sheet**

| Revision | Date   | Substantive Changes   |
|----------|--------|---|
| Rev. 0   | 9/2007 | Initial Release. Preliminary content.   |
| Rev. 1   | 6/2008 | (Note: Change descriptions refer to locations in Rev. 0.)<br>Changed MPC5516 to MPC5510 Family where appropriate.<br>Modified Figure 1. MPC5510 Family Block Diagram.<br>Deleted Table 1. MPC5510 Family Comparison, Maximum Feature Set<br>Deleted Table 2. MPC5510 Peripheral Multiplexing Examples<br>Corrected PK0 and PK1 pin assignments on 208 MAPBGA (Table 3 and Figure 4).<br>Modified Table 4, footnote 4.<br>Modified Table 8. DC Electrical Specifications and table footnotes.<br>Modified Table 9. Operating Currents and table footnotes.<br>Modified Table 12. 3.3V High Frequency External Oscillator, row 5.<br>Modified Table 14. 5V High Frequency (16 MHz) Internal RC Oscillator, row 2.<br>Modified Table 16. FMPLL Electrical Specifications, row 4.<br>Modified Table 17. eQADC Conversion Specifications (Operating) and table footnotes.<br>Modified Table 18. Flash Program and Erase Specifications, row 5.<br>Modified Table 19. Flash EEPROM Module Life (Full Temperature Range), row 1<br>Modified Table 28. Package Information. |

Table 27. Revision History (continued) of MPC5510 Data Sheet

| Revision | Date    | Substantive Changes   |
|----------|---------|---|
| Rev. 2   | 12/2008 | <p>(Note: Change descriptions refer to locations in Rev. 1.)</p> <p>Modified Table 1. MPC5510 Signal Properties: added note to TEST signal.</p> <p>Modified Table 6. DC Electrical Specifications: rows 1b, 5, 8, 9, 10, 11, 16, 19, 25, and footnotes.</p> <p>Modified Table 7. Operating Currents: Max column header, rows 1, 2, 3, 4, and footnotes.</p> <p>Modified Table 9. Low Voltage Monitors: rows 2, 3, 4, 6.</p> <p>Modified Table 10. 3.3V High Frequency External Oscillator: row 1 added footnote, removed duplicate footnote #3.</p> <p>Modified Table 11. 5V Low Frequency (32 kHz) External Oscillator: row 1.</p> <p>Modified Table 12. 5V High Frequency (16 MHz) Internal RC Oscillator: row 2.</p> <p>Modified Table 13. 5V Low Frequency (32 kHz) Internal RC Oscillator: row 2.</p> <p>Modified Table 14. FMPLL Electrical Specifications: rows 1 and 4; added two new rows.</p> <p>Modified Table 15. eQADC Conversion Specifications (Operating): rows 5, 6, 7, 8, 10, 11, and footnotes.</p> <p>Modified Figure 5. Pad Output Delay: moved the dashed horizontal line up so that it crosses the signal midway between top and bottom.</p> |
| Rev. 3   | 3/2009  | <p>(Note: Change descriptions refer to locations in Rev. 2.)</p> <p>Modified Table 4. Thermal Characteristics: all values in 208 MAPBGA column.</p> <p>Modified Table 6. DC Electrical Specifications: spec #1c, added footnote; spec #25, added footnote.</p> <p>Modified Table 7. Operating Currents; spec #5.</p> <p>Modified Table 9. Low Voltage Monitors; spec #1.</p> <p>Modified Table 14. FMPLL Electrical Specifications: updated footnote 3; added spec #10a.</p> <p>Modified Table 15. eQADC Conversion Specifications (Operating): added another footnote.</p> <p>Modified Table 16. Flash Program and Erase Specifications: updated spec #7.</p> <p>Modified Figure 5: Pad Output Delay: adjusted lower timing diagram.</p> <p>Modified Figure 8: JTAG Test Clock Input Timing; updated so that it matches the spec definitions.</p>  |
| Rev. 4   | 7/2014  | Updated the VCO Min. value from 192 to 250 MHz in <a href="#">Table 14</a> .  |
| Rev. 5   | 7/2019  | <p>Changed Freescale to NXP throughout the document.</p> <p>Added footnote "Oscillator circuit performance is highly .....analyzing oscillator circuit functionality" in <a href="#">Table 10</a> and <a href="#">Table 11</a>.</p>   |

## How to Reach Us:

### Home Page:

[nxp.com](http://nxp.com)

### Web Support:

[nxp.com/support](http://nxp.com/support)

Information in this document is provided solely to enable system and software implementers to use NXP products. There are no express or implied copyright licenses granted hereunder to design or fabricate any integrated circuits based on the information in this document. NXP reserves the right to make changes without further notice to any products herein.

NXP makes no warranty, representation, or guarantee regarding the suitability of its products for any particular purpose, nor does NXP assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation consequential or incidental damages. Typical parameters that may be provided in NXP data sheets and/or specifications can and do vary in different applications, and actual performance may vary over time. All operating parameters, including typicals, must be validated for each customer application by customer's technical experts. NXP does not convey any license under its patent rights nor the rights of others. NXP sells products pursuant to standard terms and conditions of sale, which can be found at the following address:  
[nxp.com/SalesTermsandConditions](http://nxp.com/SalesTermsandConditions).

While NXP has implemented advanced security features, all products may be subject to unidentified vulnerabilities. Customers are responsible for the design and operation of their applications and products to reduce the effect of these vulnerabilities on customer's applications and products, and NXP accepts no liability for any vulnerability that is discovered. Customers should implement appropriate design and operating safeguards to minimize the risks associated with their applications and products.

NXP, the NXP logo, NXP SECURE CONNECTIONS FOR A SMARTER WORLD, COOLFLUX, EMBRACE, GREENCHIP, HITAG, I2C BUS, ICODE, JCOP, LIFE VIBES, MIFARE, MIFARE CLASSIC, MIFARE DESFire, MIFARE PLUS, MIFARE FLEX, MANTIS, MIFARE ULTRALIGHT, MIFARE4MOBILE, MIGLO, NTAG, ROADLINK, SMARTLX, SMARTMX, STARPLUG, TOPFET, TRENCHMOS, UCODE, Freescale, the Freescale logo, Altivec, C.5, CodeTEST, CodeWarrior, ColdFire, ColdFire+, C.Ware, the Energy Efficient Solutions logo, Kinetis, Layerscape, MagniV, mobileGT, PEG, PowerQUICC, Processor Expert, QorIQ, QorIQ Qonverge, Ready Play,

SafeAssure, the SafeAssure logo, StarCore, Symphony, VortiQa, Vybrid, Airfast, BeeKit, BeeStack, CoreNet, Flexis, MXC, Platform in a Package, QUICC Engine, SMARTMOS, Tower, TurboLink, and UMEMS are trademarks of NXP B.V. All other product or service names are the property of their respective owners. AMBA, Arm, Arm7, Arm7TDMI, Arm9, Arm11, Artisan, big.LITTLE, Cordio, CoreLink, CoreSight, Cortex, DesignStart, DynamIQ, Jazelle, Keil, Mali, Mbed, Mbed Enabled, NEON, POP, RealView, SecurCore, Socrates, Thumb, TrustZone, ULINK, ULINK2, ULINK-ME, ULINK-PLUS, ULINKpro, ÉpVision, Versatile are trademarks or registered trademarks of Arm Limited (or its subsidiaries) in the US and/or elsewhere. The related technology may be protected by any or all of patents, copyrights, designs and trade secrets. All

rights reserved. Oracle and Java are registered trademarks of Oracle and/or its affiliates. The Power Architecture and Power.org word marks and the Power and Power.org logos and related marks are trademarks and service marks licensed by Power.org.

© 2019 NXP B.V.



# Mouser Electronics

Authorized Distributor

Click to View Pricing, Inventory, Delivery & Lifecycle Information:

## NXP:

[SPC5516GAMMG66](#) [SPC5517SAMLU66](#) [MPC5517GAVMG80](#) [SPC5514EBMLQ66](#) [SPC5514GBMLQ66](#)  
[SPC5515SAMLU66](#) [SPC5515SBMLQ66](#) [SPC5516EAMMG66](#) [SPC5516EBMLQ66](#) [SPC5516GBMLQ66](#)  
[SPC5516SAMLU66](#) [SPC5516SBMLQ66](#) [SPC5517EAMLU66](#) [SPC5517EAMMG66](#) [SPC5517EBMLQ66](#)  
[SPC5517GAMMG66](#) [SPC5517SBMLQ66](#) [SPC5516EAVMG80](#) [SPC5517EAVLU66](#) [SPC5517GAVMG80](#)  
[SPC5514EBVLQ66](#) [SPC5514EAMLQ66](#) [SPC5516EAMLQ48](#) [SPC5517EAVMG80](#) [SPC5517EBMLQ66R](#)  
[SPC5516EAVLQ66R](#) [SPC5517EAVLQ66](#) [SPC5517EBVLQ66R](#) [SPC5517EBVLQ66](#) [SPC5516EACMG48](#)  
[SPC5515SBVLQ48](#)