



Contents

Pin Configuration 3 Maximum Ratings 4 Operating Range 4 DC Electrical Characteristics 4 Capacitance 5 Thermal Resistance 5 AC Test Loads and Waveforms 5 Data Retention Characteristics 6 Data Retention Waveform 6 Switching Characteristics 7 Switching Waveforms 8 Truth Table 10	Product Portfolio	3
Operating Range 4 DC Electrical Characteristics 4 Capacitance 5 Thermal Resistance 5 AC Test Loads and Waveforms 5 Data Retention Characteristics 6 Data Retention Waveform 6 Switching Characteristics 7 Switching Waveforms 8	Pin Configuration	3
Operating Range 4 DC Electrical Characteristics 4 Capacitance 5 Thermal Resistance 5 AC Test Loads and Waveforms 5 Data Retention Characteristics 6 Data Retention Waveform 6 Switching Characteristics 7 Switching Waveforms 8	Maximum Ratings	4
DC Electrical Characteristics	-	
Thermal Resistance		
AC Test Loads and Waveforms	Capacitance	5
Data Retention Characteristics	Thermal Resistance	5
Data Retention Waveform		
Data Retention Waveform	Data Retention Characteristics	6
Switching Characteristics7 Switching Waveforms8		
Switching Waveforms8		
-		

Ordering Information	11
Ordering Code Definitions	11
Package Diagram	
Acronyms	13
Document Conventions	13
Units of Measure	13
Document History Page	14
Sales, Solutions, and Legal Information	15
Worldwide Sales and Design Support	15
Products	15
PSoC® Solutions	15
Cypress Developer Community	15
Technical Support	15

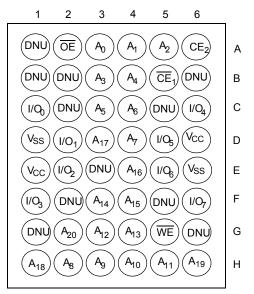


Product Portfolio

					Power Dissipation					
Product	V _{CC} Range (V)		V _{CC} Range (V) Speed Operating I _{CC} (mA) Stands		Operating I _{CC} (mA)		Standhy	Iona(uA)		
Troduct				(ns)	f = 1 MHz		1 MHz f = f _{Max}		— Standby I _{SB2} (μA)	
	Min	Typ ^[1]	Max		Typ ^[1]	Max	Typ ^[1]	Max	Typ ^[1]	Max
CY62168DV30LL	2.2	3.0	3.6	55	2	4	15	30	2.5	22

Pin Configuration

Figure 1. 48-ball VFBGA pinout (Top View) [2]



Notes

Typical values are included for reference only and are not guaranteed or tested. Typical values are measured at V_{CC} = V_{CC(typ.)}, T_A = 25 °C.
 DNU pins have to be left floating or tied to V_{SS} to ensure proper operation.



Maximum Ratings

Exceeding maximum ratings may shorten the useful life of the device. User guidelines are not tested. Storage temperature-65 °C to +150 °C Ambient temperature with Supply voltage to ground potential -0.3 V to V_{CC(max)} + 0.3 V DC voltage applied to outputs in High-Z state $^{[3,\;4]}$ -0.3 V to V $_{\rm CC(max)}$ + 0.3 V

DC input voltage [3, 4]	$-0.3 \text{ V to V}_{CC(max)} + 0.3 \text{ V}$
Output current into outputs (LOW)	,
Static discharge voltage (per MIL-STD-883, Method 3015)	> 2001 V
Latch-up current	> 200 mA

Operating Range

Range	Ambient Temperature (T _A) [5]	V cc ^[6]
Industrial	–40 °C to +85 °C	2.2 V-3.6 V

DC Electrical Characteristics

Over the Operating Range

	5	T	С	CY62168DV30-55		
Parameter	Description	Test Conditions	Min	Typ [7]	Max	Unit
V _{OH}	Output HIGH voltage	$2.2 \text{ V} \le \text{V}_{CC} \le 2.7 \text{ V}$ $I_{OH} = -0.1 \text{ m/s}$	A 2.0	_	_	V
		$2.7 \text{ V} \le \text{V}_{CC} \le 3.6 \text{ V}$ $\text{I}_{OH} = -1.0 \text{ m/s}$	A 2.4	_	_	
V _{OL}	Output LOW voltage	$2.2 \text{ V} \le \text{V}_{CC} \le 2.7 \text{ V}$ $\text{I}_{OL} = 0.1 \text{ mA}$	_	_	0.4	V
		$2.7 \text{ V} \le \text{V}_{CC} \le 3.6 \text{ V}$ $\text{I}_{OL} = 2.1 \text{ mA}$	_	_	0.4	
V _{IH}	Input HIGH voltage	$2.2~\text{V} \leq \text{V}_{\text{CC}} \leq 2.7~\text{V}$	1.8	_	V _{CC} + 0.3	V
		$2.7 \text{ V} \le \text{V}_{CC} \le 3.6 \text{ V}$	2.2	_	V _{CC} + 0.3	
V _{IL}	Input LOW voltage	$2.2~\text{V} \leq \text{V}_{\text{CC}} \leq 2.7~\text{V}$	-0.3	_	0.6	V
		$2.7 \text{ V} \le \text{V}_{CC} \le 3.6 \text{ V}$	-0.3	_	0.8	
I _{IX}	Input leakage current	$GND \le V_I \le V_{CC}$	-1	_	+1	μΑ
I _{OZ}	Output leakage current	$GND \le V_O \le V_{CC}$, Output disabled	-1	_	+1	μΑ
I _{CC}	V _{CC} operating supply current	$f = f_{Max} = 1/t_{RC}$ $V_{CC} = 3.6 V,$	_	15	30	mA
		f = 1 MHz	_	2	4	
I _{SB1}	Automatic CE power-down current – CMOS inputs	$\label{eq:center} \begin{array}{l} \overline{CE}_1 \geq V_{CC} - 0.2 \text{ V, } CE_2 \leq 0.2 \text{ V,} \\ V_{IN} \geq V_{CC} - 0.2 \text{ V or } V_{IN} \leq 0.2 \text{ V,} \\ f = f_{Max} \text{ (Address and data only),} \end{array}$	_	2.5	22	μА
		$f = 0 \ (\overline{OE}, \overline{WE})$				
I _{SB2}	Automatic CE power-down current – CMOS inputs	$\overline{\text{CE}}_1 \ge \text{V}_{\text{CC}} - 0.2 \text{ V}, \text{CE}_2 \le 0.2 \text{ V}, \\ \text{V}_{\text{IN}} \ge \text{V}_{\text{CC}} - 0.2 \text{ V} \text{ or } \text{V}_{\text{IN}} \le 0.2 \text{ V}, \\ \text{f} = 0, \text{V}_{\text{CC}} = 3.6 \text{ V}$	_	2.5	22	μА

- Notes
 3. V_{IL(min)} = -2.0 V for pulse durations less than 20 ns.
 4. V_{IH(max)} = V_{CC} + 0.75 V for pulse durations less than 20 ns.
 5. T_A is the "Instant-On" case temperature.
 6. Full device AC operation assumes a 100 μs ramp time from 0 to V_{CC}(min) and 100 μs wait time after V_{CC} stabilization.
 7. Typical values are included for reference only and are not guaranteed or tested. Typical values are measured at V_{CC} = V_{CC(typ.)}, T_A = 25 °C.



Capacitance

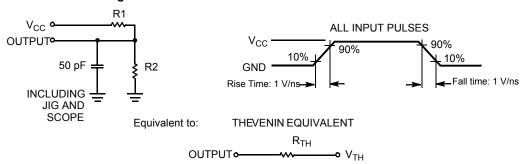
Parameter [8]	Description	Test Conditions	Max	Unit
C _{IN}	Input capacitance	$T_A = 25 {}^{\circ}\text{C}, f = 1 \text{MHz}, V_{CC} = V_{CC(typ.)}$	8	pF
C _{OUT}	Output capacitance		10	pF

Thermal Resistance

Parameter [8]	Description	Test Conditions	VFBGA	Unit
U/A		Still air, soldered on a 3 × 4.5 inch, two-layer printed circuit board	55	°C/W
θ JC	Thermal resistance (junction to case)		16	°C/W

AC Test Loads and Waveforms

Figure 2. AC Test Loads and Waveforms



Parameters	2.5 V	3.0 V	Unit
R1	16600	1103	Ω
R2	15400	1554	Ω
R _{TH}	8000	645	Ω
V _{TH}	1.2	1.75	V

Note

^{8.} Tested initially and after any design or process changes that may affect these parameters.



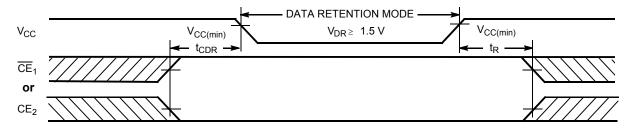
Data Retention Characteristics

Over the Operating Range

Parameter	Description	Conditions	Min	Typ ^[10]	Max	Unit
V_{DR}	V _{CC} for data retention		1.5	-	3.6	V
I _{CCDR}	Data retention current	V _{CC} = 1.5 V,	_	-	10	μА
		$\overline{\text{CE}}_1 > \text{V}_{\text{CC}} - 0.2 \text{ V or } \text{CE}_2 \le 0.2 \text{ V},$				
		$V_{IN} > V_{CC} - 0.2 \text{ V or } V_{IN} \le 0.2 \text{ V}$				
t _{CDR} ^[9]	Chip deselect to data retention time		0	_	-	ns
t _R ^[11]	Operation recovery time		55	_	_	ns

Data Retention Waveform

Figure 3. Data Retention Waveform



<sup>Notes
9. Tested initially and after any design or process changes that may affect these parameters.
10. Typical values are included for reference only and are not guaranteed or tested. Typical values are measured at V_{CC} = V_{CC(typ)}, T_A = 25 °C.
11. Full Device AC operation requires linear V_{CC} ramp from V_{DR} to V_{CC(min)} > 100 μs or stable at V_{CC(min)} > 100 μs.</sup>



Switching Characteristics

Over the Operating Range

Parameter [12]	Description	55	ns	I I mit
Parameter [12]	Description	Min	Max	Unit
Read Cycle		•	•	
t _{RC}	Read cycle time	55	_	ns
t _{AA}	Address to data valid	_	55	ns
t _{OHA}	Data hold from address change	10	_	ns
t _{ACE}	CE ₁ LOW and CE ₂ HIGH to data valid	-	55	ns
t _{DOE}	OE LOW to data valid	_	25	ns
t _{LZOE}	OE LOW to low Z [13]	5	_	ns
t _{HZOE}	OE HIGH to high Z [13, 14]	_	20	ns
t _{LZCE}	CE ₁ LOW and CE ₂ HIGH to low Z ^[13]	10	_	ns
t _{HZCE}	CE ₁ HIGH or CE ₂ LOW to high Z [13, 14]	_	20	ns
t _{PU}	CE ₁ LOW and CE ₂ HIGH to power-up	0	_	ns
t _{PD}	CE ₁ HIGH or CE ₂ LOW to power-down	_	55	ns
Write Cycle [15	, 16]			
t _{WC}	Write cycle time	55	_	ns
t _{SCE}	CE ₁ LOW and CE ₂ HIGH to write end	40	_	ns
t _{AW}	Address setup to write end	40	_	ns
t _{HA}	Address hold from write end	0	_	ns
t _{SA}	Address setup to write start	0	_	ns
t _{PWE}	WE Pulse width	40	_	ns
t _{SD}	Data setup to write end	25	_	ns
t _{HD}	Data hold from write end	0	_	ns
t _{HZWE}	WE LOW to high Z [13, 14]	_	20	ns
t _{LZWE}	WE HIGH to low Z [13]	10	_	ns

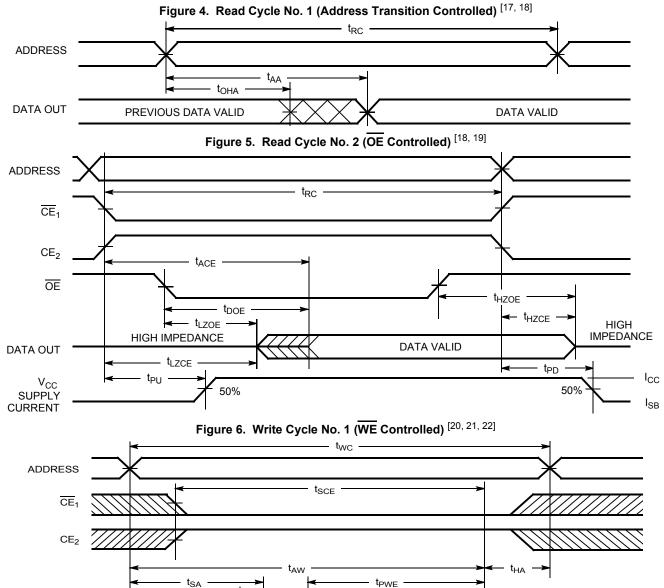
Notes

 ^{12.} Test conditions for all parameters other than tri-state parameters assume signal transition time of 3ns or less (1V/ns), timing reference levels of V_{CC(typ.)}/2, input pulse levels of 0 to V_{CC(typ.)}, and output loading of the specified I_{OL}/I_{OH} as shown in the "AC Test Loads and Waveforms" section.
 13. At any temperature and voltage condition, t_{HZCE} is less than t_{LZCE}, t_{HZOE} is less than t_{LZOE}, and t_{HZWE} for any device.
 14. t_{HZCE}, t_{HZCE}, and t_{HZWE} transitions are measured when the outputs enter a high impedance state.

^{15.} The internal write time of the memory is defined by the overlap of WE, CE₁ = V_{IL}, and CE₂ = V_{IH}. All signals must be ACTIVE to initiate a write and any of these signals can terminate a write by going INACTIVE. The data input setup and hold timing should be referenced to the edge of the signal that terminates the write.
16. The minimum write pulse width for Write Cycle No. 3 (WE Controlled, OE LOW) should be equal to sum of t_{SD} and t_{HZWE}.



Switching Waveforms



Notes

17. <u>Device</u> is continuously selected. \overline{OE} , $\overline{CE}_1 = V_{IL}$, $CE_2 = V_{IH}$.

See Note 23

18. WE is HIGH for read cycle.

DATA I/O

WE

OE

- 18. WE is HIGH for read cycle.

 19. Address valid prior to or coincident with \overline{CE}_1 transition LOW and \underline{CE}_2 transition HIGH.

 20. The internal write time of the memory is defined by the overlap of \overline{WE} , $\overline{CE}_1 = V_{IL}$, and $\overline{CE}_2 = V_{IH}$. All signals must be ACTIVE to initiate a write and any of these signals can terminate a write \underline{by} going INACTIVE. The data input setup and hold timing should be referenced to the edge of the signal that terminates the write.

 21. \underline{Data} I/O is high impedance if $\overline{OE} = V_{IH}$.

 22. If \overline{CE}_1 goes HIGH or \overline{CE}_2 goes LOW simultaneously with \overline{WE} HIGH, the output remains in high-impedance state.

 23. During this period, the I/Os are in output state and input signals should not be applied.

 t_{SD}

VALID DATA

 t_{HD}



DATA I/O

Switching Waveforms (continued)

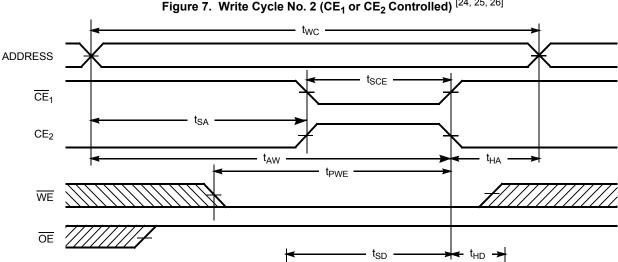
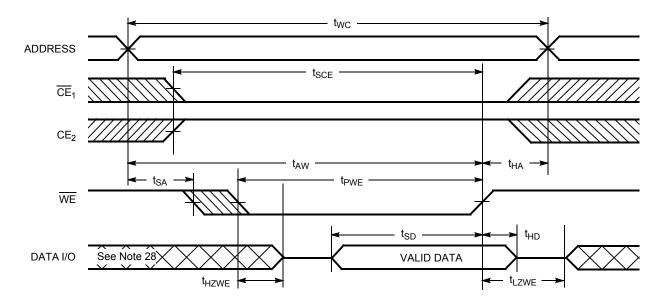


Figure 7. Write Cycle No. 2 ($\overline{\text{CE}}_1$ or CE_2 Controlled) [24, 25, 26]

Figure 8. Write Cycle No. 3 (WE Controlled, OE LOW) [27]

VALID DATA



^{24.} The internal write time of the memory is defined by the overlap of \overline{WE} , $\overline{CE}_1 = V_{IL}$, and $CE_2 = V_{IH}$. All signals must be ACTIVE to initiate a write and any of these signals can terminate a write by going INACTIVE. The data input setup and hold timing should be referenced to the edge of the signal that terminates the write.

25. Data I/O is high impedance if $\overline{OE} = V_{IH}$.

26. If \overline{CE}_1 goes HIGH or CE_2 goes LOW simultaneously with \overline{WE} HIGH, the output remains in high-impedance state.

27. The minimum write cycle pulse width should be equal to sum of t_{SD} and t_{HZWE} .

28. During this period, the I/Os are in output state and input signals should not be applied.



Truth Table

CE ₁	CE ₂	WE	OE	Inputs/Outputs	Mode	Power
Н	Х	Χ	Χ	High Z	Deselect/Power-down	Standby (I _{SB})
Х	L	Х	Х	High Z	Deselect/Power-down	Standby (I _{SB})
L	Н	Н	L	Data out (I/O ₀ –I/O ₇)	Read	Active (I _{CC})
L	Н	L	Х	Data in (I/O ₀ –I/O ₇)	Write	Active (I _{CC})
L	Н	Н	Н	High Z	Output disabled	Active (I _{CC})



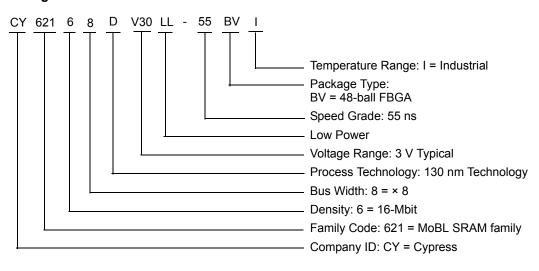
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The following table contains only the parts that are currently available. If you do not see what you are looking for, contact your local sales representative. For more information, visit the Cypress website at http://www.cypress.com and see product summary page at http://www.cypress.com/products. Cypress maintains a worldwide network of offices, solution centers, manufacturers representatives and distributors. To find the office closest to you, visit us at http://www.cypress.com/go/datasheet/offices.

Speed (ns)	Ordering Code	Package Diagram	Package Type	Operating Range
55	CY62168DV30LL-55BVI	51-85178	48-ball FBGA (8 × 9.5 × 1 mm)	Industrial

Please contact your local Cypress sales representative for availability of these parts.

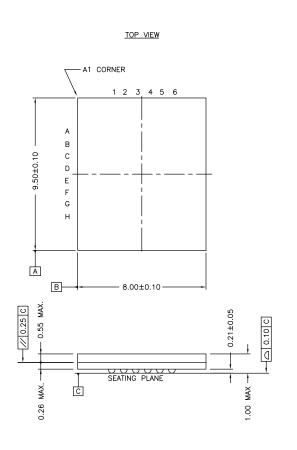
Ordering Code Definitions

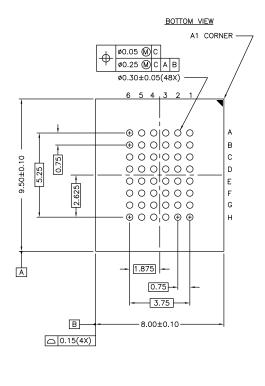




Package Diagram

Figure 9. 48-ball VFBGA (8 \times 9.5 \times 1.0 mm) BV48B Package Outline, 51-85178





51-85178 *C

Document Number: 38-05329 Rev. *M



Acronyms

Acronym	Description			
CMOS	Complementary Metal Oxide Semiconductor			
I/O	Input/Output			
SRAM	Static Random Access Memory			
VFBGA	Very Fine-Pitch Ball Grid Array			
TSOP	Thin Small Outline Package			

Document Conventions

Units of Measure

Symbol	Unit of Measure			
°C	degree Celsius			
MHz	megahertz			
μΑ	microampere			
mA	milliampere			
ns	nanosecond			
Ω	ohm			
pF	picofarad			
V	volt			
W	watt			



Document History Page

Document Title: CY62168DV30 MoBL [®] , 16-Mbit (2 M × 8) Static RAM Document Number: 38-05329					
Revision	ECN	Orig. of Change	Submission Date	Description of Change	
**	118409	GUG	09/30/02	New data sheet.	
*A	123693	DPM	02/05/03	Changed status from Advance Information to Preliminary. Added Package Diagram.	
*B	126556	DPM	04/24/03	Minor change: Change sunset owner from DPM to HRT	
*C	132869	XRJ	01/15/04	Changed status from Preliminary to Final.	
*D	272589	PCI	See ECN	Added Pb-free package related information in all instances across the document. Updated Ordering Information.	
*E	335864	PCI	See ECN	Updated Pin Configuration: Updated Figure 1 (Added Address A ₂₀ to ball G2). Updated Ordering Information: Removed redundant packages.	
*F	492895	VKN	See ECN	Changed address of Cypress Semiconductor Corporation on Page 1 from "3901 North First Street" to "198 Champion Court" Removed 70 ns speed bin related information in all instances across the document. Removed Low Power parts related information in all instances across the document. Updated Ordering Information.	
*G	2914085	NIKM	04/15/10	Updated Ordering Information: Removed inactive parts. Updated Package Diagram.	
*H	3070774	RAME	10/27/10	Changed all table notes to footnotes in all instances across the document. Added Ordering Code Definitions. Added Acronyms and Units of Measure. Updated to new template.	
*	3090588	AJU	11/19/10	Post to external web.	
*J	3329789	RAME	07/27/11	Updated Functional Description: Removed Note "For best-practice recommendations, please refer to the Cypress application note entitled System Design Guidelines, available at http://www.cypress.com website" and its reference. Updated to new template.	
*K	4192919	VINI	11/15/2013	Updated Package Diagram: spec 51-85178 – Changed revision from *A to *C. Updated to new template. Completing Sunset Review.	
*L	4574377	VINI	11/19/2014	Updated Functional Description: Added "For a complete list of related documentation, click here." at the end	
*M	5036233	VINI	12/03/2015	Updated Switching Characteristics: Added Note 16 and referred the same note in "Write Cycle". Updated Switching Waveforms: Added Note 27 and referred the same note in Figure 8. Updated to new template. Completing Sunset Review.	



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