ABSOLUTE MAXIMUM RATINGS

Analog Supply Voltage (V_{CC} - V_{EE}) ....+12V
Digital Supply Voltage (V_{DD}) ....+7V
Differential Input Voltage..................(V_{EE} - 0.3V) to (V_{CC} + 0.3V)
Common Mode Input Voltage..........(V_{EE} - 0.3V) to (V_{CC} + 0.3V)
Latch Input Voltage
(MAX9202/MAX9203 only) ....-0.3V to (V_{DD} + 0.3V)
Output Short-Circuit Duration
To GND ....Continuous
To V_{DD} 1min

Continuous Power Dissipation (T_A = +70°C)
8-Pin SOT23-8 (derate 9.1mW/°C above +70°C) ...727mW/°C
8-Pin SO (derate 5.9mW/°C above +70°C).............471mW/°C
14-Pin TSSOP (derate 9.1mW/°C above +70°C) ....727mW/°C
14-Pin SO (derate 8.3mW/°C above +70°C)...........667mW/°C
16-Pin TSSOP (derate 9.4mW/°C above +70°C) ....755mW/°C
16-Pin SO (derate 8.7mW/°C above +70°C)...........696mW/°C
Operating Temperature Range ....-45°C to +85°C
Junction Temperature..+150°C
Storage Temperature Range ....-65°C to +150°C
Lead Temperature (soldering, 10s) ....+300°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

(V_{CC} = +5V, V_{EE} = -5V, V_{DD} = +5V, GND = 0, V_{CM} = 0, LATCH_ = logic high, T_A = -40°C to +85°C. Typical values are at T_A = +25°C, unless otherwise noted.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
Analog Supply Voltage Range	V_{CC} - V_{EE}	Referenced to V_{EE}		4.75		10.5	V
Digital Supply Voltage Range	V_{DD}	Referenced to GND		4.75		5.25	V
Input Offset Voltage	V_{OS}	V_{CM} = 0, V_{OUT}= 1.4V	T_A = +25°C		1	4	mV
			T_A = -40°C to +85°C			7.5	
Input Bias Current	I_B	I_{IN+} or I_{IN-}	T_A = +25°C		1.25	5	µA
			T_A = -40°C to +85°C			7.0	
Input Offset Current	I_{OS}	V_{CM} = 0, V_{OUT} = 1.4V	T_A = +25°C		50	250	nA
			T_A = -40°C to +85°C			450	
Common-Mode Input Voltage Range	V_{CM}	Note 2		V_{EE} - 0.1		V_{CC} - 2.25	V
Common-Mode Rejection Ratio	CMRR	-5.1V < V_{CM} < +2.75V V_{OUT} = 1.4V	T_A = +25°C		50	150	µV/V
			T_A = -40°C to +85°C			250	
Power-Supply Rejection Ratio	PSRR	Note 3	T_A = +25°C		50	150	µV/V
			T_A = -40°C to +85°C			250	
Output High Voltage	V_{OH}	(V_{IN+} - V_{IN-}) > 250mV, I_{SOURCE} = 1mA		3.0	3.5		V
Output Low Voltage	V_{OL}	(V_{IN+} - V_{IN-}) < -250mV, I_{SINK} = 8mA			0.25	0.4	V
Latch Input Threshold Voltage High	V_{LH}	Note 4			1.4	2	V
Latch Input Threshold Voltage Low	V_{LL}	Note 4		0.8	1.4		V
Latch Input Current High	I_{LH}	V_{LH} = 3.0V, Note 4			0.5	3	µA
Latch Input Current Low	I_{LL}	V_{LL} = 0.3V, Note 4			0.5	3	µA
Input Capacitance	C_{IN}				4		pF
Differential Input Impedance	R_{IND}				5		MΩ
Common-Mode Input Impedance	R_{INCM}				5.5		MΩ
Positive Analog Supply Current	I_{CC}	Note 5	MAX9201		4.7	7	mA
			MAX9202		2.5	4.0	
			MAX9203		1.3	2	

ELECTRICAL CHARACTERISTICS (continued)

(V_{CC} = +5V, V_{EE} = -5V, V_{DD} = +5V, GND = 0, V_{CM} = 0, LATCH_ = logic high, T_A = -40°C to +85°C. Typical values are at T_A = +25°C, unless otherwise noted.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
Negative Analog Supply Current	I_{EE}	Note 5	MAX9201		3.4	5.0	mA
			MAX9202		1.8	3.0	
			MAX9203		1.0	1.6	
Digital Supply Current	I_{DD}	Note 5	MAX9201		2	3.0	mA
			MAX9202		1	1.5	
			MAX9203		0.5	0.8	
Power Dissipation	P_D	$V_{CC} = V_{DD}$ = +5V, V_{EE} = 0V	MAX9201		33	44	mW
			MAX9202		17	24	
			MAX9203		9	13	

TIMING CHARACTERISTICS

(V_{CC} = +5V, V_{EE} = -5V, V_{DD} = +5V, GND = 0, V_{CM} = 0, LATCH_ = logic high, T_A = -40°C to +85°C. Typical values are at T_A = +25°C, unless otherwise noted.) (Notes 1, 6)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
Input-to-Output High Response Time	t_{PD+}	V_{OD} = 5mV, C_L = 15pF, I_{OUT} = 2mA	T_A = +25°C		7	9	ns
			T_A = -40°C to +85°C			12	
Input-to-Output Low Response Time	t_{PD-}	V_{OD} = 5mV, C_L = 15pF, I_{OUT} = 2mA	T_A = +25°C		7	9	ns
			T_A = -40°C to +85°C			12	
Rise Time	t_R	C_L = 15pF, I_{OUT} = 2mA	T_A = +25°C		2.0		ns
Fall Time	t_F	C_L = 15pF, I_{OUT} = 2mA	T_A = +25°C		1.0		ns
Difference in Response Time Between Outputs	Δt_{PD}	Note 7	T_A = +25°C		0.5	1.5	ns
			T_A = -40°C to +85°C			2.5	
Latch Disable to Output High Delay	$t_{PD+}(D)$	Note 4			10		ns
Latch Disable to Output Low Delay	$t_{PD-}(D)$	Note 4			10		ns
Minimum Setup Time	t_S	Note 4			2		ns
Minimum Hold Time	t_N	Note 4			1		ns
Minimum Latch Disable Pulse Width	$t_{PW}(D)$	Note 4			8		ns

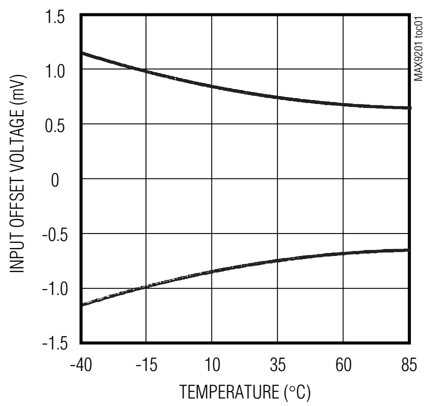
Note 1: All devices are 100% production tested at T_A = +25°C. All temperature limits are guaranteed by design.
Note 2: Inferred by CMRR test.
Note 3: Tested for +4.75V < V_{CC} < +5.25V, and -5.25V < V_{EE} < -4.75V with V_{DD} = +5V, although permissible analog power-supply range is 4.75V < V_{CC} < +10.5V for single supply operation with V_{EE} grounded.
Note 4: Specification does not apply to MAX9201.
Note 5: I_{CC} tested for 4.75V < V_{CC} < +10.5V with V_{EE} grounded. I_{EE} tested for -5.25V < V_{EE} < -4.75V with V_{CC} = +5V. I_{DD} tested for +4.75V < V_{DD} < +5.25V with all comparator outputs low, worst-case condition.
Note 6: Guaranteed by design. Times are for 100mV step inputs (see propagation delay characteristics in Figures 2 and 3)
Note 7: Maximum difference in propagation delay between two comparators in the MAX9201/MAX9202.

Low Cost, 7ns, Low-Power Voltage Comparators

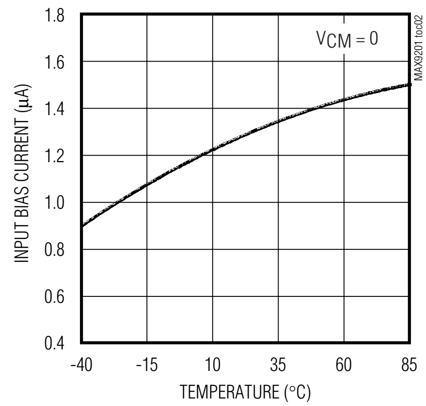
Typical Operating Characteristics

(V_{CC} = +5V, V_{EE} = -5V, V_{DD} = +5V, GND = 0, V_{CM} = 0, LATCH_ = logic high, V_{OUT} = 1.4V, T_A = +25°C, unless otherwise noted.)

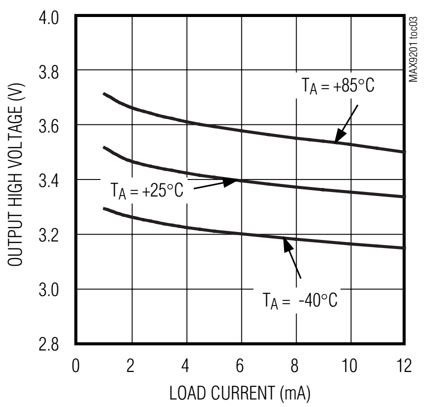
INPUT OFFSET VOLTAGE vs. TEMPERATURE



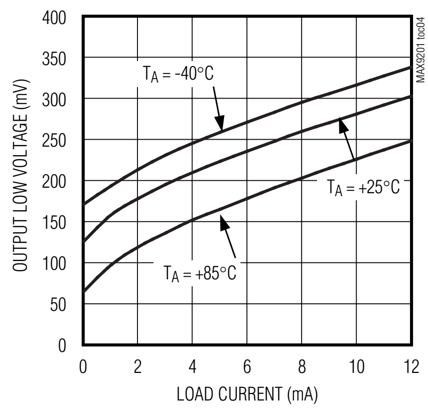
INPUT BIAS CURRENT vs. TEMPERATURE



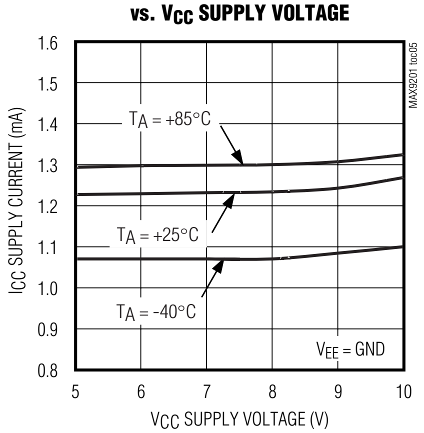
OUTPUT HIGH VOLTAGE (V_{OH}) vs. LOAD CURRENT



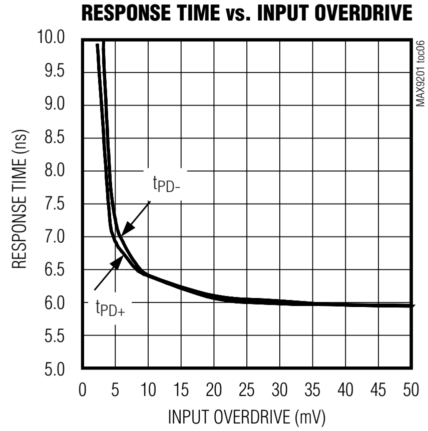
OUTPUT LOW VOLTAGE (V_{OL}) vs. LOAD CURRENT



I_{CC} SUPPLY CURRENT (PER COMPARATOR) vs. V_{CC} SUPPLY VOLTAGE

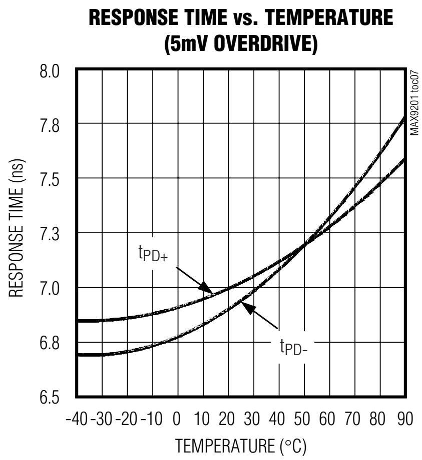


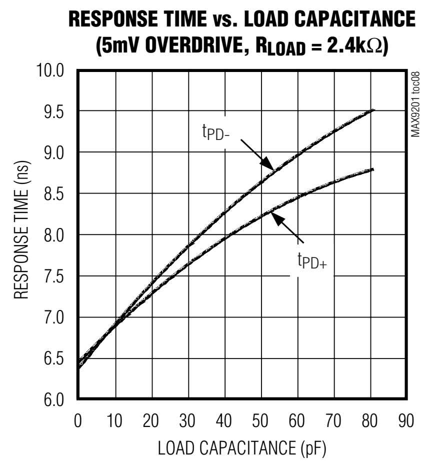
RESPONSE TIME vs. INPUT OVERDRIVE



Typical Operating Characteristics (continued)

(V_{CC} = +5V, V_{EE} = -5V, V_{DD} = +5V, GND = 0, V_{CM} = 0, LATCH_ = logic high, V_{OUT} = 1.4V, T_A = +25°C, unless otherwise noted.)





Pin Description

MAX9201

PIN	NAME	FUNCTION
1, 8, 9, 16	IN_-	Negative Input (Channels A, B, C, D)
2, 7, 10, 15	IN_+	Positive Input (Channels A, B, C, D)
3	GND	Ground
4, 5, 12, 13	OUT_	Output (Channels A, B, C, D)
6	V_{EE}	Negative Analog Supply and Substrate
11	V_{DD}	Positive Digital Supply
14	V_{CC}	Positive Analog Supply

MAX9202

PIN	NAME	FUNCTION
1, 8	IN_-	Negative Input (Channels A, B)
2, 9	IN_+	Positive Input (Channels A, B)
3	GND	Ground
4, 11	LATCH_	Latch Input (Channels A, B)
5, 12	OUT_	Output (Channels A, B)
6, 13	N.C.	No Connection
7	V_{EE}	Negative Analog Supply and Substrate
10	V_{DD}	Positive Digital Supply
14	V_{CC}	Positive Analog Supply

Low Cost, 7ns, Low-Power Voltage Comparators

Pin Description (continued)

MAX9203

PIN		NAME	FUNCTION
SO	SOT		
1	8	V_{CC}	Positive Analog Supply
2	7	IN+	Positive Input
3	6	IN-	Negative Input
4	5	V_{EE}	Negative Analog Supply and Substrate
5	4	LATCH	Latch Input
6	3	GND	Ground
7	2	OUT	Output
8	1	V_{DD}	Positive Digital Supply

Applications Information

Circuit Layout

Because of the large gain-bandwidth transfer function of the MAX9201/MAX9202/MAX9203 special precautions must be taken to realize their full high-speed capability. A printed circuit board with a good, low-inductance ground plane is mandatory. All decoupling capacitors (the small 100nF ceramic type is a good choice) should be mounted as close as possible to the power-supply pins. Separate decoupling capacitors for analog V_{CC} and for digital V_{DD} are also recommended. Close attention should be paid to the bandwidth of the decoupling and terminating components. Short lead lengths on the inputs and outputs are essential to avoid unwanted parasitic feedback around the comparators. Solder the device directly to the printed circuit board instead of using a socket.

Input Slew-Rate Requirements

As with all high-speed comparators, the high gain-bandwidth product of the MAX9201/MAX9202/ MAX9203 can create oscillation problems when the input traverses the linear region. For clean output switching without oscillation or steps in the output waveform, the input must meet minimum slew-rate requirements (0.5V/s typ). Oscillation is largely a function of board layout and of coupled source impedance and stray input capacitance. Both poor layout and large source impedance will cause the part to oscillate and increase the minimum slew-rate requirement. In some applications, it may be helpful to apply some positive feedback between the output and positive input. This pushes the output through the transition region clearly, but applies a hysteresis in threshold seen at the input terminals.

TTL Output and Latch Inputs

The comparator TTL output stages are optimized for driving low-power Schottky TTL with a fan-out of four.

When the latch is connected to a logic high level, the comparator is transparent and immediately responds to changes at the input terminals. When the latch is connected to a TTL low level, the comparator output latches (in the same state) the instant that the latch command is applied, and will not respond to subsequent changes at the input. No latch is provided on the MAX9201.

Typical Power-Supply Alternatives

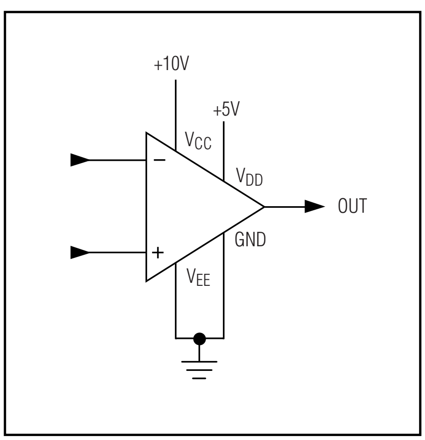


Figure 1a. Separate Analog Supply, Common Ground

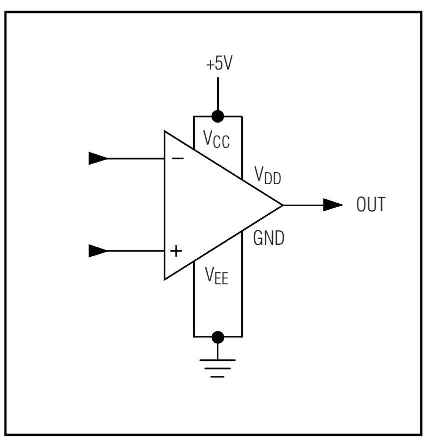


Figure 1b. Single +5V Supply, Common Ground

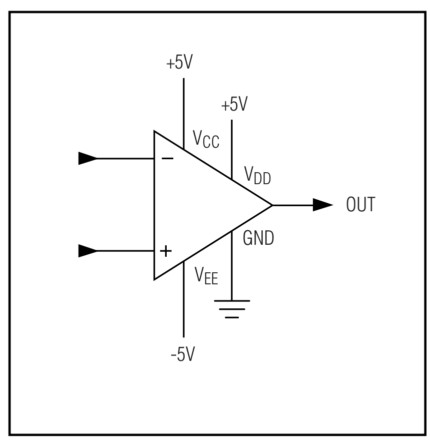


Figure 1c. Split ±5V Supply, Separate Ground

Power Supplies

The MAX9201/MAX9202/MAX9203 can be powered from separate analog and digital supplies or from a single +5V supply. The analog supply can range from +5V to +10V with V_{EE} grounded for single-supply operation (Figures 1a and 1b) or from a split ±5V supply (Figure 1c). The V_{DD} digital supply always requires +5V.

In high-speed, mixed-signal applications where a common ground is shared, a noisy digital environment can adversely affect the analog input signal. When set up with separate supplies, the MAX9201/MAX9202/MAX9203 isolate analog and digital signals by providing a separate analog ground (V_{EE}) and digital ground (GND).

Definition of Terms

V_{OS} — **Input Offset Voltage:** Voltage applied between the two input terminals to obtain TTL logic threshold (+1.4V) at the output.

V_{IN} — **Input Voltage Pulse Amplitude:** Usually set to 100mV for comparator specifications.

V_{OD} — **Input Voltage Overdrive:** Usually set to 5mV and in opposite polarity to V_{IN} for comparator specifications.

t_{pd+} — **Input to Output High Delay:** The propagation delay measured from the time the input signal crosses the input offset voltage to the TTL logic threshold (+1.4V) of an output low to high transition.

t_{pd-} — **Input to Output Low Delay:** The propagation delay measured from the time the input signal crosses the input offset voltage to the TTL logic threshold (+1.4V) of an output high to low transition.

t_{pd+} (D) — **Latch Disable to Output High Delay:** The propagation delay measured from the latch signal crossing the TTL logic threshold (+1.4V) in a low to high transition to the point of the output crossing TTL threshold (+1.4V) in a low to high transition.

tpd- (D) — **Latch Disable to Output Low Delay:** The propagation delay measured from the latch signal crossing the TTL threshold (+1.4V) in a low to high transition to the point of the output crossing TTL threshold (+1.4V) in a high to low transition.

t_s — **Minimum Setup Time:** The minimum time, before the negative transition of the latch signal, that an input signal change must be present in order to be acquired and held at the outputs.

t_h — **Minimum Hold Time:** The minimum time, after the negative transition of the latch signal, that an input signal must remain unchanged in order to be acquired and held at the output.

t_{pw} (D) — **Minimum Latch Disable Pulse Width:** The minimum time that the latch signal must remain high in order to acquire and hold an input signal change.

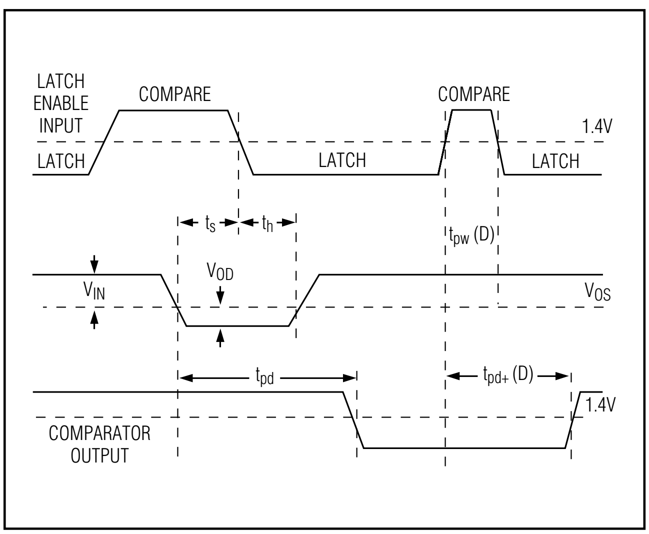


Figure 2. MAX9201/MAX9202/MAX9203 Diagram

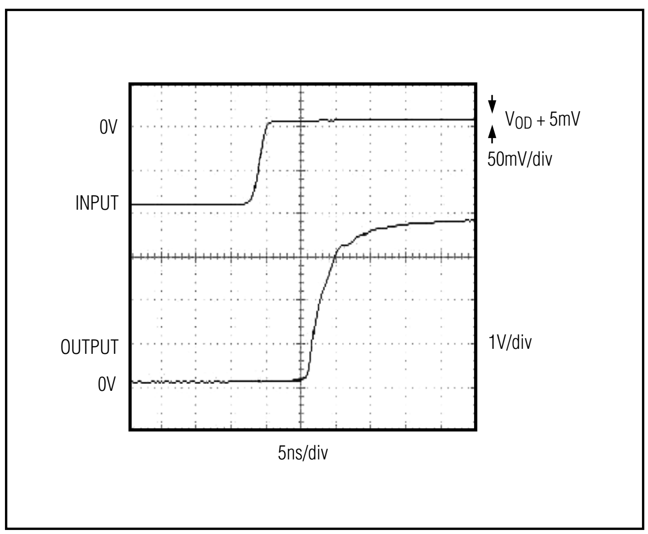


Figure 3. t_{PD+} Response Time to 5mV Overdrive

Low Cost, 7ns, Low-Power Voltage Comparators

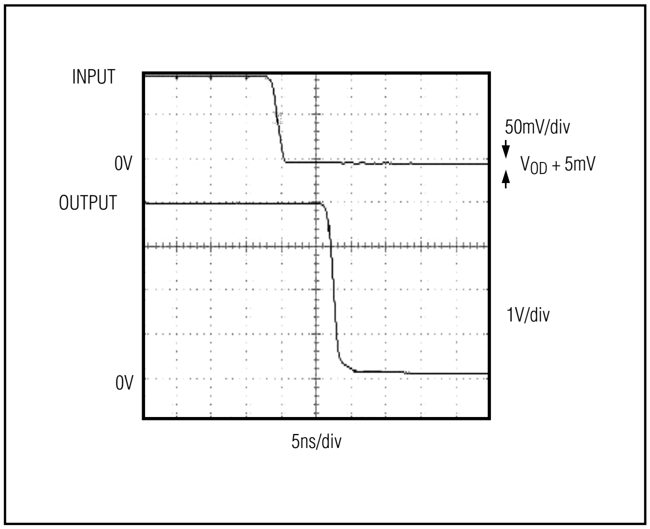


Figure 4. t_{PD-} Response Time to 5mV Overdrive

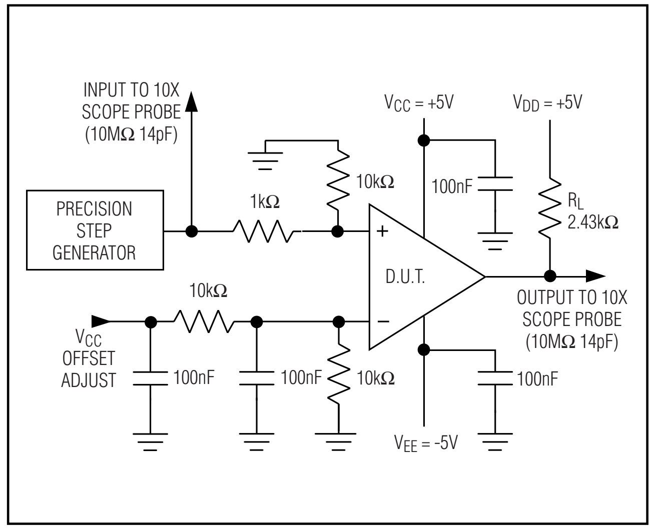


Figure 5. Response-Time Setup

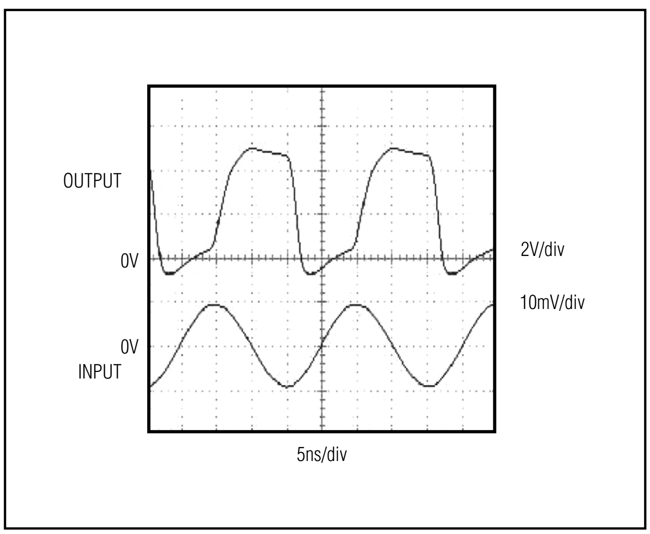


Figure 6. Response to 50MHz Sine Wave

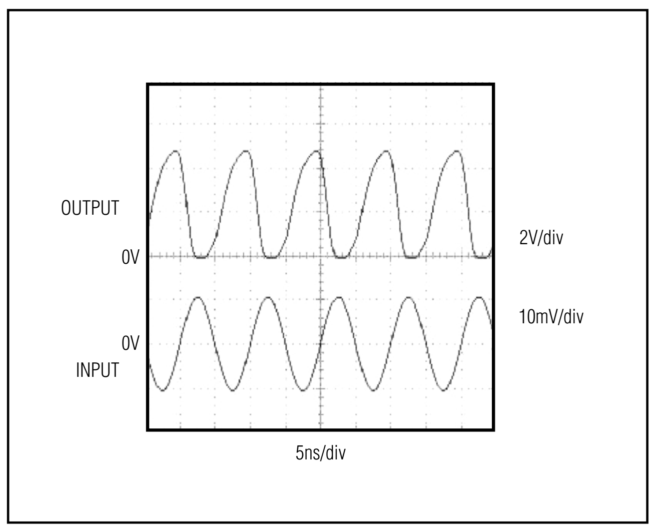


Figure 7. Response to 100MHz Sine Wave

Chip Information

MAX9201 TRANSISTOR COUNT: 348

MAX9202 TRANSISTOR COUNT: 176

MAX9203 TRANSISTOR COUNT: 116

PROCESS: Bipolar