Two-Phase Desktop CPU Core Supply Controllers with Controlled VID Change

ABSOLUTE MAXIMUM RATINGS

V_{CC} to GND .....-0.3V to +28V
V_{DD}, PWRGD, ILIM, FB to GND .....-0.3V to +6V
EN, GNDS, VPOS, REF, VID_,
TIME to GND .....0.3V to V_{VDD} + 0.3V
PGND to GND .....-0.3V to +0.3V
CS1, CS2 to GND .....-2V to +28V
VLG to GND.....-0.3V to +7V
BST1, BST2 to GND .....-0.3V to +35V
LX1 to BST1.....-7V to +0.3V
LX2 to BST2.....-7V to +0.3V
DH1 to LX1.....-0.3V to V_{BST1} + 0.3V
DH2 to LX2.....-0.3V to V_{BST2} + 0.3V
DL1, DL2 to PGND .....-0.3V to V_{VLG} + 0.3V
Continuous Power Dissipation (T_A = +70°C)
28-Pin QSOP (derate 20.8mW/°C above +70°C).....860.2mW
Operating Temperature Range .....-40°C to +85°C
Junction Temperature.....+150°C
Storage Temperature Range .....-65°C to +150°C
Lead Temperature (soldering, 10s) .....+300°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

(V_{CC} = 12V, V_{EN} = V_{VDD} = 5V, PGND = GNDS = GND = 0, VID_ = GND, C_{VPOS} = 47pF, C_{REF} = 0.1µF, V_{ILIM} = 1V, **T_A = 0°C to +85°C**, unless otherwise noted. Typical values are at T_A = +25°C.)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
GENERAL					
V_{CC} Operating Range	MAX1937	6		24	V
	MAX1938/MAX1939	8		24	
V_{DD} Operating Range		4.5	5	5.5	V
VLG Operating Range	V_{VLG} > V_{VDD}	4.5		6.5	V
V_{CC} Operating Supply Current	FB above threshold (no switching)		20	40	µA
V_{DD} Operating Supply Current	FB above threshold (no switching)		1.4	2.5	mA
VLG Operating Supply Current	FB above threshold (no switching)	20		60	µA
V_{CC} Shutdown Current	EN = GND		<1	5	µA
V_{DD} Shutdown Current	EN = GND, VID_ not connected		50	100	µA
VLG Shutdown Current	EN = GND		<1	5	µA
TIME Output Voltage		1.96	2.00	2.04	V
ILIM Input Bias	V_{ILIM} = 1.5V	-250		+250	nA
VPOS Output Voltage	CS_= GND, VPOS connected to REF through a 75kΩ resistor	1.96	2.0	2.04	V
REFERENCE					
Reference Voltage	-50µA ≤ I_{REF} ≤ 50µA	1.987	2.000	2.013	V
SOFT-START					
Ramp Period	MAX1937	1.1		5.5	ms
	MAX1938	1.5		6.2	
	MAX1939	1.3		6.5	
Soft-Start Voltage Step			25		mV
ERROR AMPLIFIER					
FB Input Resistance	Resistance from FB to GND		180		kΩ
GNDS Input Bias Current		-5		+5	µA
Output Regulation Voltage Accuracy		-0.75		+0.75	%

ELECTRICAL CHARACTERISTICS (continued)

(V_{CC} = 12V, V_{EN} = V_{VDD} = 5V, PGND = GNDS = GND = 0, VID_ = GND, C_{VPOS} = 47pF, C_{REF} = 0.1µF, V_{ILIM} = 1V, **T_A = 0°C to +85°C**, unless otherwise noted. Typical values are at T_A = +25°C.)

PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
FAULT PROTECTION						
V_{DD} Undervoltage Lockout (UVLO) Threshold	Rising or falling V_{DD}		4.00	4.25	4.45	V
V_{DD} UVLO Hysteresis				80		mV
VLG UVLO Threshold	Rising or falling VLG		4.00	4.25	4.45	V
VLG UVLO Hysteresis				40		mV
Thermal Shutdown	Rising temperature, typical hysteresis = 15°C			160		°C
Reference UVLO Threshold	Rising edge			1.600		V
	Falling edge			1.584		
Output Overvoltage Fault Threshold	Rising and falling	MAX1937/MAX1938	1.97	2.00	2.03	V
		MAX1939	2.215	2.250	2.285	
Output UVLO Threshold	Rising and falling percentage of the nominal regulation voltage		65	70	75	%
CURRENT LIMIT						
Current-Limit Threshold	PGND to CS_, V_{ILIM} = 1.5V		135	150	165	mV
	PGND to CS_, V_{ILIM} = 1V		90	100	110	
	PGND to CS_, V_{ILIM} = 0.5V		45	50	55	
CS Input Offset Voltage	CS_ = GND		-3		+3	mV
CS_ Input Bias Current	CS_ = GND		-5		+5	µA
VOLTAGE POSITIONING						
VPOS Input Offset Voltage			-3		+3	mV
VPOS Gain	From CS_ to FB; V_{CS1}, V_{CS2} = 0, -100mV; R_{VPOS} = 75kΩ		72.5	75.0	77.5	%/V
VPOS Gain	From CS1, CS2 to FB; V_{CS1}, V_{CS2} = +13mV, -113mV; R_{VPOS} = 75kΩ		68	75	82	%/V
TIMER AND DRIVERS						
On-Time	LX1 = LX2 = CS1 = CS2 = GND, V_{FB} = 1.5V		420	525	630	ns
Minimum Off-Time	DH1 low to DH2 high, and DH2 low to DH1 high		260	325	390	ns
Break-Before-Make Time	DH_ low to DL_ high	MAX1937/MAX1938		60		ns
		MAX1939		60		
	DL_ low to DH_ high	MAX1937/MAX1938		85		
		MAX1939		70		

Two-Phase Desktop CPU Core Supply Controllers with Controlled VID Change

ELECTRICAL CHARACTERISTICS (continued)

(V_{CC} = 12V, V_{EN} = V_{VDD} = 5V, PGND = GNDS = GND = 0, VID_ = GND, C_{VPOS} = 47pF, C_{REF} = 0.1µF, V_{ILIM} = 1V, **T_A = 0°C to +85°C**, unless otherwise noted. Typical values are at T_A = +25°C.)

PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
DH_ On-Resistance in Low State	V_{BST1} = V_{BST2} = 6V, LX1 = LX2 = GND			1.5	3.0	Ω
DH_ On-Resistance in High State	$V_{BST\_}$ = 6V, LX_ = GND			1.5	3.0	Ω
DL_ On-Resistance in Low State				0.5	1.7	Ω
DL_ On-Resistance in High State				1.5	3.0	Ω
BST_ Leakage Current	$V_{BST\_}$ = 30V, $V_{LX\_}$ = 24V				50	µA
LX_ Leakage Current	$V_{BST\_}$ = 30V, $V_{LX\_}$ = 24V				50	µA
EN AND VID						
Low Level Threshold					0.8	V
High Level Threshold			1.6			V
Pullup Resistance	Internally pulled up to V_{DD}		50	100	200	kΩ
PWRGD						
PWRGD Upper Trip Level			10.0	12.5	15.0	%
PWRGD Lower Trip Level			-15	-12.5	-10	%
Output Low Level					0.4	V
Output High Leakage					1	µA
CONTROLLED VID CHANGE						
On-the-Fly VID Change Slew Rate	25mV per step	R_{TIME} = 120kΩ	6.17	6.67	7.25	µs
		R_{TIME} = 47kΩ	2.35	2.63	2.99	
		R_{TIME} = 470kΩ	23.5	26.3	29.9	
VID_ Change Frequency Range			38		380	kHz
PWRGD Blanking Time	V_{VDD} = 4.5V to 5.5V		125	200	350	µs

ELECTRICAL CHARACTERISTICS

(V_{VCC} = 12V, V_{EN} = V_{VDD} = 5V, PGND = GNDS = GND, VID_= GND, C_{VPOS} = 47pF, C_{REF} = 0.1µF, V_{ILIM} = 1V, **T_A = -40°C to +85°C**, unless otherwise noted.) (Note 1)

PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
GENERAL						
V_{CC} Operating Range	MAX1937		6		24	V
	MAX1938/MAX1939		8		24	
V_{DD} Operating Range			4.5		5.5	V
VLG Operating Range	$V_{VLG} \geq V_{VDD}$		4.5		6.5	V
V_{CC} Operating Supply Current	FB above threshold (no switching)				40	µA
V_{DD} Operating Supply Current	FB above threshold (no switching)				2.5	mA
VLG Operating Supply Current	FB above threshold (no switching)		20		60	µA
V_{CC} Shutdown Current	EN = GND				5	µA
V_{DD} Shutdown Current	EN = GND, VID_ not connected				100	µA
VLG Shutdown Current	EN = GND				5	µA
TIME Output Voltage			1.96		2.04	V
ILIM Input Bias	V_{ILIM} = 1V		-250		+250	nA
VPOS Output Voltage	CS_ = GND, VPOS connected to REF through a 75kΩ resistor		1.96		2.04	V
REFERENCE						
Reference Voltage	-50µA ≤ I_{REF} ≤ 50µA		1.98		2.02	V
SOFT-START						
Ramp Period	MAX1937		1.1		5.5	ms
	MAX1938		1.5		6.6	
	MAX1939		1.3		7.0	
ERROR AMPLIFIER						
GNDS Input Bias Current			-5		+5	µA
Output Regulation Voltage Accuracy			-1		+1	%
FAULT PROTECTION						
V_{DD} UVLO Threshold	Rising or falling V_{DD}		4.00		4.45	V
VLG UVLO Threshold	Rising or falling VLG		4.00		4.45	V
Output Overvoltage Fault Threshold	Rising and falling	MAX1937/MAX1938	1.97		2.03	V
		MAX1939	2.215		2.285	
Output UVLO Threshold	Rising and falling percentage of the nominal regulation voltage		65		75	%
CURRENT LIMIT						
Current-Limit Threshold	PGND to CS_, V_{ILIM} = 1.5V		135		165	mV
	PGND to CS_, V_{ILIM} = 1V		90		110	
	PGND to CS_, V_{ILIM} = 0.5V		45		55	

Two-Phase Desktop CPU Core Supply Controllers with Controlled VID Change

ELECTRICAL CHARACTERISTICS (continued)

(V_{VCC} = 12V, V_{EN} = V_{VDD} = 5V, PGND = GNDS = GND, VID_= GND, C_{VPOS} = 47pF, C_{REF} = 0.1µF, V_{ILIM} = 1V, **T_A = -40°C to +85°C**, unless otherwise noted.) (Note 1)

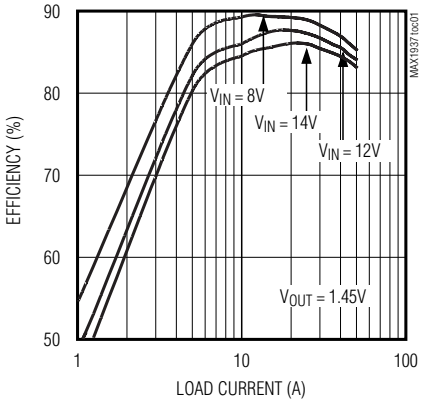
PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
CS Input Offset Voltage	CS_ = GND		-5		+5	mV
CS_ Input Bias Current	CS_ = GND		-5		+5	µA
VOLTAGE POSITIONING						
VPOS Input Offset Voltage			-5		+5	mV
VPOS Gain	From CS_ to FB; V_{CS1}, V_{CS2} = 0, -100mV; R_{VPOS} = 75kΩ		72.5		77.5	%/V
VPOS Gain	From CS1, CS2 to FB; V_{CS1}, V_{CS2} = +13mV, -113mV; R_{VPOS} = 75kΩ		68		82	%/V
TIMER AND DRIVERS						
On-Time	LX1 = LX2 = CS1 = CS2 = GND, V_{FB} = 1.5V		420		630	ns
Minimum Off-Time	DH1 low to DH2 high, and DH2 low to DH1 high		260		390	ns
DH_ On-Resistance in Low State	V_{BST1} = V_{BST2} = 6V, LX1 = LX2 = GND				3	Ω
DH_ On-Resistance in High State	$V_{BST\_}$ = 6V, LX_ = GND				3	Ω
DL_ On-Resistance in Low State					1.7	Ω
DL_ On-Resistance in High State					3	Ω
BST_ Leakage Current	$V_{BST\_}$ = 30V, $V_{LX\_}$ = 24V				50	µA
LX_ Leakage Current	$V_{BST\_}$ = 30V, $V_{LX\_}$ = 24V				50	µA
EN AND VID_						
Low Level Threshold					0.8	V
High Level Threshold			1.6			V
Pullup Resistance	Internally pulled up to V_{DD}		50		200	kΩ
PWRGD						
PWRGD Upper Trip Level			10		15	%
PWRGD Lower Trip Level			-15		-10	%
Output Low Level					0.4	V
Output High Leakage					1	µA
CONTROLLED VID CHANGE						
On-the-Fly VID Change Slew Rate	25mV per step	R_{TIME} = 120kΩ	6.17		7.25	µs
		R_{TIME} = 47kΩ	2.35		2.99	
		R_{TIME} = 470kΩ	23.5		29.9	
VID_ Change Frequency Range			38		380	kHz
PWRGD Blanking Time	V_{VDD} = 4.5V to 5.5V		125		350	µs

Note 1: Specifications to -40°C are guaranteed by design and not production tested.

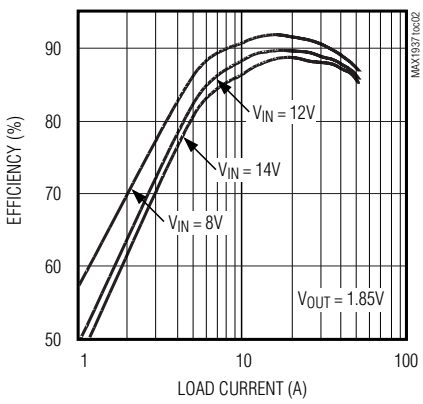
Typical Operating Characteristics

(V_{IN} = 12V, V_{OUT} = 1.45V, T_A = +25°C, unless otherwise noted.)

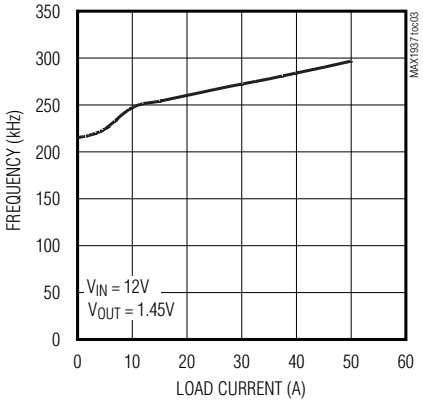
EFFICIENCY vs. LOAD CURRENT AT 1.45V OUTPUT



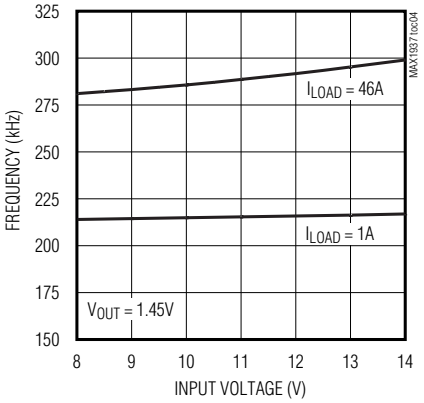
EFFICIENCY vs. LOAD CURRENT AT 1.85V OUTPUT



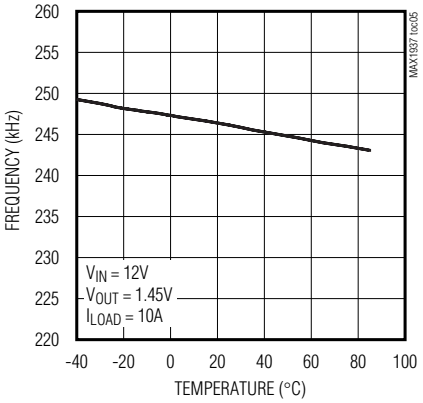
FREQUENCY vs. LOAD CURRENT



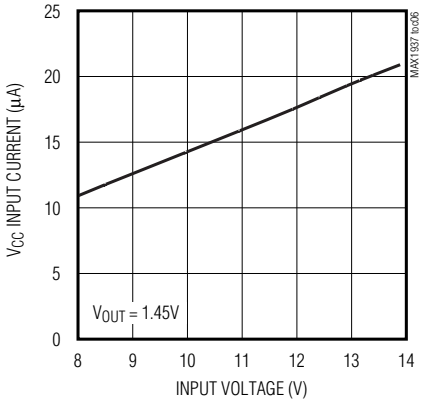
FREQUENCY vs. INPUT VOLTAGE



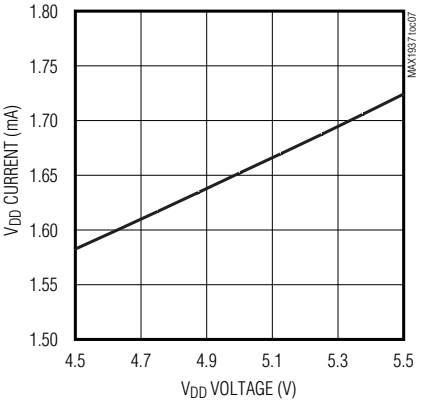
FREQUENCY vs. TEMPERATURE



VCC INPUT CURRENT vs. INPUT VOLTAGE



VDD CURRENT vs. VDD VOLTAGE

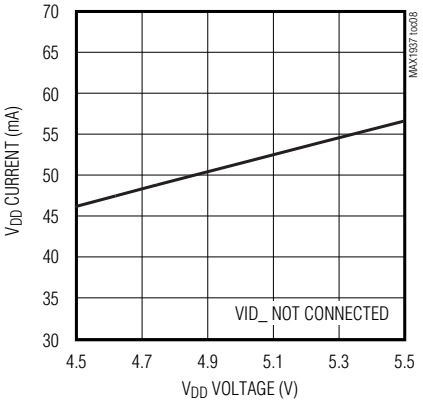


Two-Phase Desktop CPU Core Supply Controllers with Controlled VID Change

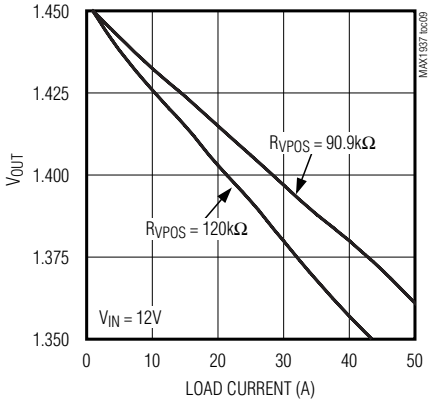
Typical Operating Characteristics (continued)

(V_{IN} = 12V, V_{OUT} = 1.45V, T_A = +25°C, unless otherwise noted.)

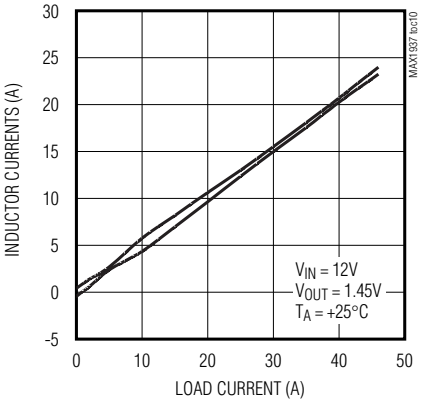
V_{DD} CURRENT vs. V_{DD} VOLTAGE IN SHUTDOWN



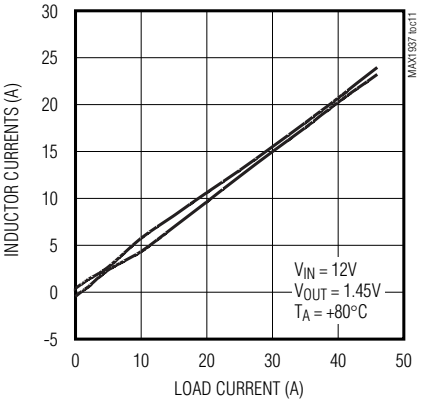
OUTPUT VOLTAGE vs. LOAD CURRENT AT 1.45V OUTPUT



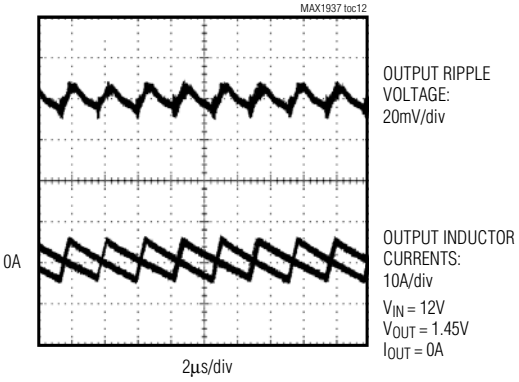
CURRENT SHARING



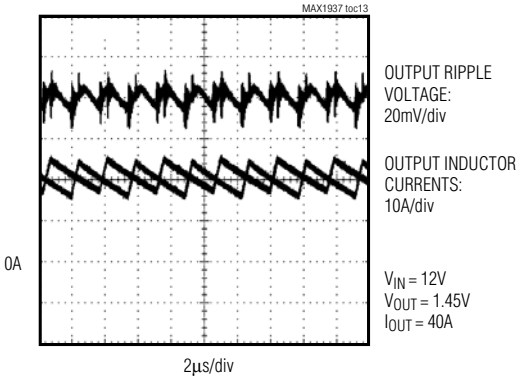
CURRENT SHARING



INDUCTOR CURRENT WAVEFORMS WITH 0A LOAD



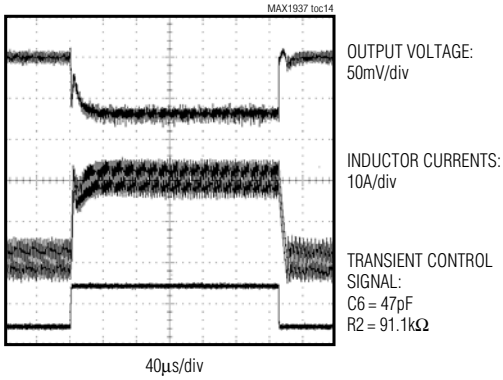
INDUCTOR CURRENT WAVEFORMS WITH 40A LOAD



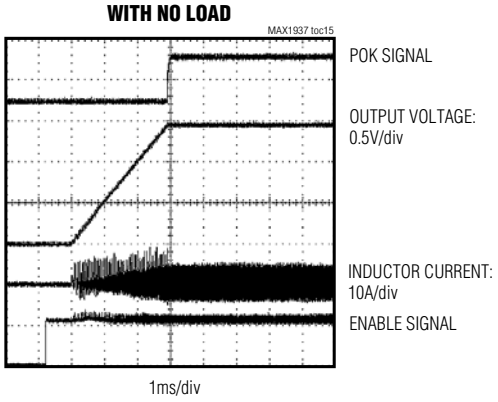
Typical Operating Characteristics (continued)

(V_{IN} = 12V, V_{OUT} = 1.45V, T_A = +25°C, unless otherwise noted.)

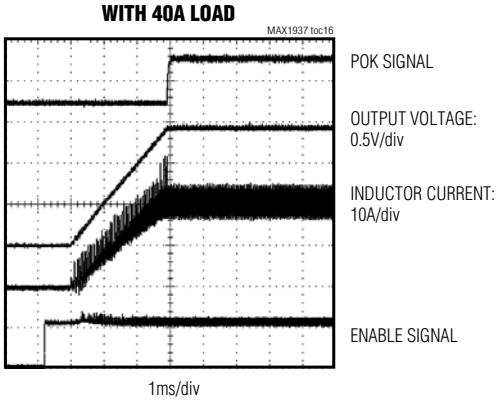
LOAD TRANSIENT 1A TO 40A TO 1A



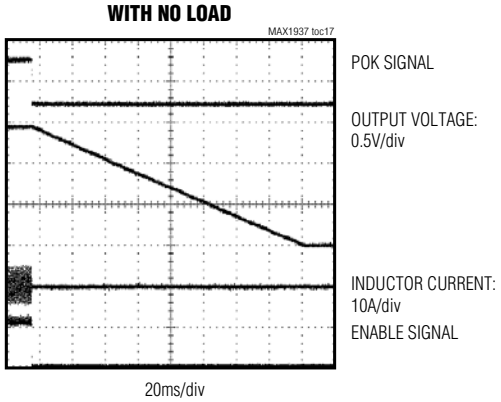
SOFT-START WAVEFORMS WITH NO LOAD



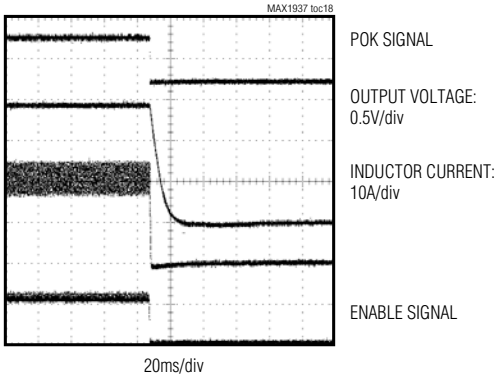
SOFT-START WAVEFORMS WITH 40A LOAD



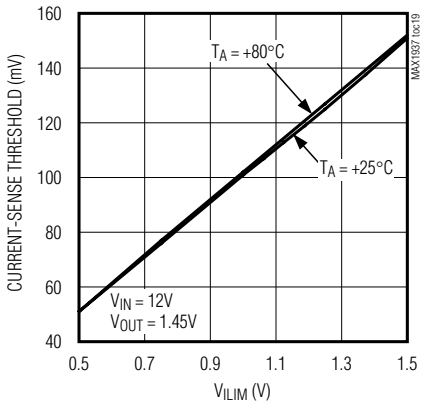
SHUTDOWN WAVEFORM WITH NO LOAD



SHUTDOWN WAVEFORM WITH 40A LOAD



CURRENT-SENSE THRESHOLD vs. V_{ILIM}

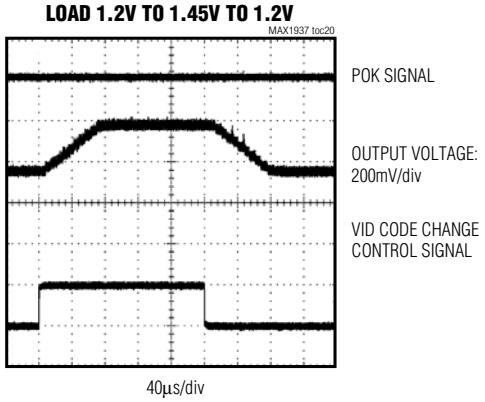


Two-Phase Desktop CPU Core Supply Controllers with Controlled VID Change

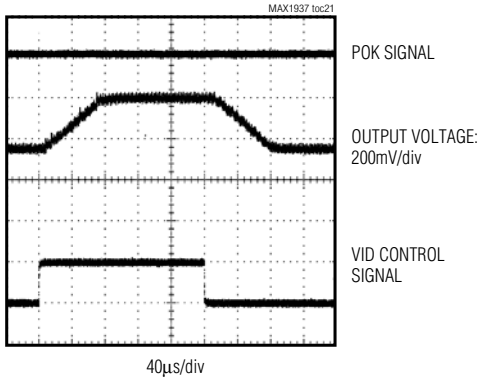
Typical Operating Characteristics (continued)

(V_{IN} = 12V, V_{OUT} = 1.45V, T_A = +25°C, unless otherwise noted.)

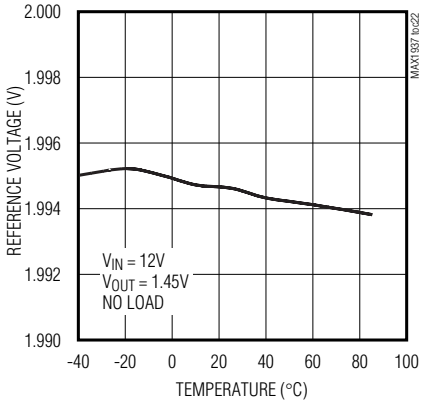
VID CODE CHANGE ON-THE-FLY WITH 40A LOAD 1.2V TO 1.45V TO 1.2V



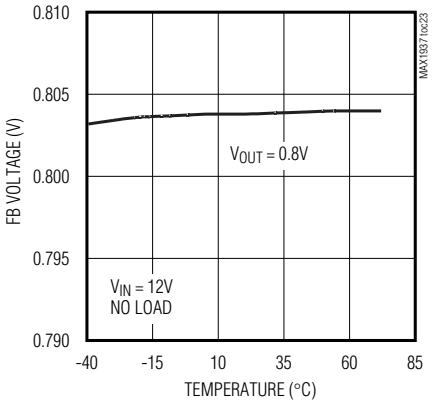
VID CODE CHANGE ON-THE-FLY WITH 1A LOAD 1.2V TO 1.45V TO 1.2V



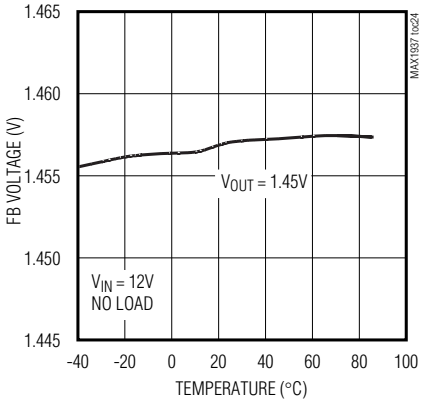
REFERENCE VOLTAGE vs. TEMPERATURE



FB VOLTAGE vs. TEMPERATURE



FB VOLTAGE vs. TEMPERATURE



Pin Description

PIN	NAME	FUNCTION
1	VID0	Voltage Identification Input Bit 0. See Table 1. Internal 100kΩ pullup resistor to V_{DD}.
2	VID1	Voltage Identification Input Bit 1. See Table 1. Internal 100kΩ pullup resistor to V_{DD}.
3	TIME	Connect to an external resistor (47kΩ to 470kΩ) for VID change slew-rate control.
4	VID2	Voltage Identification Input Bit 2. See Table 1. Internal 100kΩ pullup resistor to V_{DD}.
5	VID3	Voltage Identification Input Bit 3. See Table 1. Internal 100kΩ pullup resistor to V_{DD}.
6	VID4	Voltage Identification Input Bit 4. See Table 1. Internal 100kΩ pullup resistor to V_{DD}.
7	VPOS	Voltage Positioning. Connect a resistor between VPOS and REF to set the output voltage-positioning droop, or connect directly to REF for no output voltage positioning. Connect a 47pF capacitor from VPOS to GND.
8	V_{DD}	IC Analog Power-Supply Input. Connect a 5V supply to V_{DD}.
9	ILIM	Current-Limit Threshold per Phase. Connect ILIM to V_{DD} to set a default current limit of 120mV, or connect to a voltage-divider from REF to GND to adjust the current limit. See the *Setting the Current Limit* section.
10	GND	Ground
11	GNDS	Remote Ground Sense. Connect GNDS to the output ground at the load. For VRM applications, also connect a 100Ω resistor from GNDS to PGND locally.
12	REF	Reference Output. Connect a 0.1µF capacitor from REF to GND.
13	EN	Enable Input. Leave unconnected or drive high for normal operation. Drive low for shutdown.
14	FB	Remote Feedback Sense. Connect FB to the output at the load. For VRM applications, also connect a 100Ω resistor from FB to the output locally.
15	PWRGD	Power-Good Output. Open-drain output is high impedance when the output is in regulation and pulled low when the output deviates more than 12.5% from the voltage set by the VID code. PWRGD is also low in shutdown or during any fault condition. To use as a logic output, connect a pullup resistor from PWRGD to the logic supply.
16	BST2	High-Side MOSFET Gate-Driver Bootstrap Input. Connect 0.22µF or higher value bypass capacitor from BST2 to LX2. Keep trace length as short as possible. Connect a Schottky diode between BST2 and VLG. See the *Selecting a BST Capacitor* section.
17	DH2	High-Side MOSFET Gate-Drive Output. Connect to the high-side MOSFET gate. DH2 is pulled low in shutdown.
18	LX2	Inductor Connection. Connect to the switched side of the inductor.
19	CS2	Negative Current-Sense Input. Connect to a current-sense resistor in series with the low-side MOSFET, or connect to LX2 to use the low-side MOSFET's on-resistance for current sensing.
20	DL2	Low-Side MOSFET Gate-Driver Output. Connect to the low-side MOSFET gate. DL2 is pulled low in shutdown.
21	PGND	Power Ground. Connect to power ground at the point where the current-sense resistors or low-side MOSFET sources connect. PGND is used as the positive current-sense connection.

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Pin Description (continued)

PIN	NAME	FUNCTION
22	VLG	DL_ Driver Power-Supply Input. Connect to a 4.5V to 6.5V supply for powering the low-side MOSFET gate drive, and the bootstrap circuit for driving the high-side MOSFETs. Ensure that V_{VLG} is greater than or equal to V_{VDD}.
23	DL1	Low-Side MOSFET Gate-Driver Output. Connect to the low-side MOSFET gate. DL1 is pulled low in shutdown.
24	CS1	Negative Current-Sense Input. Connect to a current-sense resistor in series with the low-side MOSFET or connect to LX1 to use the low-side MOSFET's on-resistance for current sensing.
25	LX1	Inductor Connection. Connect to the switched side of the inductor.
26	DH1	High-Side MOSFET Gate-Drive Output. Connect to the high-side MOSFET gate. DH1 is pulled low in shutdown.
27	BST1	High-Side MOSFET Gate-Driver Bootstrap Input. Connect 0.22µF or higher value bypass capacitor from BST1 to LX1. Keep trace length as short as possible. Connect a Schottky diode between BST1 and VLG. See the *Selecting a BST Capacitor* section.
28	V_{CC}	Input Voltage Sense. Connect to the input supply at the high-side MOSFET drain. The voltage sensed at V_{CC} is used to set the on-time.

Detailed Description

The MAX1937/MAX1938/MAX1939 is a family of synchronous, two-phase step-down controllers capable of delivering load currents up to 60A. The controllers use Quick-PWM control architecture in conjunction with active load current voltage positioning. Quick-PWM control provides instantaneous load-step response, while programmable voltage positioning allows the converter to utilize full transient regulation limits, reducing the output capacitance requirement. Furthermore, the two phases operate 180° out-of-phase with an effective 500kHz switching frequency, thus reducing input and output current ripple, as well as reducing input filter capacitor requirements.

The MAX1937/MAX1938/MAX1939 are compliant with the AMD Hammer, Intel VRM 9.0/VRM 9.1, and AMD Athlon Mobile VID code specifications (see Table 1 for VID codes). The internal DAC provides ultra-high accuracy of ±0.75%. A controlled VID voltage transition is implemented to minimize both undervoltage and overvoltage overshoot during VID input change.

Remote sensing is available for high output-voltage accuracy. The MOSFET switches are driven by with a 6V gate-drive circuit to minimize switching and crossover conduction losses to achieve efficiency as high as 90%. The MAX1937/MAX1938/ MAX1939 feature cycle-by-cycle current limit to ensure current limit is not exceeded. Crowbar protection is available to protect against output overvoltage.

On-Time One-Shot

The heart of the Quick-PWM core is the one-shot that sets the high-side switch on-time. This fast, low-jitter, one-shot circuitry varies the on-time in response to the input and output voltages. The high-side switch on-time is inversely proportional to the voltage applied to V_{CC} and directly proportional to the output voltage. This algorithm results in a nearly constant switching frequency, despite the lack of a fixed-frequency clock generator. The benefits of a constant switching frequency are twofold: the frequency selected avoids noise-sensitive regions, and the inductor ripple current operating point remains relatively constant, resulting in easy design methodology and predictable output voltage ripple:

$$t_{ON} = \frac{K\left(V_{OUT} + V_{DROP}\right)}{V_{VCC}}$$

where the constant K is 4µs and V_{DROP} is the voltage drop across the low-side MOSFET's on-resistance plus the drop across the current-sense resistor ($V_{DROP} \approx$ 75mV), if used.

The on-time one-shot has good accuracy at the operating point specified in the *Electrical Characteristics*. On-times at operating points far removed from the conditions specified in the *Electrical Characteristics* can vary over a wide range. For example, the regulators run slower with input voltages greater than 12V because of the very short on-times required.

Table 1. VID Programmed Output Voltage

VID4	VID3	VID2	VID1	VID0	V_{OUT} (V)		
					MAX1937	MAX1938	MAX1939
0	0	0	0	0	1.550	1.850	2.000
0	0	0	0	1	1.525	1.825	1.950
0	0	0	1	0	1.500	1.800	1.900
0	0	0	1	1	1.475	1.775	1.850
0	0	1	0	0	1.450	1.750	1.800
0	0	1	0	1	1.425	1.725	1.750
0	0	1	1	0	1.400	1.700	1.700
0	0	1	1	1	1.375	1.675	1.650
0	1	0	0	0	1.350	1.650	1.600
0	1	0	0	1	1.325	1.625	1.550
0	1	0	1	0	1.300	1.600	1.500
0	1	0	1	1	1.275	1.575	1.450
0	1	1	0	0	1.250	1.550	1.400
0	1	1	0	1	1.225	1.525	1.350
0	1	1	1	0	1.200	1.500	1.300
0	1	1	1	1	1.175	1.475	Shutdown
1	0	0	0	0	1.150	1.450	1.275
1	0	0	0	1	1.125	1.425	1.250
1	0	0	1	0	1.100	1.400	1.225
1	0	0	1	1	1.075	1.375	1.200
1	0	1	0	0	1.050	1.350	1.175
1	0	1	0	1	1.025	1.325	1.150
1	0	1	1	0	1.000	1.300	1.125
1	0	1	1	1	0.975	1.275	1.100
1	1	0	0	0	0.950	1.250	1.075
1	1	0	0	1	0.925	1.225	1.050
1	1	0	1	0	0.900	1.200	1.025
1	1	0	1	1	0.875	1.175	1.000
1	1	1	0	0	0.850	1.150	0.975
1	1	1	0	1	0.825	1.125	0.950
1	1	1	1	0	0.800	1.100	0.925
1	1	1	1	1	Shutdown	Shutdown	Shutdown

Note: *In the above table, a zero indicates the VID_ pin is connected to GND or driven low, indicates the VID_ pin is driven high or not connected.*

While the on-time is set by the input and output voltage, other factors contribute to the switching frequency. The on-time guaranteed in the *Electrical Characteristics* is influenced by switching delays in the external high-side MOSFET. Resistive losses in the inductor, both MOSFETs, output capacitor ESR, and PC board copper losses in the output and ground, tend to raise the switching frequency at higher output currents. Switch dead-time can also increase the effective on-time, reducing the switching frequency. This effect occurs when the inductor current reverses at light or negative load currents. With reversed inductor current, the inductor's

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EMF causes LX to go high earlier than normal, extending the on-time by a period equal to the DH rising dead-time.

When the controller operates in continuous mode, the dead-time is no longer a factor, and the actual switching frequency is:

$$f_{SW} = \frac{V_{OUT} + V_{DROP1}}{t_{ON}(V_{VCC} + V_{DROP1} - V_{DROP2})}$$

where V_{DROP1} is the sum of the parasitic voltage drops in the inductor discharge path, including the synchronous rectifier, inductor, and PC board resistances; V_{DROP2} is the sum of the resistances in the charging path, including the high-side MOSFET, inductor, and PC board resistances.

Synchronized 2-Phase Operation

The two phases of the MAX1937/MAX1938/MAX1939 operate 180° out-of-phase to reduce input filtering requirements, reduce electromagnetic interference (EMI), and improve efficiency. This effectively lowers cost and saves board space, making the MAX1937/MAX1938/MAX1939 ideal for cost-sensitive applications.

With dual synchronized out-of-phase operation, the MAX1937/MAX1938/MAX1939s' high-side MOSFETs turn on 180° out-of-phase. The instantaneous input current peaks of both regulators do not overlap, resulting in reduced input voltage ripple and RMS ripple current. This reduces the input capacitance requirement, allowing fewer or less expensive capacitors, and reduces shielding requirements for EMI. The 180° out-of-phase waveforms are shown in the *Typical Operating Characteristics.*

Each phase operates with a 250kHz switching frequency. Since the two regulators operate 180° out-of-phase, an effective switching of 500kHz is seen at the input and output. In addition to being at a higher frequency (compared to a single-phase regulator), both the input and output ripple have lower amplitude.

Phase Overlap

To minimize the crosstalk noise in the two phases, the maximum duty cycle of the MAX1937/MAX1938/MAX1939 is less than 50%. To provide a fast transient response, these devices have a phase-overlap mode that allows the two phases to operate in phase when a heavy-load transient is detected. In-phase operation continues until the output voltage returns to the nominal output voltage regulation value.

Once regulation is achieved, the controller returns to 180° out-of-phase operation. A minimum current-adaptive phase-selection algorithm is used to determine which phase is used to start the first out-of-phase cycle. Once the output voltage returns to the nominal output voltage regulation value, the subsequent cycle starts with the phase that has the lowest inductor current. For example, if the current-sense inputs indicate that phase 2 has lower inductor current than phase 1, the controller turns on phase 2's high-side MOSFET first when returning to normal operation.

Differential Voltage Sensing and Error Comparator

The MAX1937/MAX1938/MAX1939 use differential sensing of the output voltage to achieve the highest possible accuracy of the output voltage. This allows the error comparator to sense the actual voltage at the load, so that the controller can compensate for losses in the power output and ground lines.

FB and GNDS are used for the differential output voltage sensing. The controller triggers the next cycle (turn on the high-side MOSFET) when the error comparator is low (V_{FB} - V_{GNDS} is less than the VID regulation voltage), V_{CS} is below the current-limit threshold, and the minimum off-time one-shot has timed out.

Traces from FB and GNDS should be routed close to each other and as far away as possible from sources of noise (such as the inductors and high di/dt traces). If noise on these connections cannot be prevented, then use RC filters. To filter FB, connect a 100Ω series resistor from the positive sense trace to FB, and connect a 1000pF capacitor from FB to GND right at the FB pin. For GNDS, connect a 100Ω series resistor from the negative sense trace to GNDS, and connect a 1000pF capacitor from GNDS to GND at the GNDS pin.

For VRM applications, connect a 10kΩ resistor from FB to the output locally (on the VRM board), and connect a 10kΩ resistor from GNDS to PGND locally (on the VRM board). FB and GNDS also connect to the output at the load (off the VRM board, at the microprocessor). This provides the benefits of differential output voltage sensing mentioned above and the safety of regulating the output voltage on the board in case the external sense connections get disconnected.

External Linear Regulator

A 6V linear regulator (U2) is used to step down the main supply. The output of this linear regulator is connected to VLG to provide power for the low-side gate drive and bootstrap circuit. Using 6V for this supply improves efficiency by providing a stronger gate drive than a 5V supply. To reduce switching noise on VLG,

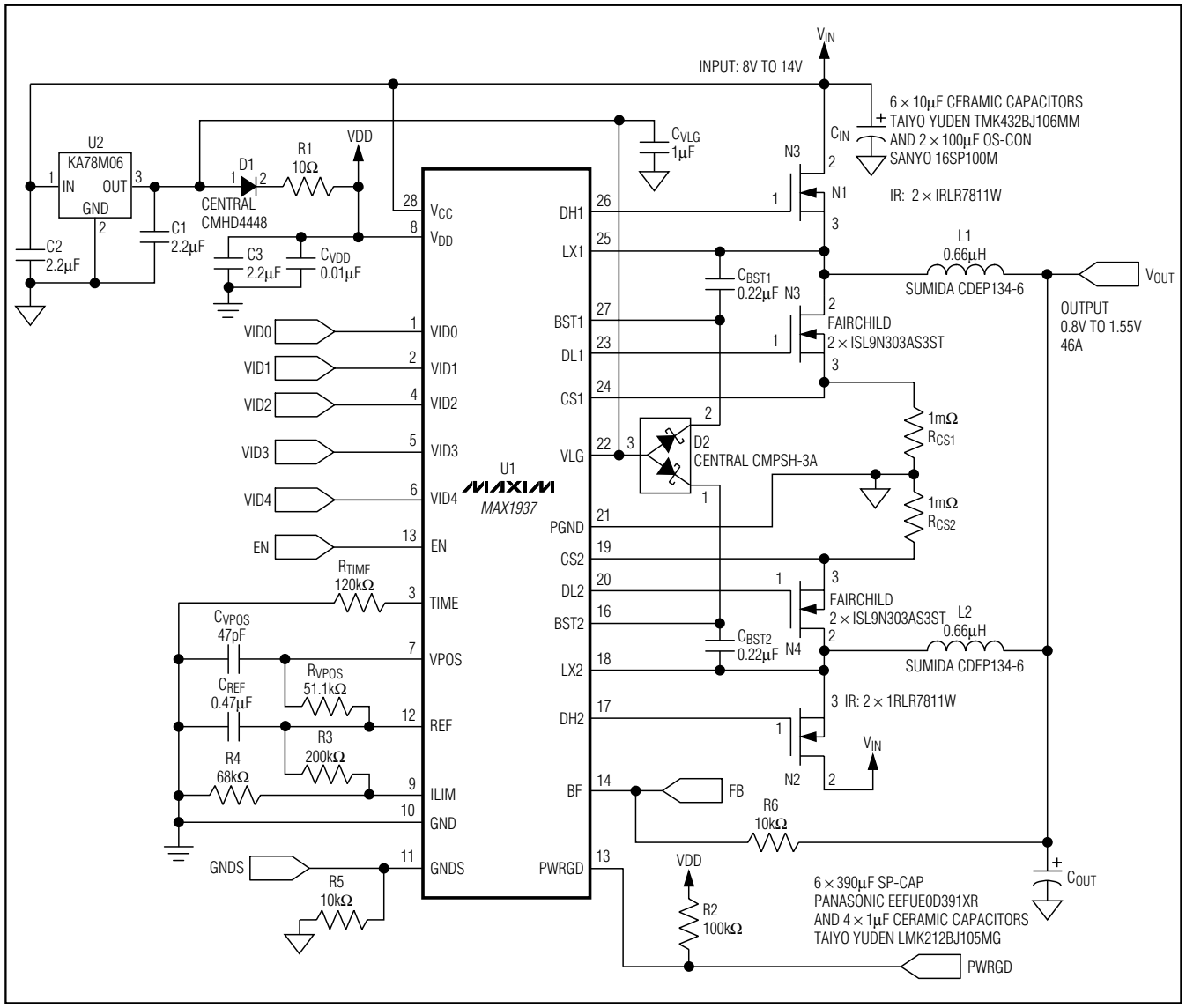

Figure 1. MAX1937 Application Circuit

connect a capacitor (C_{VLG}) from VLG to PGND. Place this capacitor as close as possible to the VLG pin.

The MAX1937/MAX1938/MAX1939 also require an external 5V supply connected to V_{DD}. A diode with a forward voltage drop of about 1V (D1) is used to stepdown the 6V supply to power the IC, as shown in Figure 1. The diode connects between the linear regulator output and the RC filter used to filter the voltage at V_{DD} (R1, C_{VDD}, and C3). In the PC board layout, place C_{VDD} as close as possible to the V_{DD} pin.

High-Side Gate-Drive Supply (BST_)

The drive voltage for the high-side MOSFETs is generated using a bootstrap circuit. The capacitor, $C_{BST\_}$, should be sized properly to minimize the ripple voltage for switching. The ripple voltage should be less than 200mV. For more information on selecting capacitors for the BST circuit, see the *Selecting a BST Capacitor* section. To minimize the forward voltage drop across the bootstrap diodes (D2), use Schottky diodes. The recommended value for the boost capacitors ($C_{BST\_}$) is 0.22µF.

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MOSFET Drivers

The DH_ and DL_ drivers are optimized for driving large high-side (N1 and N2) and larger low-side MOSFETs (N3 and N4). This is consistent with the low duty-cycle operation of the controller. The DL_ low-side drive waveform is always the complement of the DH_ high-side drive waveform, with a fixed dead-time between one MOSFET turning off and the other turning on to prevent cross-conduction or shoot-through current.

The internal transistor that drives DL_ low is robust with a 0.5Ω (typ) on-resistance. This helps prevent DL_ from being pulled up during the fast rise time of the LX_ node due to capacitive coupling from the drain to the gate of the low-side synchronous-rectifier MOSFET. However, some combinations of high-side and low-side MOSFETs may cause excessive gate-drain coupling, leading to poor efficiency, EMI, and shoot-through currents. This is often remedied by adding a resistor (typically less than 5Ω) in series with BST_, which increases the turn-on time of the high-side MOSFET without degrading the turn-off time.

Current-Limit Circuit

The MAX1937/MAX1938/MAX1939 use either the on-resistance of the low-side MOSFETs or a current-sense resistor to monitor the inductor current. Using the low-side MOSFETs' on-resistance as the current-sense element provides a lossless and inexpensive solution ideal for high-efficiency or cost-sensitive applications. The disadvantage to this method is that the on-resistance of MOSFETs vary from part to part, and overtemperature, which means it cannot be counted on for high accuracy. If high accuracy is needed, use current-sense resistors, which provide an accurate current limit under all conditions but reduce efficiency slightly because of the power lost in the resistors.

The current-limit circuit employs a "valley" current-sensing algorithm to monitor the inductor current. If the current-sense signal does not drop below the current-limit threshold, the controller does not initiate a new cycle. This limits the maximum value of I_{VALLEY} to the current set by the current-limit threshold (Figure 2).

The current-limit threshold is adjustable over a wide range, allowing for a range of current-sense resistor values. The voltage on ILIM sets the current-limit threshold between PGND and CS_ to $0.1 \times V_{ILIM}$. The 10mV to 200mV adjustment range corresponds to ILIM voltages from 100mV to 2V. The ILIM voltage is set by a resistor-divider between REF and GND. See the *Setting the Current Limit* section for details.

Current Balancing

The DC current balancing between phases depends on the accuracy of the current-sense elements and the offset of the current-balance amplifier.

The maximum offset of the current-balance amplifier ($V_{CBOFFSET}$) is ±3mV. The current-balance accuracy can be calculated from:

$$\text{Current-balance accuracy} = V_{CBOFFSET} / (I_L \times R_{CS})$$

where I_L is the peak inductor current and R_{CS} is the value of the current-sense resistor.

The current-balance accuracy is most important at full load. With a load current of 50A (I_L = 25A) and 2mΩ current-sense resistors, the worst-case current-balance accuracy is:

$$\text{Current-balance accuracy} = 0.003 / (25 \times 0.002) = 6\%$$

If the on-resistance of the low-side MOSFETs is used for current sensing, the part-to-part variation of the MOSFET on-resistance is a significant factor in the current balance. The matching between MOSFETs should be on the order of 15%, worst case. Thus, even if the current-balance amplifier has no offset, the DC-current balance could be as bad as 15%. In practice, a little help is received from the thermal ballasting of the MOSFETs. That is to say, the positive temperature coefficient of the on-resistance of MOSFETs reduces the mismatch current between the two phases.

Voltage Positioning (VPOS)

During a load transient, the output voltage instantly changes by the ESR of the output capacitors times the change in load current ($\Delta V_{OUT} = -ESR_{COUT} \times \Delta I_{LOAD}$). Conventional DC-DC converters respond by regulating the output voltage back to its nominal state after the load transient occurs (Figure 3). However, the CPU requires that the output voltage remain within a specific voltage band. Dynamically positioning the output voltage allows the use of fewer output capacitors and reduces power consumption under heavy load.

For a conventional (nonvoltage-positioned) circuit, the total output voltage deviation from light load to full load and back to light load is:

$$V_{P-P1} = 2 \times (ESR_{COUT} \times \Delta I_{LOAD}) + V_{SAG} + V_{SOAR}$$

where V_{SAG} and V_{SOAR} are defined in the *Output Capacitor Selection* section. Setting the converter to regulate at a lower voltage when under load allows a larger voltage step when the output current suddenly decreases. The total voltage change for a voltage-positioned circuit is:

$$V_{P-P2} = (ESR_{COUT} \times \Delta I_{LOAD}) + V_{SAG} + V_{SOAR}$$

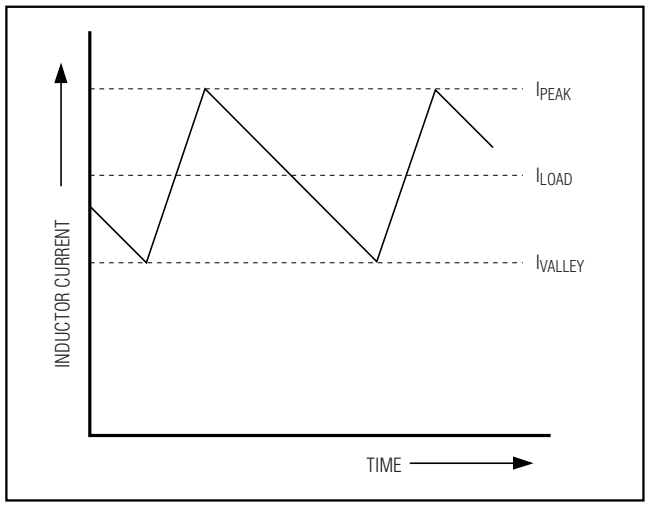


Figure 2. Inductor Current Waveform

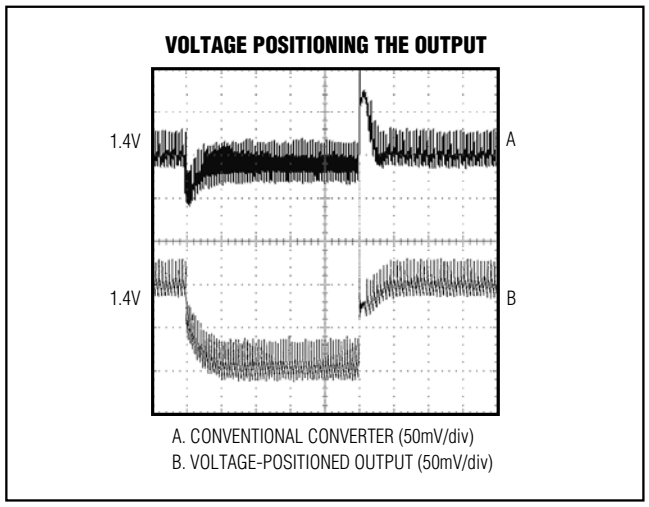


Figure 3. Voltage-Positioning and Nonvoltage-Positioning Waveforms

The maximum allowable voltage change during a transient is fixed by the supply range of the CPU ($V_{P-P1} = V_{P-P2}$). This means that the voltage-positioned circuit tolerates twice the ESR in the output capacitors. Because the ESR specification is achieved by paralleling several capacitors, fewer capacitors are needed for the voltage-positioned circuit. Figure 4 shows transient response regions.

An additional benefit of voltage positioning is reduced power consumption at high-load currents. Because the output voltage is lower under heavy load, the CPU draws less current. The result is lower power dissipation in the CPU.

Voltage Reference (REF)

A 2V reference is provided on the MAX1937/MAX1938/MAX1939 through the REF pin. REF is capable of sourcing or sinking up to 50µA. In addition to providing a reference for the IC, REF is used for setting the current limit and voltage positioning. Connect a 0.47µF capacitor from REF to GND. This capacitor should be placed as close as possible to the REF pin.

A UVLO is provided for the reference voltage. The reference voltage must rise above 1.600V to activate the controller. The controller is disabled if the reference voltage falls below 1.584V.

Enable Input (EN) and Soft-Start

When EN is low, DL_ and DH_ are held low (turning off the MOSFETs), leaving LX_ high impedance. In addition, the reference is turned off and PWRGD is pulled low. In shutdown, total current consumption is about 50µA (typ).

In the case of shutdown by VID code, only DL_ and DH_ are held low. The rest of the controller is enabled.

When EN is driven high, the startup sequence begins. Once the reference voltage rises above its 1.6V UVLO threshold, the controller begins switching and starts to ramp up the output voltage. The output voltage is ramped up in 25mV steps every 50µs until the output reaches the nominal output voltage.

Fault Conditions

The MAX1937/MAX1938/MAX1939 contain internal circuitry to protect themselves and surrounding circuitry from damage from output overvoltage and output undervoltage conditions. When either of these conditions occurs, DH_ is pulled low, DL_ is driven high, and PWRGD is pulled low. These pins remain in this state until either power is cycled on V_{DD} or EN is toggled high-low-high.

Setting the Output Voltage (VID_)

An internal DAC is used to set the output regulation voltage. A 5-bit code on inputs VID0–VID4 is used to specify the output voltage. Some codes disable the output. There is an internal 100kΩ pullup resistor to VDD on each of the VID_ inputs. Connecting VID_ to GND sets the bit to logic low (0); connecting VID_ to VDD or leaving it unconnected sets the bit to logic high (1). Use external pullup resistors to speed the low-to-high logic transition, or for lower logic voltages. See Table 1 for a list of codes and corresponding output regulation voltages for each of the parts.

The VID_ codes for the MAX1937 comply with AMD Hammer code. The VID_ codes on the MAX1938 are

Two-Phase Desktop CPU Core Supply Controllers with Controlled VID Change

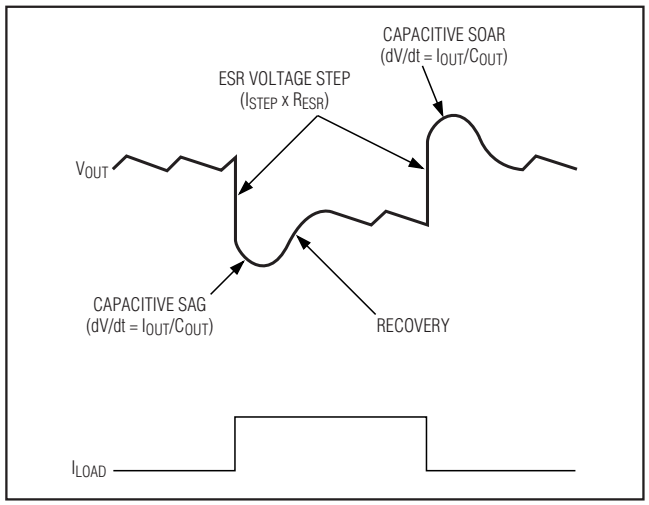


Figure 4. Transient Response Regions

set for Intel VRM 9.0/9.1 and AMD Athlon. The MAX1939 is set for AMD Athlon Mobile.

VID_ Change Slew Rate (TIME)

The MAX1937/MAX1938/MAX1939 allow the VID_ code to be changed while the converter is operating (on-the-fly). The slew rate at which the output voltage is changing is controlled through TIME. The slew rate is adjusted externally by connecting a 47kΩ to 470kΩ resistor (R_{TIME}) from TIME to GND. To set the slew rate, select the R_{TIME} resistor using the following equation:

$$R_{TIME} = \frac{521}{SR}\ (\Omega)$$

where SR is the slew rate of the output voltage in V/µs. The output voltage is stepped up or down in 25mV steps until it reaches the voltage set by the new VID code.

Power-Good Output (PWRGD)

PWRGD is an open-drain output that is pulled low when the output voltage deviates more than 12.5% from its regulation voltage (set by VID_ inputs). PWRGD is pulled low in shutdown, input UVLO, and during start-up. Any fault condition forces PWRGD low until the fault is cleared, and the IC is reset by cycling power at V_{DD} or momentarily toggling EN. For logic-level output voltages, connect an external pullup resistor between PWRGD and the logic power supply. A 100kΩ resistor works well in most applications.

Design Procedure

Output Inductor Selection

For most applications, an inductor value of 0.5µH to 1µH is recommended. The inductance is set by the desired amount of inductor current ripple (LIR). A larger inductance value minimizes output ripple current and increases efficiency, but slows transient response. For the best compromise of size, cost, and efficiency, a LIR of 30% to 40% is recommended (LIR = 0.3 to 0.4). The inductor value is found from:

$$L = \frac{V_{OUT} \times \left(V_{IN} - V_{OUT}\right)}{V_{IN} \times f_{SW} \times I_{LOAD(MAX)} \times LIR}$$

where f_{SW} is the actual switching frequency of a phase. The selected inductor should have the lowest possible equivalent DC resistance and a saturation current greater than the peak inductor current (I_{PEAK}). I_{PEAK} is found from:

$$I_{PEAK} = I_{LOAD(MAX)} \times \left(1 + \frac{LIR}{2}\right)$$

Output Capacitor Selection

The output capacitor must have low enough ESR to meet output ripple and load-transient requirements. Also, the capacitance value must be high enough to absorb the inductor energy going from a full-load to a no-load condition without tripping the OVP circuit.

In CPU core power supplies and other applications where the output is subject to large load transients, the output capacitor's size typically depends on how much ESR is needed to prevent the output from dipping too low under a load transient. Ignoring the sag due to finite capacitance:

$$R_{ESR} = V_{STEP(MAX)} / \Delta I_{LOAD(MAX)}$$

The actual capacitance value required relates to the physical size needed to achieve low ESR, as well as to the chemistry of the capacitor technology. Thus, the capacitor is usually selected by ESR and voltage rating rather than by capacitance value (this is true of OS-CONs, SP capacitors, POSCAPs, and other electrolytic capacitors). Generally, ceramic capacitors are not recommended for bulk output capacitance but make excellent high-frequency decoupling capacitors.

Once enough capacitance is added to meet the overshoot requirement, undershoot at the rising load edge

(V_{SAG}) is no longer a problem. The amount of overshoot from stored inductor energy can be calculated as:

$$V_{SOAR} = \frac{I^2_{PEAK} \times L}{2 \times C_{OUT} \times V_{OUT}}$$

where I_{PEAK} is the peak inductor current.

The undershoot at the rising load edge of a load transient is calculated from:

$$V_{SAG} = \frac{L \times \Delta I^2_{LOAD} \times \left[\frac{V_{OUT} \times K}{V_{IN}} + t_{OFF(MIN)} \right]}{2 \times C_{OUT} \times V_{OUT} \times \left[\frac{(V_{IN} - V_{OUT}) \times K}{V_{IN}} - t_{OFF(MIN)} \right]}$$

where ΔI_{LOAD} is the change in load current, and K is 4µs.

To ensure stability, make sure that the zero frequency created by the output capacitance, and the ESR of the output capacitor do not exceed 50kHz. The zero frequency is found from:

$$f_{ZESR} = \frac{1}{2\pi \times ESR_{COUT} \times C_{OUT}}$$

Currently, aluminum electrolytic, Sanyo POSCAP, and Panasonic SP capacitors have ESR zero frequencies well below 50kHz. When using ceramic capacitors, it might be necessary to use a series resistance to ensure that the ESR zero is below 50kHz.

Input Capacitor Selection

The input capacitor reduces peak currents drawn from the power source and reduces noise and voltage ripple on the input caused by the circuit's switching. The input capacitor must meet the ripple current requirement (I_{RMS}) imposed by the switching currents as defined by the following equation:

$$I_{RMS} = \frac{I_{LOAD}}{2} \frac{\sqrt{V_{OUT} \times (V_{IN} - V_{OUT})}}{V_{IN}}$$

I_{RMS} has a maximum value when the input voltage equals twice the output voltage (V_{IN} = $2V_{OUT}$), so $I_{RMS(MAX)}$ = I_{LOAD} / 2. For most applications, nontantalum capacitors (ceramic, aluminum electrolytic, polymer, or OS-CON) are preferred at the input because of their robustness with high inrush currents typical of systems that may be powered from very low impedance sources.

Multiple smaller value capacitors can be used in parallel to satisfy the ESR and capacitance requirements.

Selecting a BST Capacitor

The BST capacitors must be large enough to handle the gate-charging requirements of the high-side MOSFETs. For most applications, 0.22µF ceramic capacitors are recommended.

BST capacitors are needed to keep the voltage on the BST_ pins from dropping too much when the high-side MOSFET gates are charged. A capacitor value that prevents $V_{BST\_}$ from dropping more than 100mV to 200mV is adequate. The capacitance needed for the BST_ capacitor is calculated from:

$$C_{BST\_} = \frac{Q_{GH}}{\Delta V_{BST\_}}$$

where Q_{GH} is the total gate charge of the high-side MOSFET and $\Delta V_{BST\_}$ is the amount that the voltage on the BST_ pin drops when the gate is charged. If using multiple MOSFETs in parallel, use the sum of all the gate charges for Q_{GH}.

Setting the Current Limit

Current limit sets the maximum value of the inductor "valley" current. I_{VALLEY} is calculated from the following equation:

$$I_{VALLEY} = \frac{I_{LOAD(MAX)}}{2} \times \left(1 - \frac{LIR}{2} \right)$$

The current-limit threshold (I_{LIMIT}) must be set higher than the valley current:

$$I_{LIMIT} > I_{VALLEY}$$

The current-limit threshold is set by the voltage at ILIM and the value of the current-sense resistors:

$$I_{LIMIT} = \frac{V_{ILIM}}{10 \times R_{CS}}$$

where V_{ILIM} is the voltage on the ILIM pin (0.1V to 2V) and R_{CS} is the value of the current-sense resistor. If the on-resistance of the low-side MOSFET is used for current sensing, then the maximum value of the on-resistance (overtemperature and part-to-part variation) must be used for R_{CS}.

Two-Phase Desktop CPU Core Supply Controllers with Controlled VID Change

V_{ILIM} is set from 0.5V to 2V by connecting ILIM to a resistor-divider from REF to GND. Select resistors R3 and R4 such that the current through the divider is at least 5µA:

$$R3 + R4 \le 400k\Omega$$

A typical value for R3 is 200kΩ; then solve for R4 using:

$$R4 = R3 \times \frac{V_{ILIM}}{2 - V_{ILIM}}$$

Setting the Voltage Positioning

Voltage positioning dynamically changes the output-voltage set point in response to the load current. When the output is loaded, the signals fed back from the current-sense inputs adjust the output voltage set point, thereby decreasing power dissipation. The load-transient response of this control loop is extremely fast yet well controlled, so the amount of voltage change can be accurately confined within the limits stipulated in the microprocessor power-supply guidelines. To understand the benefits of dynamically adjusting the output voltage, see the *Voltage Positioning (VPOS)* section.

The amount of output voltage change is adjusted by an external gain resistor (R_{VPOS}). Connect R_{VPOS} between REF and VPOS. The output voltage changes in response to the load current as follows:

$$V_{OUT} = V_{VID} - g_{m(VPOS)} \times R_{VPOS} \times \left(\frac{I_{OUT} \times R_{CS}}{2} \right)$$

where V_{VID} is the programmed output voltage set by the VID code (Table 1), and the voltage-positioning transconductance ($g_{m(VPOS)}$) is typically 20µS. R_{CS} is the value of the current-sense resistor connected from CS_ to PGND. If the on-resistance of the low-side MOSFETs is used instead of current-sense resistors for current sensing, then use the maximum on-resistance of the low-side MOSFETs for R_{CS} in the equation above.

MOSFET Power Dissipation

Power dissipation in the high-side MOSFET is worst at high duty cycles (maximum output voltage, minimum input voltage). Two major factors contribute to the high-side power dissipation, conduction losses, and switching losses. Conduction losses are because of current flowing through a resistance, and can be calculated from:

$$P_{D(HS)COND} = \frac{V_{OUT} \times I^2_{LOADMAX} \times R_{DS(ON)}}{4 \times V_{IN}}$$

where $R_{DS(ON)}$ is the on-resistance of the high-side MOSFET and V_{IN} is the input voltage. To minimize conduction losses, select a MOSFET with a low $R_{DS(ON)}$.

Switching losses are also a major contributor to power dissipation in the high-side MOSFET. Switching losses are difficult to precisely calculate and should be measured in the circuit. To estimate the switching losses, use the following equation:

$$P_{D(HS)SW} \cong (I_{PEAK} \times t_{fall} + I_{VALLEY} \times t_{rise}) \frac{V_{IN} \times f_{SW}}{2}$$

where I_{PEAK} and I_{VALLEY} are the maximum peak and valley inductor currents, t_{FALL} and t_{RISE} are the fall and rise times of the high-side MOSFET, and f_{SW} is the switching frequency (about 250kHz).

The total power dissipated in the high-side MOSFET is then found from:

$$P_{D(HS)} = P_{D(HS)COND} + P_{D(HS)SW}$$

The power dissipation in the low-side MOSFET is highest at low duty cycles (high input voltage, low output voltage), and is mainly because of conduction losses:

$$P_{D(LS)COND} = \left(1 - \frac{V_{OUT}}{V_{IN}}\right) \times \frac{I^2_{LOADMAX}}{4} \times R_{DS(ON)}$$

Switching losses in the low-side MOSFET are small because of its voltage being clamped by the body diode. Switching losses can be estimated from:

$$P_{D(LS)SW} \cong \frac{I_{LOADMAX}}{2} \times t_{DT} \times V_{DF} \times f_{SW}$$

where $I_{LOADMAX/2}$ is the maximum average inductor current, t_{DT} is the time/cycle that the low-side MOSFET conducts through its body diode, and V_{DF} is the forward voltage drop across the body diode.

The total power dissipation in the low-side MOSFET is:

$$P_{D(LS)} = P_{D(LS)COND} + P_{D(LS)SW}$$

IC Power Dissipation

During normal operation, power dissipation in the controller is mostly from the gate drivers. This can be calculated from the following equation:

$$P_{GATE} = 2 \times V_{VLG} \times f_{SW} \times (Q_{GH} + Q_{GL})$$

where f_{SW} is approximately 250kHz, Q_{GH} is the gate charge of the high-side MOSFET, and Q_{GL} is the gate charge of the low-side MOSFET. The values used for the gate charge are at the gate drive voltage (V_{VLG}). The "2" in the above equation is due to the two phases of the converter. If multiple MOSFETs are used in parallel, add the gate charges of each MOSFET to find the total gate charge used in the above equation.

Make sure that the maximum power dissipation of the IC is not exceeded (see the *Absolute Maximum Ratings*).

Applications Information

PC Board Layout Guidelines

A properly designed PC board layout is important in any switching DC-DC converter circuit. If possible, mount the MOSFETs, inductor, input/output capacitors, and current-sense resistor on the top side of the PC board. Connect the ground for these devices close together on a power ground plane. Make all other ground connections to a separate analog ground plane. Connect the analog ground plane to power ground at a single point.

To help dissipate heat, place high-power components (MOSFETs, inductor, and current-sense resistor) on a large PC board area, or use a heat sink. Keep high current traces short and wide to reduce the resistance in these traces. Also make the gate-drive connections (DH_ and DL_) short and wide, measuring 10 to 20 squares (50mils to 100mils wide if the MOSFET is 1in from the controller IC).

Use Kelvin sense connections for the current-sense resistors.

Place the REF capacitor, the V_{DD} capacitor, and the BST_ diode and capacitor as close as possible to the IC. If the IC is far from the input capacitors, bypass V_{CC} to GND with an additional 0.1µF or greater ceramic capacitor close to the V_{CC} pin.

For an example PC board layout, refer to the MAX1937 or MAX1938 evaluation kit.

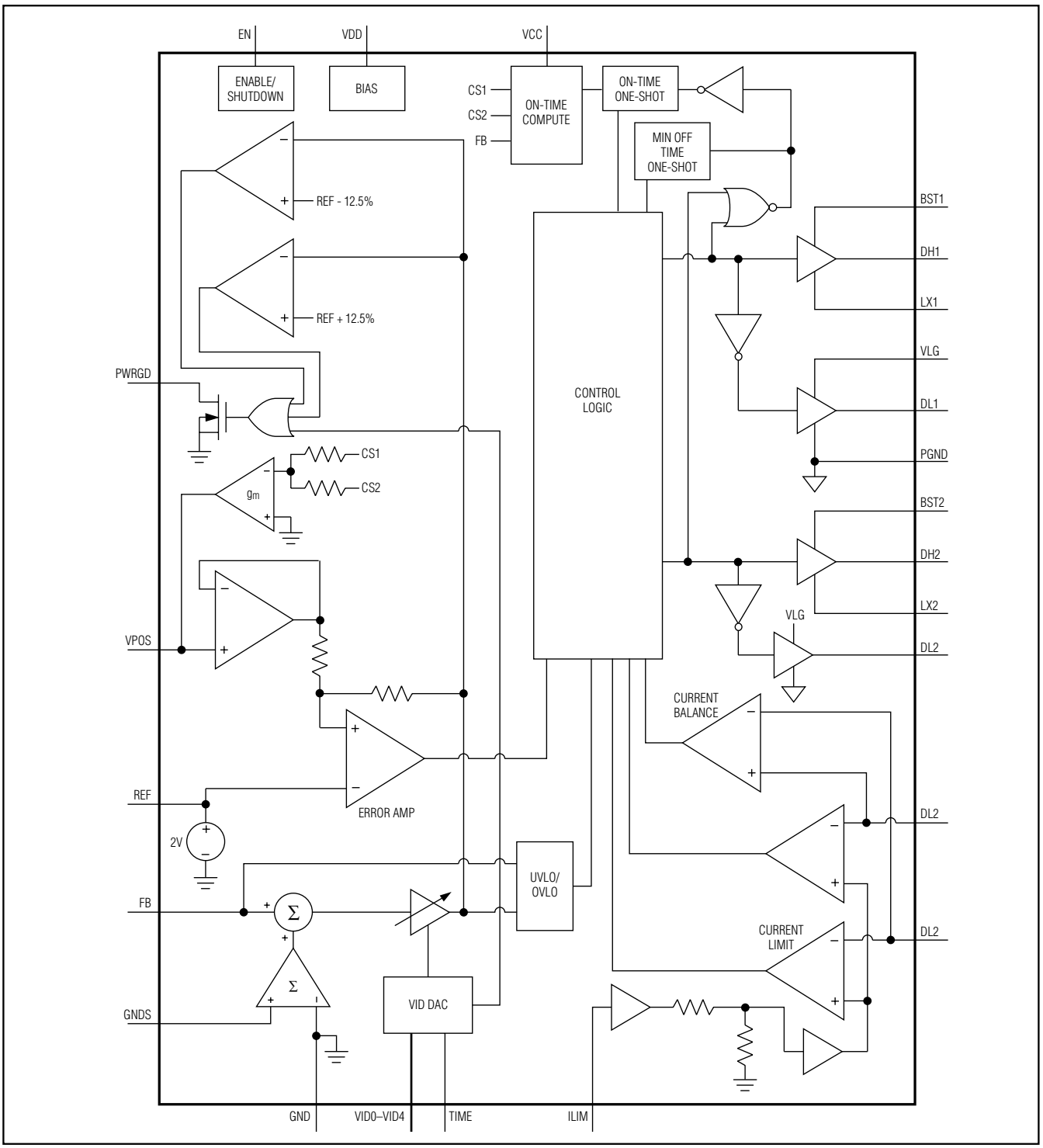
Chip Information

TRANSISTOR COUNT: 6243

PROCESS: BiCMOS

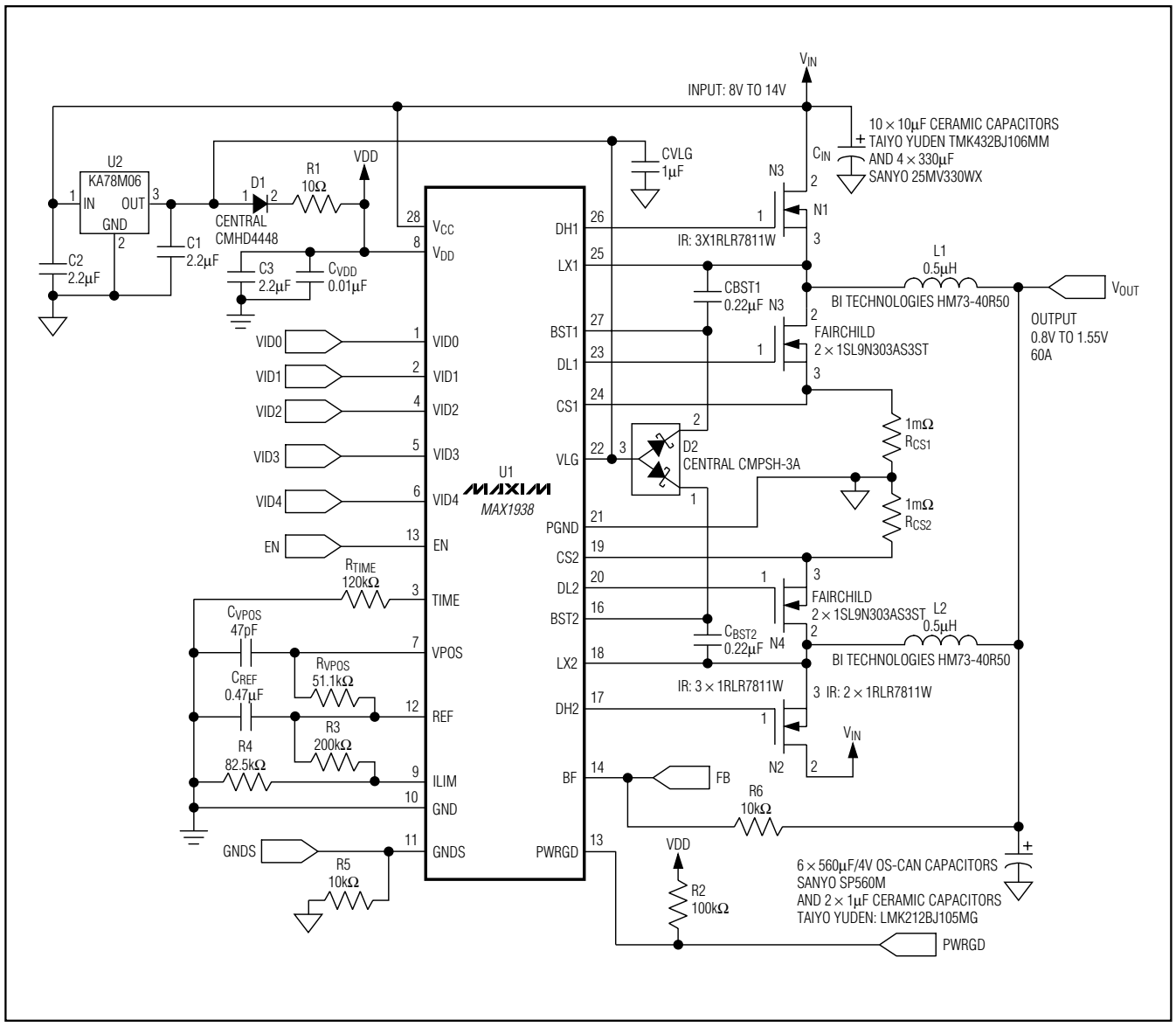
Two-Phase Desktop CPU Core Supply Controllers with Controlled VID Change

Functional Diagram



Two-Phase Desktop CPU Core Supply Controllers with Controlled VID Change

MAX1938 Typical Application Circuit

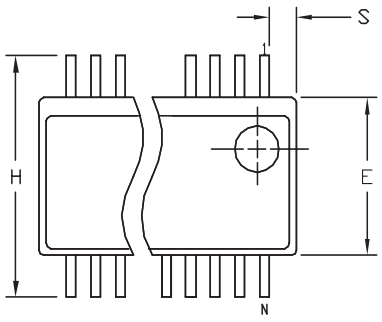


Two-Phase Desktop CPU Core Supply Controllers with Controlled VID Change

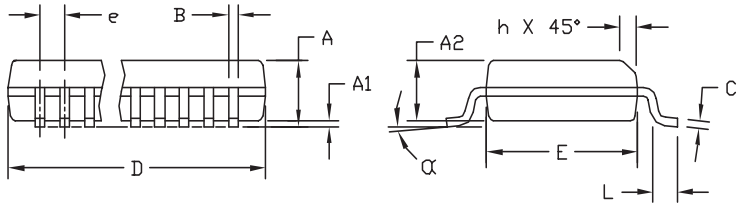
Package Information

(The package drawing(s) in this data sheet may not reflect the most current specifications. For the latest package outline information, go to **www.maxim-ic.com/packages**.)

QSOP.EPS



	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	.053	.069	1.35	1.75
A1	.004	.010	.102	.254
A2	.049	.065	1.245	1.651
B	.008	.012	0.20	0.30
C	.0075	.0098	0.191	0.249
D	SEE VARIATIONS			
E	.150	.157	3.81	3.99
e	.025 BSC		0.635 BSC	
H	.230	.244	5.84	6.20
h	.010	.016	0.25	0.41
L	.016	.035	0.41	0.89
N	SEE VARIATIONS			
α	0°	8°	0°	8°



VARIATIONS:

	INCHES		MILLIMETERS			
	MIN.	MAX.	MIN.	MAX.	N	
D	.189	.196	4.80	4.98	16	AB
S	.0020	.0070	0.05	0.18		
D	.337	.344	8.56	8.74	20	AD
S	.0500	.0550	1.270	1.397		
D	.337	.344	8.56	8.74	24	AE
S	.0250	.0300	0.635	0.762		
D	.386	.393	9.80	9.98	28	AF
S	.0250	.0300	0.635	0.762		

NOTES:
1). D & E DO NOT INCLUDE MOLD FLASH OR PROTRUSIONS.
2). MOLD FLASH OR PROTRUSIONS NOT TO EXCEED .006" PER SIDE.
3). CONTROLLING DIMENSIONS: INCHES.
4). MEETS JEDEC MO137.

DALLAS SEMICONDUCTOR MAXIM
PROPRIETARY INFORMATION

TITLE:
PACKAGE OUTLINE, QSOP .150", .025" LEAD PITCH

APPROVAL	DOCUMENT CONTROL NO.	REV.	
	21-0055	F	1/1

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