ABSOLUTE MAXIMUM RATINGS

V_{DD} to GND .....+6V
V_{SS} to GND (MAX110).....+0.3V to -6V
AGND to DGND.....-0.3V to +0.3V
V_{IN1+}, V_{IN1-} .....(V_{DD} + 0.3V) to (V_{SS} - 0.3V)
V_{IN2+}, V_{IN2-} .....(V_{DD} + 0.3V) to (V_{SS} - 0.3V)
V_{REF+}, V_{REF-} .....(V_{DD} + 0.3V) to (V_{SS} - 0.3V)
Digital Inputs and Outputs .....(V_{DD} + 0.3V) to -0.3V
Continuous Power Dissipation
16-Pin Plastic DIP (derate 10.53mW/°C above +70°C).....842mW
16-Pin Wide SO (derate 9.52mW/°C above +70°C) 762mW
20-Pin SSOP (derate 8.00mW/°C above +70°C) 640mW
16-Pin CERDIP (derate 10.00mW/°C above +70°C).....800mW
Operating Temperature Ranges
MAX11_ _C_ _.....0°C to +70°C
MAX11_ _E_ _.....-40°C to +85°C
MAX11_BMJE .....-55°C to +125°C
Storage Temperature Range .....-65°C to +160°C
Lead Temperature (soldering, 10sec) .....+300°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS—MAX110

(V_{DD} = 5V ±5%, V_{SS} = -5V ±5%, f_{XCLK} = 1MHz, ÷ 2 mode (DV2 = 1), 81,920 CLK cycles/conv, V_{REF+} = 1.5V, V_{REF-} = -1.5V, T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are at T_A = +25°C.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
ACCURACY (Note 1)							
Resolution	RES	(Note 2)		14 + POL + OFL			Bits
Differential Nonlinearity	DNL	(Notes 3, 4)				±2	LSB
No-Missing-Codes Resolution		(Note 3)		13 + POL + OFL			Bits
Relative Accuracy (Notes 3, 5–7)	INL	MAX110AC/E	$-V_{REF} \le V_{IN} \le V_{REF}$		±0.03	±0.06	%FSR
			$-0.83 \times V_{REF} \le V_{IN} \le 0.83 \times V_{REF}$		±0.015	±0.03	
		MAX110BC/E	$-V_{REF} \le V_{IN} \le V_{REF}$		±0.04		
			$-0.83 \times V_{REF} \le V_{IN} \le 0.83 \times V_{REF}$		±0.018		
		MAX110BM	$-V_{REF} \le V_{IN} \le V_{REF}$			±0.1	
			$-0.83 \times V_{REF} \le V_{IN} \le 0.83 \times V_{REF}$			±0.05	
Offset Error		$V_{IN+} = V_{IN-} = 0V$				±4	mV
Offset Error Temperature Drift		After offset null			0.003		µV/°C
		Uncalibrated			0.02		
Common-Mode Rejection Ratio	CMRR	$-2.5V \le (V_{IN+} = V_{IN-}) \le 2.5V$			6		ppm/V
Full-Scale Error		After gain calibration (Note 5)				±0.1	%
		Uncalibrated		-8		0	
Full-Scale Error Temperature Drift					8		ppm/°C
Power-Supply Rejection		V_{SS} = -5V, V_{DD} = 4.75V to 5.25V			15		ppm
		V_{DD} = 5V, V_{SS} = -4.75V to -5.25V			30		
ANALOG INPUTS							
Differential Input Voltage Range	V_{IN}	(Note 6)		$-V_{REF}$		$+V_{REF}$	V
Absolute Input Voltage Range	V_{IN+}, V_{IN-}			V_{SS} + 2.25		V_{DD} - 2.25	V
Input Bias Current	I_{IN+}, I_{IN-}					500	nA
Input Capacitance		(Note 3)				10	pF

ELECTRICAL CHARACTERISTICS—MAX110 (continued)

(V_{DD} = 5V ±5%, V_{SS} = -5V ±5%, f_{XCLK} = 1MHz, ÷ 2 mode (DV2 = 1), 81,920 CLK cycles/conv, V_{REF+} = 1.5V, V_{REF-} = -1.5V, T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are at T_A = +25°C.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
REFERENCE INPUTS							
Differential Reference Input Voltage Range	V_{REF}			0		3.0	V
Absolute Reference Input Voltage Range	V_{REF+}, V_{REF-}			V_{SS} + 2.25		V_{DD} - 2.25	V
Reference Input Current	I_{REF+}, I_{REF-}	V_{REF+} = 2.5V, V_{REF-} = 0V				500	nA
Reference Input Capacitance		(Note 3)				10	pF
CONVERSION TIME							
Synchronous Conversion Time (Note 7)	t_{CONV}	10,240 clock-cycles/conversion			20.48		ms
		102,400 clock-cycles/conversion			204.80		
Oversampling Clock Frequency	f_{OSC}	(Note 8)		0.25		1.25	MHz
DIGITAL INPUTS ($\overline{CS}$, SCLK, DIN, and XCLK when RCSEL = 0V)							
Input High Voltage	V_{IH}			2.4			V
Input Low Voltage	V_{IL}					0.8	V
Input Capacitance		(Note 3)				10	pF
Input Leakage Current	I_{LKG}	Digital inputs at 0V or 5V				±1	µA
DIGITAL OUTPUTS (DOUT, $\overline{BUSY}$, and XCLK when RCSEL = V_{DD})							
Output Low Voltage	V_{OL}	DOUT, $\overline{BUSY}$, I_{SINK} = 1.6mA				0.4	V
		XCLK, I_{SINK} = 200µA				0.4	
Output High Voltage	V_{OH}	DOUT, $\overline{BUSY}$, V_{DD} = 4.75V, I_{SOURCE} = 1.0mA		V_{DD} - 0.5			V
		XCLK, V_{DD} = 4.75V, I_{SOURCE} = 200µA		V_{DD} - 0.5			
Leakage Current	I_{LKG}	V_{OUT} = 5V or 0V				±10	µA
Output Capacitance		(Note 3)				10	pF
POWER REQUIREMENTS (all digital inputs at 0V or 5V)							
Positive Supply Voltage	V_{DD}	Performance guaranteed by supply rejection test		4.75		5.25	V
Negative Supply Voltage	V_{SS}	Performance guaranteed by supply rejection test		-4.75		-5.25	V
Positive Supply Current	I_{DD}	V_{DD} = 5.25V, V_{SS} = -5.25V	f_{XCLK} = 500kHz, continuous-conversion mode		550	950	µA
			XCLK unloaded, continuous-conversion mode, RC oscillator operational (Note 9)		780		
Negative Supply Current	I_{SS}	V_{DD} = 5.25V, V_{SS} = -5.25V	f_{XCLK} = 500kHz, continuous-conversion mode		320	650	µA
Power-Down Current	I_{DD}	V_{DD} = 5.25V, V_{SS} = -5.25V, V_{XCLK} = 0V, PD = 1			4	10	µA
	I_{SS}				0.05	2	

ELECTRICAL CHARACTERISTICS—MAX111

(V_{DD} = 5V ±5%, f_{XCLK} = 1MHz, ÷ 2 mode (DV2 = 1), 81,920 CLK cycles/conv, V_{REF+} = 1.5V, V_{REF-} = 0V, T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are at T_A = +25°C.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
ACCURACY (Note 1)							
Resolution	RES	(Note 2)		14 + POL + OFL			Bits
Differential Nonlinearity	DNL	(Notes 3, 4)				±2	LSB
No-Missing-Codes Resolution		(Note 3)		13 + POL + OFL			Bits
Relative Accuracy, Differential Input (Notes 3, 5–7)	INL	MAX111AC/E	$-V_{REF} \le V_{IN} \le V_{REF}$		±0.05	±0.10	%FSR
			$-0.667 \times V_{REF} \le V_{IN} \le 0.667 \times V_{REF}$		±0.03	±0.05	
		MAX111BC/E	$-V_{REF} \le V_{IN} \le V_{REF}$			±0.18	
			$-0.667 \times V_{REF} \le V_{IN} \le 0.667 \times V_{REF}$			±0.10	
		MAX111BM	$-V_{REF} \le V_{IN} \le V_{REF}$			±0.25	
			$-0.667 \times V_{REF} \le V_{IN} \le 0.667 \times V_{REF}$			±0.20	
Relative Accuracy, Single-Ended Input (IN- = GND)	INL	MAX111AC/E	$0V \le V_{IN} \le V_{REF}$		±0.1		%FSR
			$V_{IN} \le 0.667 \times V_{REF}$		±0.06		
		MAX111BC/E	$0V \le V_{IN} \le V_{REF}$		±0.18		
			$V_{IN} \le 0.667 \times V_{REF}$		±0.10		
		MAX111BM	$0V \le V_{IN} \le V_{REF}$		±0.25		
			$V_{IN} \le 0.667 \times V_{REF}$		±0.15		
Offset Error		$V_{IN+} = V_{IN-} = 0V$				±4	mV
Common-Mode Rejection Ratio	CMRR	$10mV \le (V_{IN+} = V_{IN-}) \le 2.0V$			6		ppm/V
Full-Scale Error		After gain calibration (Note 5)				±0.2	%
		Uncalibrated		-8		0	
Full-Scale Error Temperature Drift					8		ppm/°C
Power-Supply Rejection		V_{DD} = 4.75V to 5.25V			15		ppm
ANALOG INPUTS							
Differential Input Voltage Range	V_{IN}	(Note 6)		$-V_{REF}$		$+V_{REF}$	V
Absolute Input Voltage Range	V_{IN+}, V_{IN-}			0		V_{DD} - 3.2	V
Input Bias Current	I_{IN+}, I_{IN-}					500	nA
Input Capacitance		(Note 3)				10	pF

ELECTRICAL CHARACTERISTICS—MAX111 (continued)

(V_{DD} = 5V ±5%, f_{XCLK} = 1MHz, ÷ 2 mode (DV2 = 1), 81,920 CLK cycles/conv, V_{REF+} = 1.5V, V_{REF-} = 0V, T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are at T_A = +25°C.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
REFERENCE INPUTS							
Differential Reference Input Voltage Range	V_{REF}			0		1.5	V
Absolute Reference Input Voltage Range	V_{REF+}, V_{REF-}			0		V_{DD} - 3.2	V
Reference Input Current	I_{REF+}, I_{REF-}	V_{REF+} = 1.5V, V_{REF-} = 0V				500	nA
Reference Input Capacitance		(Note 3)				10	pF
CONVERSION TIME							
Synchronous Conversion Time (Note 7)	t_{CONV}	10,240 clock-cycles/conversion			20.48		ms
		102,400 clock-cycles/conversion			204.80		
Oversampling Clock Frequency	f_{OSC}	(Note 8)		0.25		1.25	MHz
DIGITAL INPUTS ($\overline{CS}$, SCLK, DIN, and XCLK when RCSEL = 0V)							
Input High Voltage	V_{IH}			2.4			V
Input Low Voltage	V_{IL}					0.8	V
Input Capacitance		(Note 3)				10	pF
Input Leakage Current	I_{LKG}	Digital inputs at 0V or 5V				±1	µA
DIGITAL OUTPUTS (DOUT, $\overline{BUSY}$, and XCLK when RCSEL = V_{DD})							
Output Low Voltage	V_{OL}	DOUT, $\overline{BUSY}$, I_{SINK} = 1.6mA				0.4	V
		XCLK, I_{SINK} = 200µA				0.4	
Output High Voltage	V_{OH}	DOUT, $\overline{BUSY}$, V_{DD} = 4.75V, I_{SOURCE} = 1.0mA		V_{DD} - 0.5			V
		XCLK, V_{DD} = 4.75V, I_{SOURCE} = 200µA		V_{DD} - 0.5			
Leakage Current	I_{LKG}	V_{OUT} = 5V or 0V				±1	µA
Output Capacitance		(Note 3)				10	pF
POWER REQUIREMENTS (all digital inputs at 0V or 5V)							
Positive Supply Voltage	V_{DD}	Performance guaranteed by supply rejection test		4.75		5.25	V
Supply Current	I_{DD}	V_{DD} = 5.25V	f_{XCLK} = 500kHz, continuous-conversion mode		640	1200	µA
			XCLK unloaded, continuous-conversion mode, RC oscillator operational (Note 9)		960		
Power-Down Current	I_{DD}	V_{DD} = 5.25V, V_{XCLK} = 0V, PD = 1			4	10	µA

Note 1: These specifications apply after auto-null and gain calibration. Performance at power-supply tolerance limits is guaranteed by power-supply rejection tests. Tests are performed at V_{DD} = 5V and V_{SS} = -5V (MAX110).
Note 2: 32,768 LSBs cover an input voltage range of $\pm V_{REF}$ (15 bits). An additional bit (OFL) is set for $V_{IN} > V_{REF}$.
Note 3: Guaranteed by design. Not subject to production testing.
Note 4: DNL is less than ±2 counts (LSBs) out of 2^{15} counts (±14 bits). The major source of DNL is noise, and this can be further improved by averaging.
Note 5: See *3-Step Calibration* section in text.
Note 6: $V_{REF} = (V_{REF+} - V_{REF-})$, $V_{IN} = (V_{IN1+} - V_{IN1-})$ or $(V_{IN2+} - V_{IN2-})$. The voltage is interpreted as negative when the voltage at the negative input terminal exceeds the voltage at the positive input terminal.
Note 7: Conversion time is set by control bits CONV1–CONV4.
Note 8: Tested at clock frequency of 1MHz with the divide-by-2 mode (i.e. oversampling clock of 500kHz). See *Typical Operating Characteristics* section for the effect of other clock frequencies. Also read the *Clock Frequency* section.
Note 9: This current depends strongly on C_{XCLK} (see *Applications Information* section).

TIMING CHARACTERISTICS (see Figure 6)

(V_{DD} = 5V, V_{SS} = -5V (MAX110), $T_A = T_{MIN}$ to T_{MAX}, unless otherwise noted. Typical values are at T_A = +25°C.)

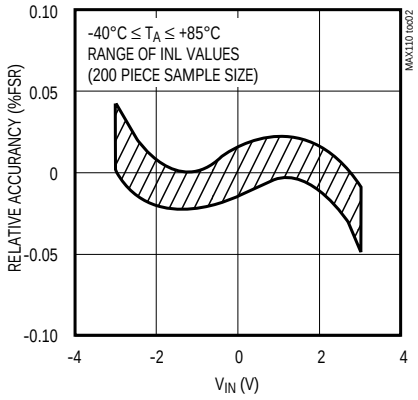
PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
$\overline{CS}$ to SCLK Setup Time (Note 10)	t_{CSS}	T_A = +25°C		60			ns
		MAX11_ _C/E		80			
		MAX11_ BM		100			
$\overline{CS}$ to SCLK Hold Time (Note 10)	t_{CSH}			0			ns
DIN to SCLK Setup Time (Note 10)	t_{DS}	T_A = +25°C		60			ns
		MAX11_ _C/E		80			
		MAX11_ BM		100			
DIN to SCLK Hold Time (Note 10)	t_{DH}			0			ns
SCLK, XCLK Pulse Width (Note 10)	t_{CK}	T_A = +25°C		100			ns
		MAX11_ _C/E		120			
		MAX11_ BM		160			
Data Access Time (Note 10)	t_{DA}	C_{LOAD} = 50pF	T_A = +25°C	0	35	80	ns
			MAX11_ _C/E	0		100	
			MAX11_ BM	0		120	
SCLK to DOUT Valid Delay (Note 10)	t_{DO}	C_{LOAD} = 50pF	T_A = +25°C	0	60	100	ns
			MAX11_ _C/E	0		120	
			MAX11_ BM	0		140	
Bus Relinquish Time (Note 10)	t_{DH}	T_A = +25°C			35	80	ns
		MAX11_ _C/E/M				120	
RC Oscillator Frequency		T_A = +25°C			2.0		MHz
		MAX11_ _C/E		1.3		2.8	
		MAX11_ BM		1.1		3.0	

Note 10: Timing specifications are guaranteed by design. All input control signals are specified with $t_r = t_f$ = 5ns (10% to 90% of +5V) and timed from a +1.6V voltage level.

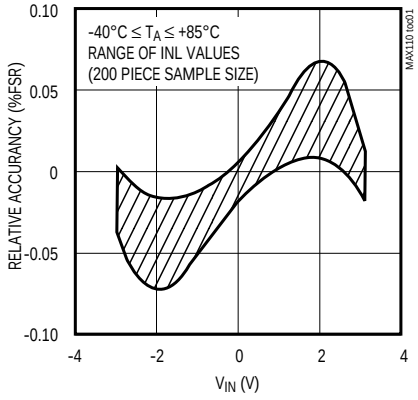
Typical Operating Characteristics

(MAX110, V_{DD} = 5V, V_{SS} = -5V, V_{REF+} = 1.5V, V_{REF-} = -1.5V, differential input (V_{IN+} = -V_{IN-}), f_{XCLK} = 1MHz, ÷ 2 mode (DV2 = 1), 81,920 clocks/conv, T_A = +25°C, unless otherwise noted.)

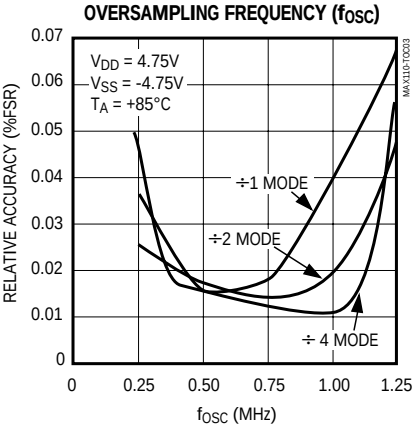
MAX110 RELATIVE ACCURACY (-0.83 V_{REF} < V_{IN} < 0.83 V_{REF})



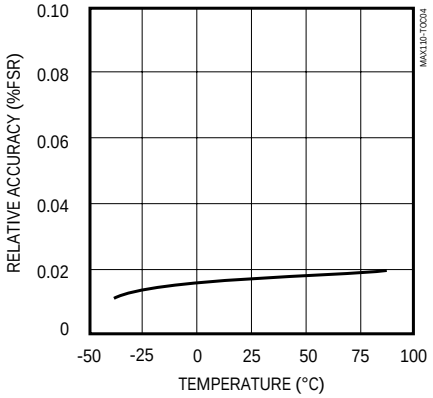
MAX110 RELATIVE ACCURACY (-V_{REF} < V_{IN} < V_{REF})



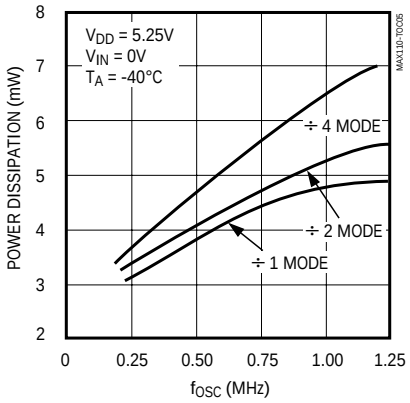
MAX110 RELATIVE ACCURACY vs. OVERSAMPLING FREQUENCY (f_{OSC})



MAX110 RELATIVE ACCURACY vs. TEMPERATURE



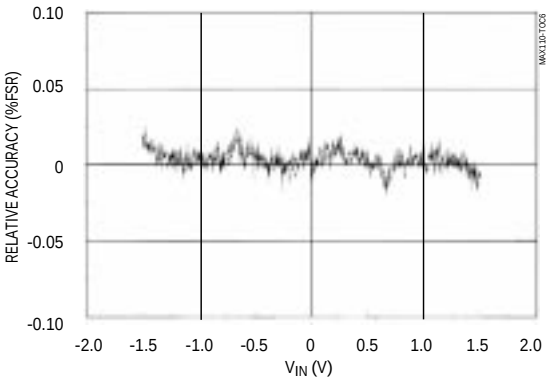
MAX110 POWER DISSIPATION vs. OVERSAMPLING FREQUENCY (f_{OSC})



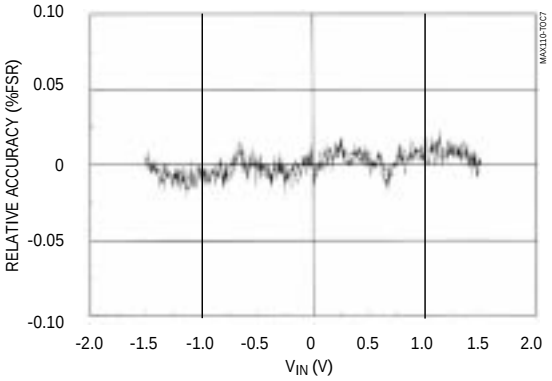
Typical Operating Characteristics (continued)

(MAX111, V_{DD} = 5V, V_{REF+} = 1.5V, V_{REF-} = 0V, differential input (V_{IN+} = -V_{IN-}), f_{XCLK} = 1MHz, ÷ 2 mode (DV2 = 1), 81,920 clocks/conv, T_A = +25°C, unless otherwise noted.)

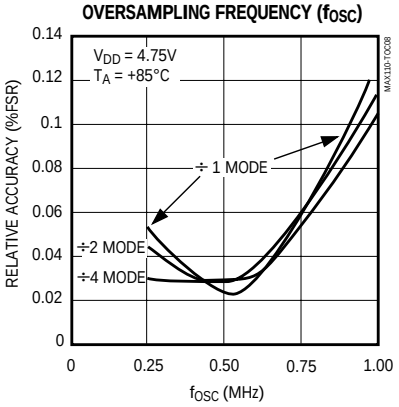
MAX111 RELATIVE ACCURACY (-0.667V_{REF} < V_{IN} < 0.667V_{REF})



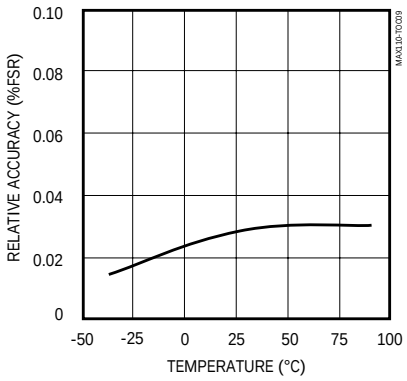
MAX111 RELATIVE ACCURACY (-V_{REF} < V_{IN} < V_{REF})



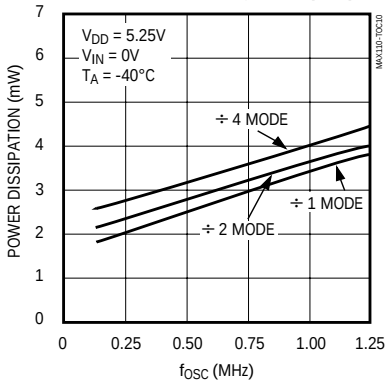
MAX111 RELATIVE ACCURACY vs. OVERSAMPLING FREQUENCY (f_{OSC})



MAX111 RELATIVE ACCURACY vs. TEMPERATURE



MAX111 POWER DISSIPATION vs. OVERSAMPLING FREQUENCY (f_{OSC})



Pin Description

PIN		NAME	FUNCTION
DIP/SO	SSOP		
1	1	IN1+	Channel 1 Positive Analog Input
2	2	REF-	Negative Reference Input
3	3	REF+	Positive Reference Input
4	6	V_{DD}	Positive Power-Supply Input—connect to +5V
5	7	RCSEL	RC Select Input. Connect to GND to select external clock mode. Connect to V_{DD} to select RC OSC mode. XCLK must be connected to V_{DD} or GND through a resistor (1MΩ or less) when RC OSC mode is selected.
6	8	XCLK	Clock Input / RC Oscillator Output. TTL/CMOS-compatible oversampling clock input when RCSEL = GND. Connects to the internal RC oscillator when RCSEL = V_{DD}. XCLK must be connected to V_{DD} or GND through a resistor (1MΩ or less) when RC OSC mode is selected.
7	9	SCLK	Serial Clock Input. TTL/CMOS-compatible clock input for serial-interface data I/O.
8	10	$\overline{BUSY}$	Busy Output. Goes low at conversion start, and returns high at end of conversion.
9	11	$\overline{CS}$	Chip-Select Input. Pull this input low to perform a control-word-write/data-read operation. A conversion begins when $\overline{CS}$ returns high, provided $\overline{NO\text{-}OP}$ is a 1. See the section *Using the MAX110/MAX111 with SPI, QSPI, and MICROWIRE Serial Interfaces.*
10	12	DOUT	Serial Data Output. High-impedance when $\overline{CS}$ is high.
11	13	DIN	Serial Data Input. See *Control Register* section.
12	16	GND	Digital Ground
13	17	V_{SS}	MAX110 Negative Power-Supply Input—connect to -5V
		AGND	MAX111 Analog Ground
14	18	IN2-	Channel 2 Negative Analog Input
15	19	IN2+	Channel 2 Positive Analog Input
16	20	IN1-	Channel 1 Negative Analog Input
—	4, 5, 14, 15	N.C.	No Connect—there is no internal connection to this pin

Detailed Description

The MAX110/MAX111 ADC converts low-frequency analog signals to a 16-bit serial digital output (14 data bits, a sign bit, and an overrange bit) using a first-order sigma-delta loop (Figure 1). The differential input voltage is internally connected to a precision voltage-to-current converter. The resulting current is integrated and applied to a comparator. The comparator output then drives an up/down counter and a 1-bit DAC. When the DAC output is fed back to the integrator input, the sigma-delta loop is completed.

During a conversion, the comparator output is a V_{REF-} to V_{REF+} square wave; its duty cycle is proportional to the magnitude of the differential input voltage applied to the ADC. The up/down counter clocks data in from the comparator at the oversampling clock rate and averages the pulse-width-modulated (PWM) square wave to produce the conversion result. A 16-bit static shift register stores the result at the end of the conversion. Figure 2 shows the ADC waveforms for a differential analog input equal to 1/2 (V_{REF+} - V_{REF-}). The resulting comparator and 1-bit DAC outputs are high for seven cycles and low for three cycles of the oversampling clock.

Since the analog input signal is integrated over many clock cycles, much of the signal and quantization noise is attenuated. The more clock cycles allowed during each conversion, the greater the noise attenuation (see *Programming Conversion Time*).

Low-Cost, 2-Channel, ±14-Bit Serial ADCs

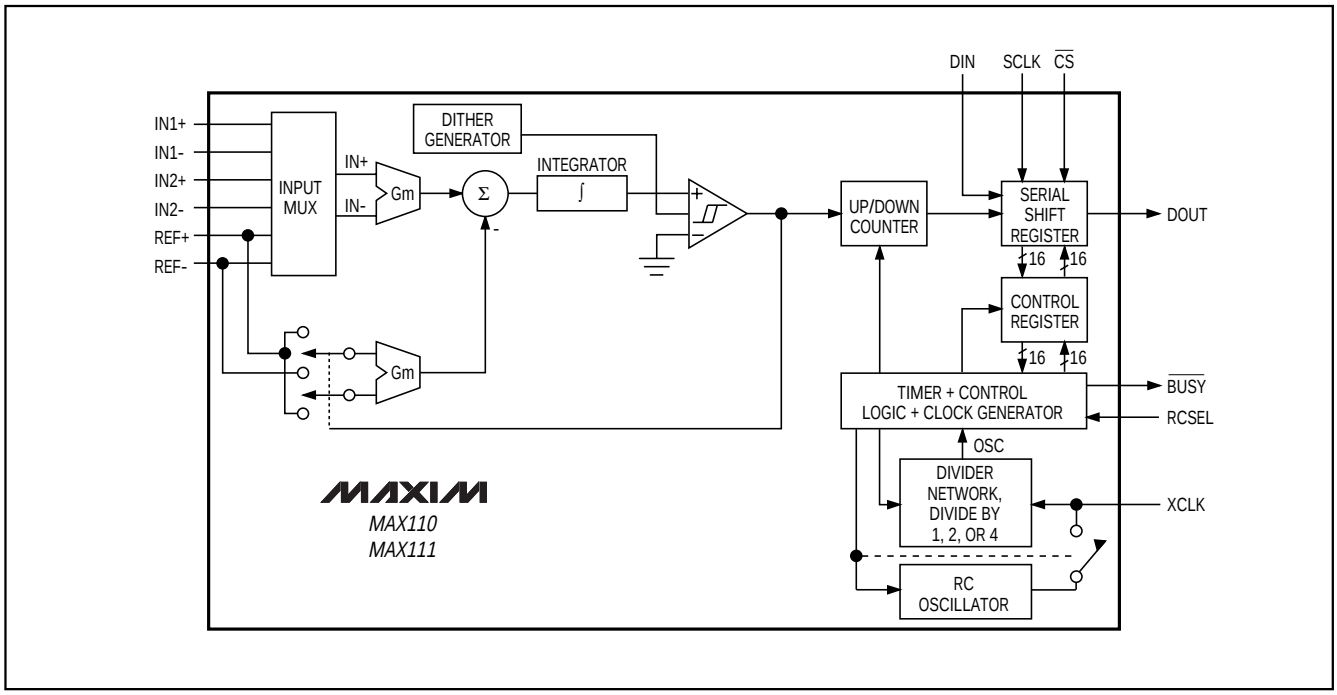


Figure 1. Functional Diagram

Oversampling Clock

XCLK internally connects to a clock-frequency divider network, whose output is the ADC oversampling clock, f_{OSC}. This allows the selected clock source (internal RC oscillator or external clock applied to XCLK) to be divided by one, two, or four (see *Clock Divider-Ratio Control Bits*).

Figure 3 shows the two methods for providing the oversampling clock to the MAX110/MAX111. In external-clock mode (Figure 3a), the internal RC oscillator is disabled and XCLK accepts a TTL/CMOS-level clock to provide the oversampling clock to the ADC.

Select external-clock mode (Figure 3a) by connecting RCSEL to GND and a TTL/CMOS-compatible clock to XCLK (see *Selecting the Oversampling Clock Frequency*).

In RC-oscillator mode (Figure 3b), the internal RC oscillator is active and its output is connected to XCLK (Figure 1). Select RC-oscillator mode by connecting RCSEL to V_{DD}. This enables the internal oscillator and connects it to XCLK for use by the ADC and external system components. Minimize the capacitive loading on XCLK when using the internal RC oscillator.

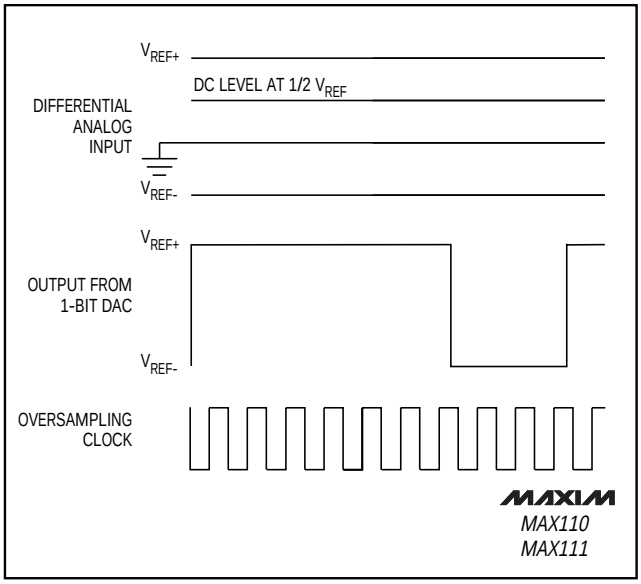


Figure 2. ADC Waveforms During a Conversion

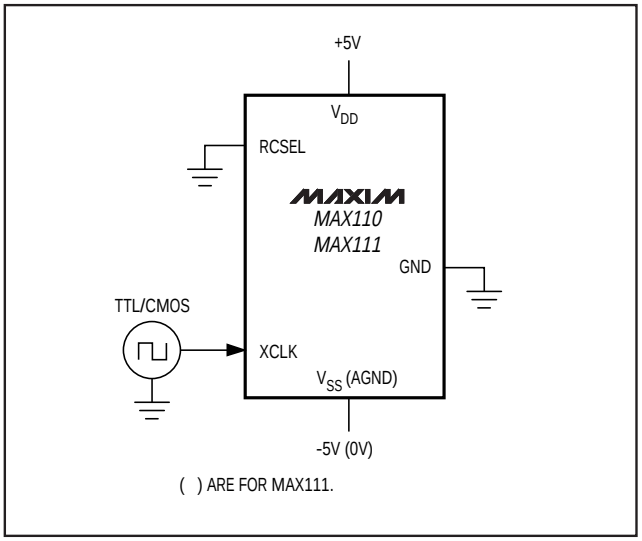


Figure 3a. Connection for External-Clock Mode

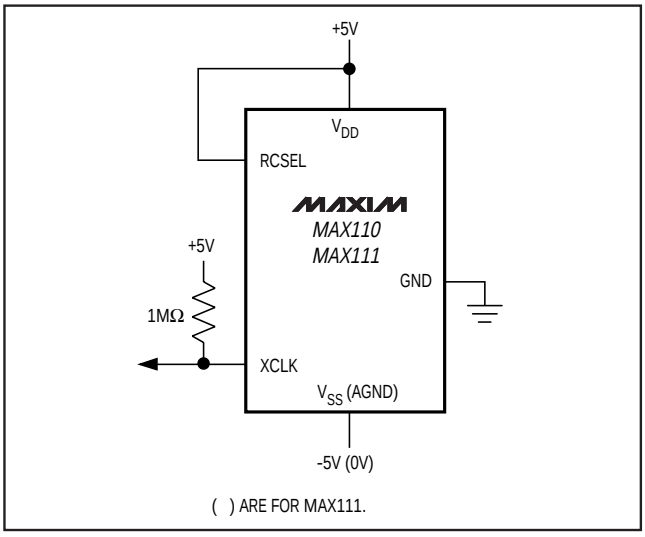


Figure 3b. Connection for Internal RC-Oscillator Mode—XCLK connects to the internal RC oscillator. Note, the pull-up resistor is not necessary if the internal oscillator is never shut down.

ADC Operation

The output data from the MAX110/MAX111 is arranged in twos-complement format (Figures 4, 5). The sign bit (POL) is shifted out first, followed by the overrange bit (OR), and the 14 data bits (MSB first) (see Figure 6). The MAX110 operates from ±5V power supplies and converts low-frequency analog signals in the ±3V range when using the maximum reference voltage of V_{REF} = 3V ($V_{REF} = V_{REF+} - V_{REF-}$). Within the ±3V input range, greater accuracy is obtained within ±2.5V (see *Electrical Characteristics* for details). Note that a negative input voltage is defined as $V_{IN-} > V_{IN+}$. For the MAX110, the absolute voltage at any analog input pin must remain within the (V_{SS} + 2.25V) to (V_{DD} - 2.25V) range.

The MAX111 operates from a single +5V supply and converts low-frequency differential analog signals in the ±1.5V range when using the maximum reference voltage of V_{REF} = 1.5V. As indicated in the *Electrical Characteristics*, greater accuracy is achieved within the ±1.2V range. The absolute voltage at any analog input pin for the MAX111 must remain within 0V to V_{DD} - 3.2V. When $V_{IN-} > V_{IN+}$ the input is interpreted as negative.

The overrange bit (OFL) is provided to sense when the input voltage level has exceeded the reference voltage level. The converter does not “saturate” until the input voltage is typically 20% larger. The linearity is not guaranteed in this range. Note that the overrange bit works properly if the reference voltage remains within the recommended voltage range (see *Reference Inputs*). If the reference voltage exceeds the recommended input range, the overrange bit may not operate properly.

Digital Interface—Starting a Conversion

Data is transferred into and out of the serial I/O shift register by pulling $\overline{CS}$ low and applying a serial clock at SCLK. This fully static shift register allows SCLK to range from DC to 2MHz. Output data from the ADC is clocked out on SCLK’s falling edge and should be read on SCLK’s rising edge. Input data to the ADC at DIN is clocked in on SCLK’s rising edge. A new conversion begins when $\overline{CS}$ returns high, provided the MSB in the input control word ($\overline{NO\text{-}OP}$) is a 1 (see *Using the MAX110/MAX111 with MICROWIRE, SPI, and QSPI Serial Interfaces*). Figure 6 shows the detailed serial-interface timing diagram.

$\overline{CS}$ must remain high during the conversion (while $\overline{BUSY}$ remains low). Bringing $\overline{CS}$ low during the conversion causes the ADC to stop converting, and may result in erroneous output data.

Using the MAX110/MAX111 with SPI, QSPI, and MICROWIRE Serial Interfaces

Figure 7 shows the most common serial-interface connections. The MAX110/MAX111 are compatible with SPI, QSPI (CPHA = 0, CPOL = 0), and MICROWIRE serial-interface standards.

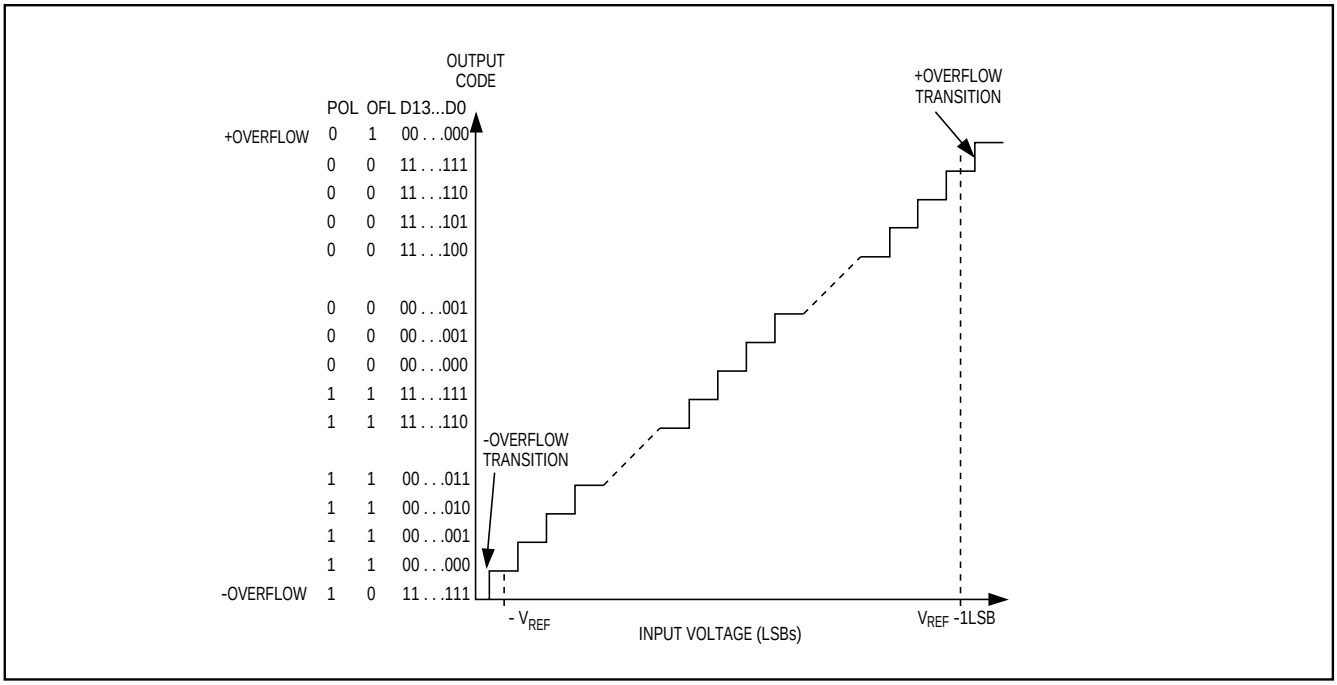


Figure 4. Differential Transfer Function

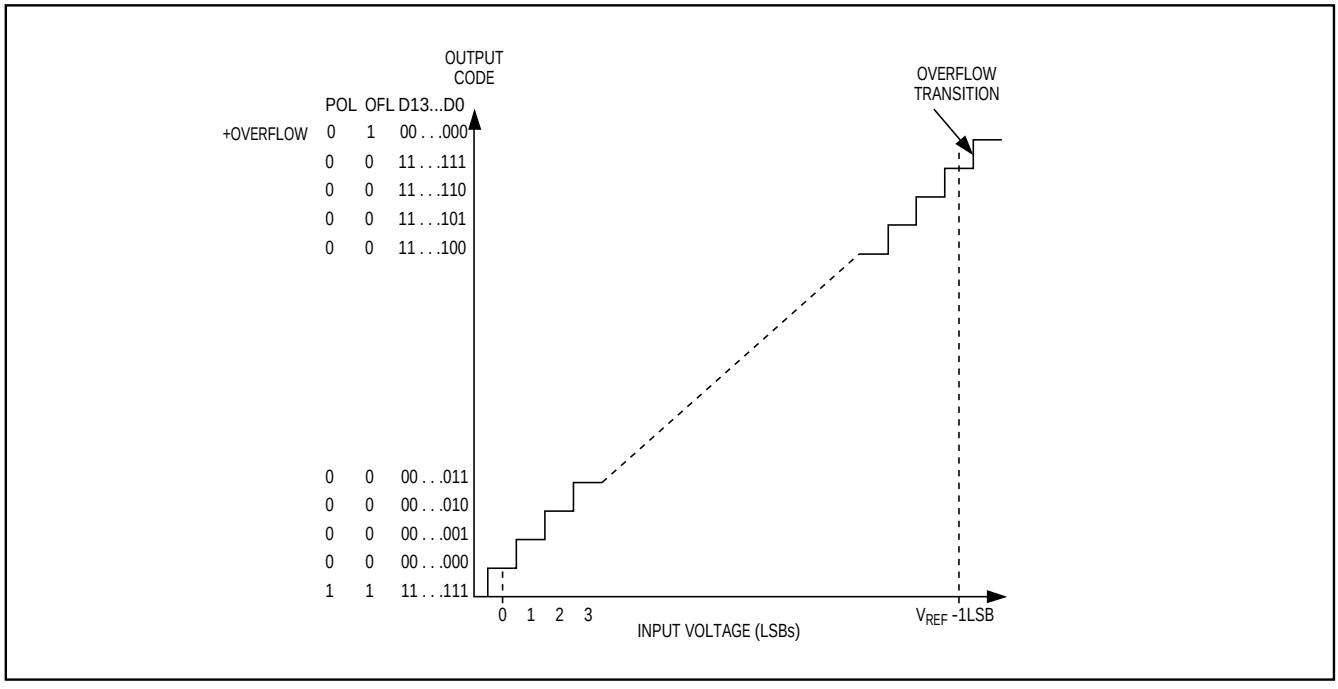


Figure 5. Unipolar Transfer Function

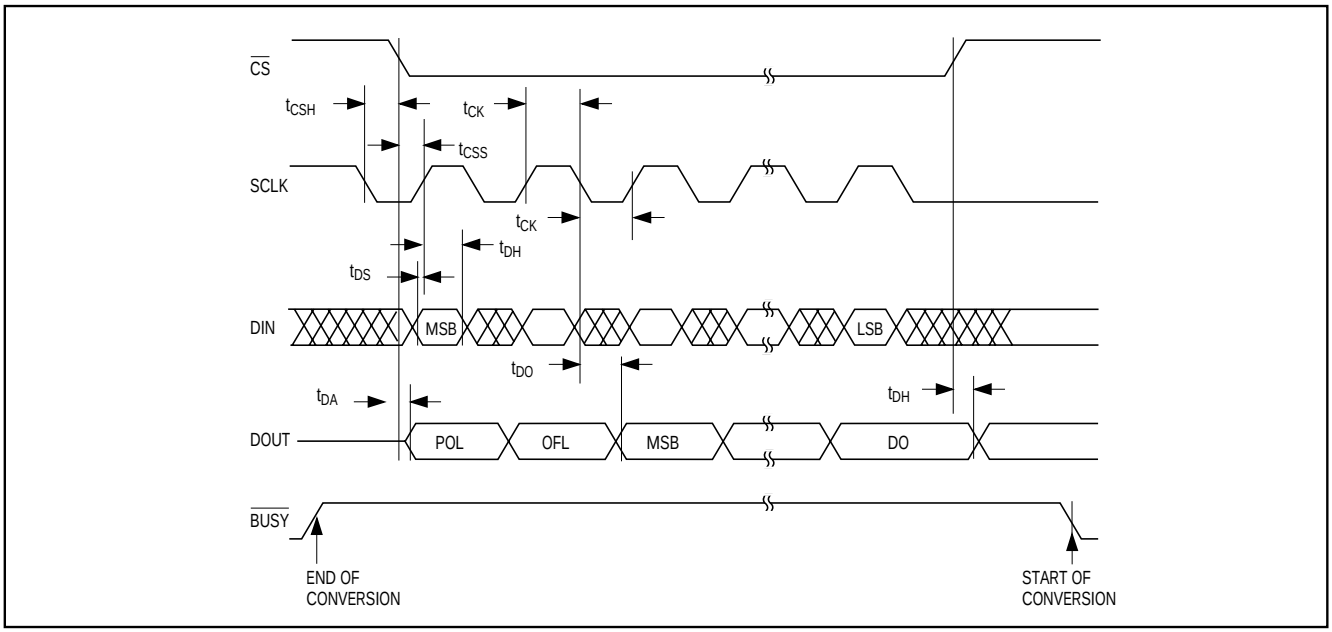


Figure 6. Detailed Serial-Interface Timing

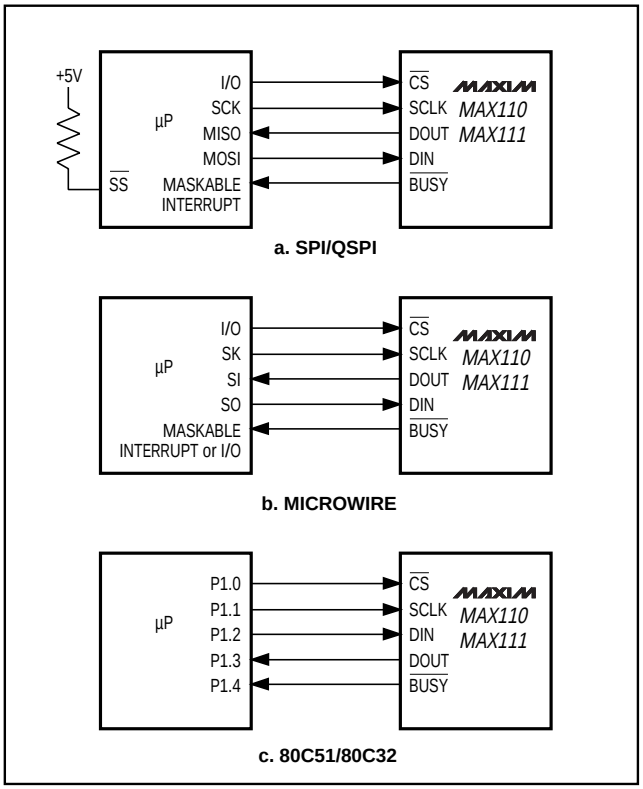


Figure 7. Common Serial-Interface Connections

The ADC serial interface operates with just SCLK, DIN, and DOUT (allow sufficient time for the conversion to complete between read/write operations). Achieve continuous operation by connecting $\overline{BUSY}$ to an uncommitted µP I/O or interrupt, to signal the processor when the conversion results are ready. Figures 8a and 8b show the timing for SPI/MICROWIRE and QSPI operation.

The fully static 16-bit I/O register allows infinite time between the two 8-bit read/write operations necessary to obtain the full 16 bits of data with SPI and MICROWIRE. $\overline{CS}$ must remain low during the entire two-byte transfer (Figure 8a). QSPI allows a full 16-bit data transfer (Figure 8b).

Interfacing to the 80C32 Microcontroller Family

Figure 7c shows the general 80C32 connection to the MAX110/MAX111 using Port 1. For a more detailed discussion, see the MAX110 evaluation kit manual.

I/O Shift Register

Serial data transfer is accomplished with a 16-bit fully static shift register. The 16-bit control word shifted into this register during a data-transfer operation controls the ADC's various functions. The MSB ($\overline{NO\text{-}OP}$) enables/disables transfer of the control word within the ADC. A logic 1 causes the remaining 15 bits in the control word to be transferred from the I/O register into the control register when $\overline{CS}$ goes high, updating the ADC's configuration and starting a new conversion. If

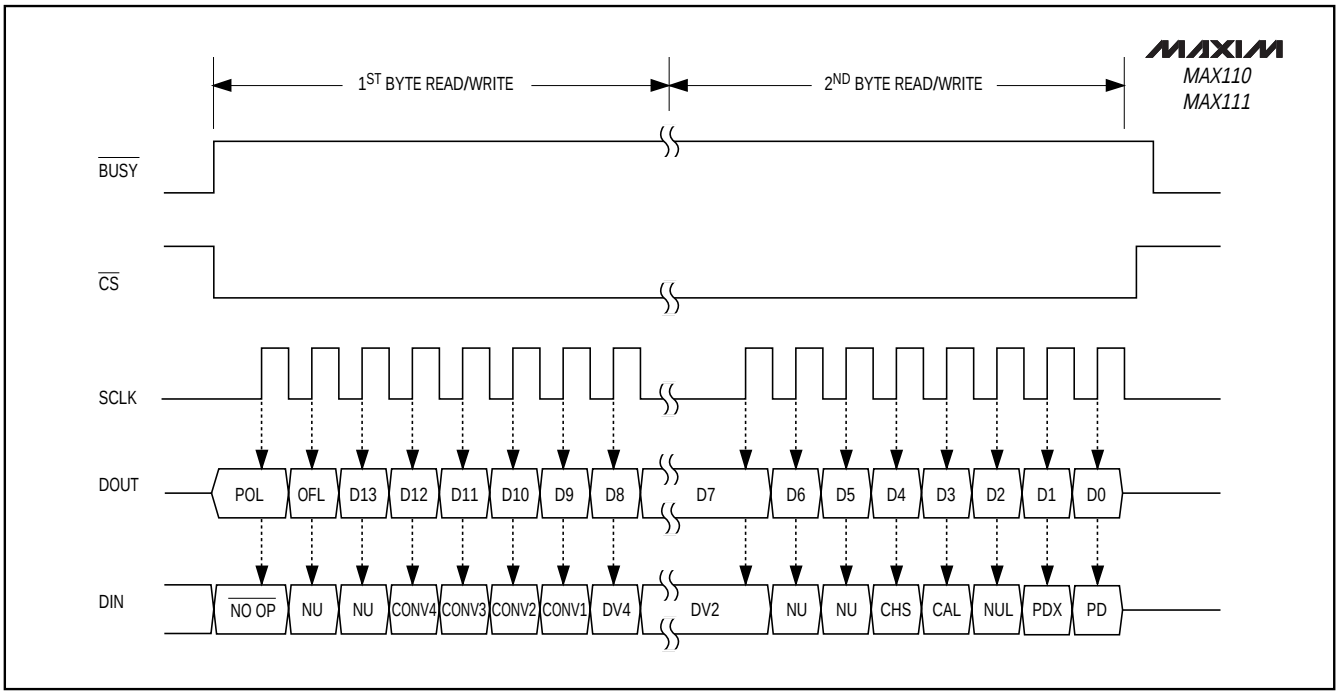


Figure 8a. SPI/MICROWIRE-Interface Timing

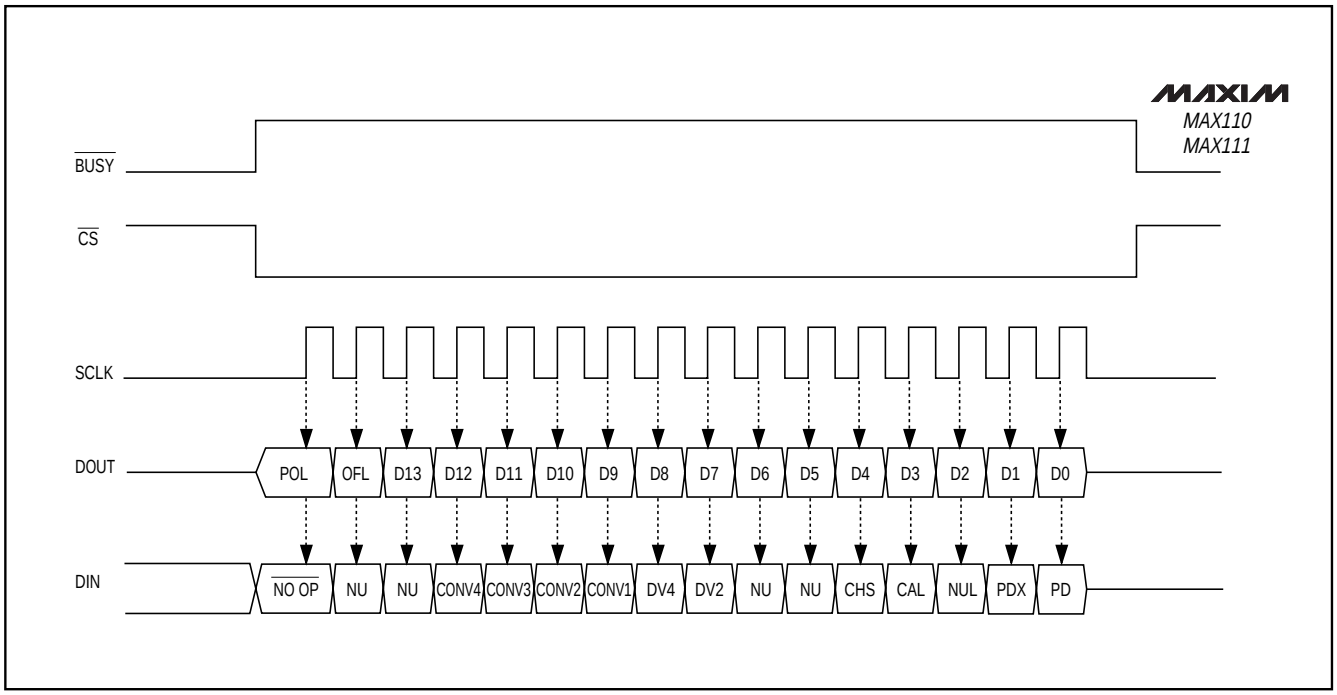


Figure 8b. QSPI Serial-Interface Timing

Table 1. Input Control-Word Bit Map

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
$\overline{\text{NO-OP}}$	NU	NU	CONV4	CONV3	CONV2	CONV1	DV4	DV2	NU	NU	CHS	CAL	NUL	PDX	PD

↑
First bit clocked in.

BIT	NAME	DESCRIPTION
15	$\overline{\text{NO-OP}}$	If this bit is a logic high, the remaining 15 LSBs are transferred to the control register and a new conversion begins when $\overline{\text{CS}}$ returns high. If this bit is set low, the control word is not passed to the control register, the ADC configuration remains unchanged, and no new conversion begins when $\overline{\text{CS}}$ returns high.
5, 6, 13, 14	NU	Used for test purposes only. Set these bits low.
9–12	CONV1–CONV4	Conversion Time Control Bits. See Table 4.
7, 8	DV2, DV4	XCLK to Oversampling Cock Ratio Control Bits. See Table 5.
4	CHS	Input Channel Select. A logic high selects channel 2 (IN2+ and IN2-), while a logic low selects channel 1 (IN1+ and IN1-). See Tables 2 and 3.
3	CAL	Gain-Calibration Bit. A logic high selects gain-calibration mode. See Table 3.
2	NUL	Internal Offset-Null Bit. A logic high selects offset-null mode. See Table 3.
1	PDX	Oscillator Power-Down. Set this bit high to power down the RC oscillator.
0	PD	Analog Power-Down. Set this bit high to power down the analog section.

$\overline{\text{NO-OP}}$ is a zero, the control word is not transferred to the control register, the ADC's configuration remains unchanged, and no new conversion is initiated. This allows specific ADCs in a "daisy chain" arrangement to be reconfigured while leaving the remaining ADCs unchanged. Table 1 lists the various ADC control word functions.

Output data is shifted out of DOUT at the same time the input control word for the next conversion is shifted in (Figure 8).

On power-up, all internal registers reset to zero. Therefore, when writing the first control word to the ADC, the data simultaneously shifted out will be zeros. The first conversion begins when $\overline{\text{CS}}$ goes high ($\overline{\text{NO-OP}}$ = 1). The results are placed in the 16-bit I/O register for access on the next data-transfer operation.

Power-Down Mode

Bits 0 and 1 control the ADC's power-down mode. If bit 0 (PD) is a logic high, power is removed from all analog circuitry except the RC oscillator. A logic high at bit 1 (PDX) removes power from the RC oscillator. If both bits PD and PDX are a logic high, or if PD is high and RCSEL is low, the supply currents reduce to 4µA. If an external XCLK clock continues to run in power-down mode, the supply current will depend on the clock rate.

When PDX is set high, the internal RC oscillator stops shortly after $\overline{\text{CS}}$ returns high. If the next control word written to the device has $\overline{\text{NO-OP}}$ = 1 instructing the ADC to convert, BUSY will go low, but because the RC oscillator is stopped, BUSY will remain low and will not allow a new conversion to begin. To avoid this situation, write a "dummy" control word with $\overline{\text{NO-OP}}$ = 0 and any combination of bits 14-0 in the control word following the control word with PDX = 0. With $\overline{\text{NO-OP}}$ = 0, bits 14-0 are ignored and the internal state machine resets. Next, perform a normal 3-step calibration (see Table 3). Note that XCLK must be connected to V_{DD} or GND through a resistor (suggested value is 1MΩ) when the RC oscillator mode is selected (RCSEL = V_{DD}). This resistor is not necessary if the external oscillator mode is used, or if the internal oscillator is not shut down.

Selecting the Analog Inputs

Bit 4 (CHS) controls which of the two differential inputs connect to the internal ADC inputs (see the *Functional Diagram*). A logic high selects IN2+ and IN2- while a logic low selects IN1+ and IN1-. Table 2 shows the allowable input multiplexer configurations.

Table 2. Allowable Input Multiplexer Configurations

CAL	NUL	CHS	$\overline{\text{NO-OP}}$	ADC IN+	ADC IN-	DESCRIPTION
0	0	0	1	IN1+	IN1-	Channel 1 connected to ADC inputs. Conversion begins when $\overline{CS}$ returns high.
0	0	1	1	IN2+	IN2-	Channel 2 connected to ADC inputs. Conversion begins when $\overline{CS}$ returns high.
0	1	0	1	IN1-	IN1-	IN1- connected to the ADC inputs; offset-null mode selected. Autonull conversion begins when $\overline{CS}$ returns high, and the results are stored in the null register.
0	1	1	1	IN2-	IN2-	IN2- connected to the ADC inputs; offset-null mode selected. Autonull conversion begins when $\overline{CS}$ returns high, and the results are stored in the null register.
1	1	X	1	REF-	REF-	REF- connected to the ADC inputs; offset-null mode selected. Autonull conversion begins when $\overline{CS}$ returns high, and the results are stored in the null register.
1	0	X	1	REF+	REF-	REF+ and REF- connected to the ADC inputs; gain-calibration mode selected. Autocal conversion begins when $\overline{CS}$ returns high, and the results are stored in the 16-bit I/O register.
X	X	X	0	No Change	No Change	Input control word is not transferred to the control register. ADC configuration remains unchanged and no new conversion starts when $\overline{CS}$ returns high.

X = Don't Care

Table 3. Procedure to Calibrate the ADC

STEP	DESCRIPTION	CONTROL WORD									
		$\overline{\text{NO-OP}}$	Not Used	CONV1-CONV4	DV2 & DV4	Not Used	CHS	CAL	NUL	PDX	PD
1	Sets the new conversion speed (if required) and performs an offset correction conversion with the internal ADC inputs shorted to REF-. The result is stored in the null register. (This step also selects the speed/resolution for the ADC.)	1	00	New Data	XX	00	X	1	1	0	0
2	Performs a gain-calibration conversion with the null register contents as the starting value. The result is stored in the calibration register.	1	00	No Change	XX	00	X	1	0	0	0
3	Performs an offset-null conversion with the internal ADC inputs shorted to the selected input channel's negative input (IN1- or IN2-). The next operation performs the first signal conversion with the new setup.	1	00	No Change	XX	00	0 or 1	0	1	0	0

X = Don't Care

3-Step Calibration

The data sheet electrical specifications apply to the device after optional calibration of gain error and offset. Uncalibrated, the gain error is typically 2%.

Table 3 describes the three steps required to calibrate the ADC completely.

Once the ADC is calibrated to the selected channel, set CAL = 0 and NUL = 0 and leave CHS unchanged in the next control word to perform a signal conversion on the selected analog input channel.

Calibrate the ADC after the following operations:

— when power is first applied

— if the reference common-mode voltage changes

— if the common-mode voltage of the selected input channel varies significantly. The CMRR of the analog inputs is 0.25LSB/V.

— after changing channels (if the common-mode voltages of the two channels are different)

— after changing conversion speed/resolution.

— after significant changes in temperature. The offset drift with temperature is typically 0.003µV/°C.

Automatic gain calibration is not allowed in the 102,400 cycles per conversion mode (see *Programming Conversion Time*). In this mode, calibration can be achieved by connecting the reference voltage to one input channel and performing a normal conversion. Subsequent conversion results can be corrected by software. **Do not issue a $\overline{\text{NO-OP}}$ command directly following the gain calibration, as the calibration data will be lost.**

Programming Conversion Time

The MAX110/MAX111 are specified for 12 bits of accuracy and up to ±14 bits of resolution. The ADC's resolution depends on the number of clock cycles allowed during each conversion. Control-register bits 9–12 (CONV1–CONV4) determine the conversion time by controlling the nominal number of oversampling clock cycles required for each conversion (OSCC/CONV). Table 4 lists the available conversion times and resulting resolutions.

To program a new conversion time, perform a 3-step calibration with the appropriate CONV1–CONV4 data used in Table 3. The ADC is now calibrated at the new conversion speed/resolution.

Table 4. Available Conversion Times

CONV4	CONV3	CONV2	CONV1	CLOCK CYCLES PER CONVERSION	NOMINAL CONVERSION TIME RCSEL = GND, DV2 = DV4 = 0, XCLK = 500kHz (ms)	CONVERSION RESOLUTION (Bits)
1	0	0	1	10,240	20.48	12 + POL
0	0	1	1	20,480	40.96	13 + POL
0	1	1	0	81,920	163.84	14 + POL
0	0	0	0	102,400*	204.80	14 + POL

* Gain-calibration mode is not available with 102,400 clock cycles/conversion selected.

Table 5. Clock Divider-Ratio Control

DV2	DV4	DESCRIPTION
0	0	XCLK or internal RC oscillator connects directly to the ADC; $f_{OSC} = f_{XCLK}$.
0	1	XCLK or internal RC oscillator is divided by 4 and connects to the ADC; $f_{OSC} = f_{XCLK} \div 4$.
1	0	XCLK or internal RC oscillator is divided by 2 and connects to the ADC; $f_{OSC} = f_{XCLK} \div 2$.
1	1	Not allowed

Clock duty cycles of 50% ±10% are recommended.

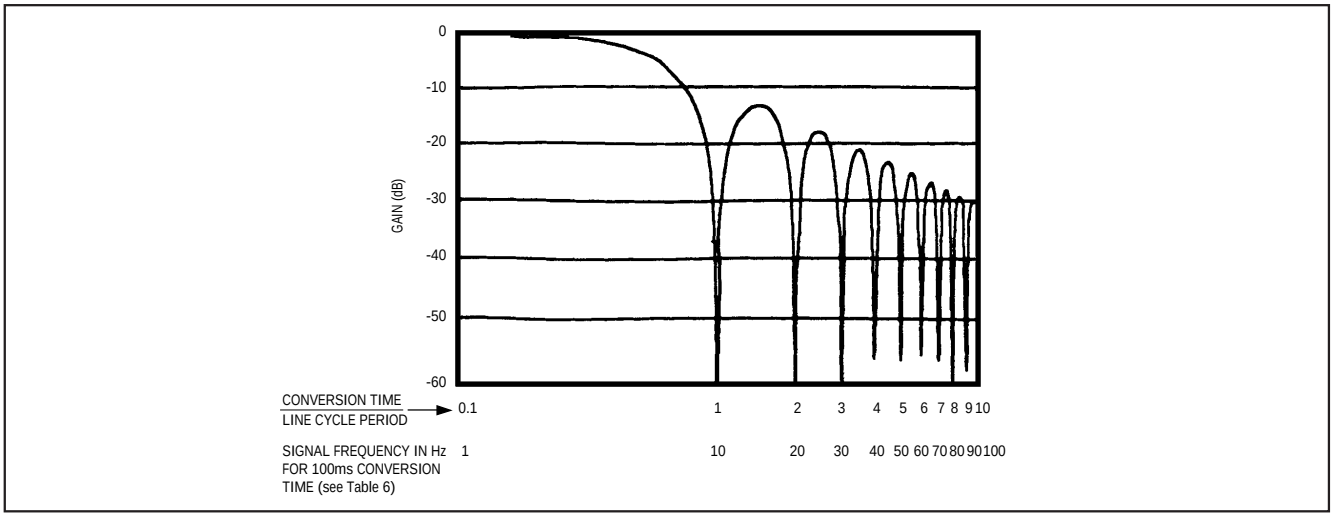


Figure 9. MAX110/MAX111 Noise Rejection Follows SIN(X) / X Function

Selecting the Oversampling Clock Frequency

Choose the oversampling frequency, f_{OSC}, carefully to achieve the best relative-accuracy performance from the MAX110/MAX111 (see *Typical Operating Characteristics*).

Clock Divider-Ratio Control Bits

Bits 7 and 8 (DV2 and DV4) program the clock-frequency divider network. The divider network sets the frequency ratio between f_{XCLK} (the frequency of the external TTL/CMOS clock or internal RC oscillator) and f_{OSC} (the oversampling frequency used by the ADC). An oversampling clock frequency between 450kHz and 700kHz is optimum for the converter. **Best performance over the extended temperature range is obtained by choosing 1MHz or 1.024MHz with the divide-by-2 option (DV2 = 1) (see the section *Effect of Dither on INL*)**. To determine the converter's accuracy at other clock frequencies, see the *Typical Operating Characteristics* and Table 5.

Effect of Dither on Relative Accuracy

First-order sigma-delta converters require dither for randomizing any systematic tone being generated in the modulator. The frequency of the dither source plays an important role in linearizing the modulator. The ratio of the dither generator's frequency to that of the modulator's oversampling clock can be changed by setting the DV2/DV4 bits. The XCLK clock is directly used by the dither generator while the DV2/DV4 bits reduce the oversampling clock by a ratio of 2 or 4. Over the commercial temperature range, any ratio (i.e., 1, 2, or 4) between the dither frequency and the oversampling clock frequency can be used for best performance. Over the extended and military temperature ranges, the ratio of 2 or 4 gives the best performance. See the *Typical Operating Characteristics* to observe the effect of the clock divider on the converter's linearity.

50Hz/60Hz Line Frequency Rejection

High rejection of 50Hz or 60Hz is obtained by using an oversampling clock frequency and a clock-cycles/conversion setting so the conversion time equals an integral number of line cycles, as in the following equation:

$$f_{OSC} = f_{LINE} \times m / n$$

where f_{OSC} is the oversampling clock frequency, f_{LINE} = 50Hz or 60Hz, m is the number of clock cycles per conversion (see Table 4), and n is the number of line cycles averaged every conversion.

This noise rejection is inherent in integrating and sigma-delta ADCs, and follows a SIN(X) / X function (Figure 9). Notches in this function represent extremely high rejection, and correspond to frequencies with an integral number of cycles in the MAX110/MAX111's selected conversion time.

The shortest conversion time resulting in maximum simultaneous rejection of both 60Hz and 50Hz line frequencies is 100ms. When using the MAX111, use a 200ms conversion time for maximum 60Hz and 50Hz rejection **and** optimum performance. For either device, select the appropriate oversampling clock frequency and either an 81,240 or 102,400 clock cycles per conversion (CCPC) ratio. Table 6 suggests the possible configurations.

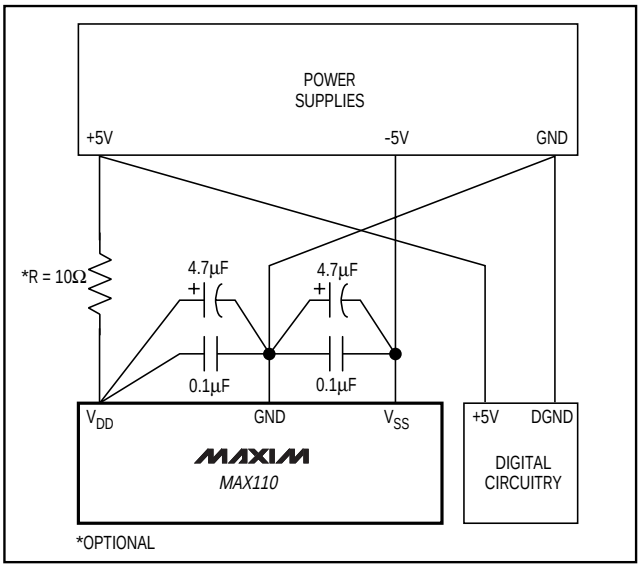


Figure 10a. MAX110 Power-Supply Grounding Connections

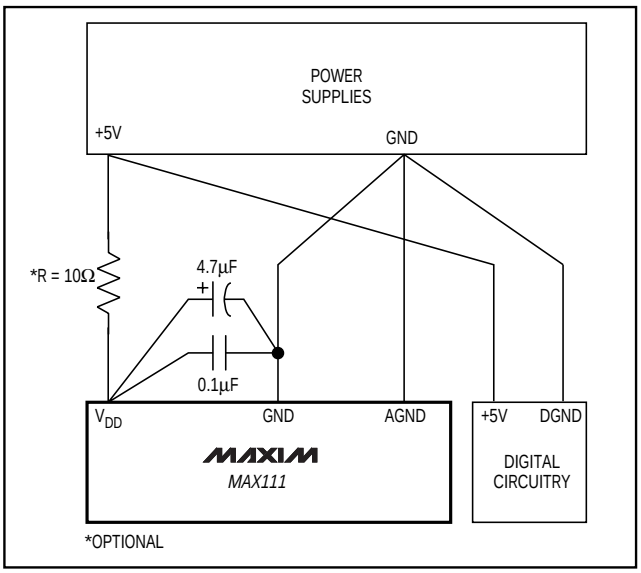


Figure 10b. MAX111 Power-Supply Grounding Connections

A 100ms conversion time cannot be achieved with either 10,240 CCPC or 20,480 CCPC modes because f_{OSC} would be below the minimum 250kHz requirement.

When the gain calibration is performed, the conversion times change approximately 1% to compensate for the modulator's gain error. This slightly degrades the line-frequency rejection, because the corrected conversion time is no longer an exact multiple of the line frequency. Typically, the rejection of 50Hz/60Hz from the converter is 55dB; i.e., if there is 100mV injection at the reference or the analog input pin, it will cause an uncertainty of ±0.006%. If the system has large 50Hz/60Hz noise, the use of internal auto gain calibration is not recommended. Instead, gain calibration should be done off-chip, using numerical computation methods.

If you wish to use a configuration other than those suggested in Table 6, you can accomplish similar 50Hz and 60Hz line-frequency rejection off-chip by averaging several conversions.

Applications Information

Layout, Grounding, Bypassing

For minimal noise, bypass each supply to GND with a 0.1µF capacitor. A ground plane should also be placed under the analog circuitry. To minimize the coupling effects of stray capacitance, keep digital lines as far from analog components and lines as possible. Figure 10 shows the suggested power-supply and ground-plane connections.

Table 6. Suggested XCLK Frequencies to Achieve Maximum Rejection of Both 50Hz/60Hz Line Frequencies

MAX110 ($t_{CONVERT}$ = 100ms)				
DIVIDER RATIO	81,240 CCPC		102,400 CCPC	
	f_{XCLK} (MHz)	RELATIVE ACCURACY (%)	f_{XCLK} (MHz)	RELATIVE ACCURACY (%)
1:1	0.8124	0.025	1.024	0.065
2:1	1.6248	0.018	2.048	0.045
4:1	3.2496	0.016	4.096	0.030

MAX111 ($t_{CONVERT}$ = 200ms)				
DIVIDER RATIO	81,240 CCPC		102,400 CCPC	
	f_{XCLK} (MHz)	RELATIVE ACCURACY (%)	f_{XCLK} (MHz)	RELATIVE ACCURACY (%)
1:1	0.4062	0.030	0.512	0.030
2:1	0.8124	0.025	1.024	0.025
4:1	1.6248	0.022	2.048	0.023

CCPC = Clock Cycles per Conversion

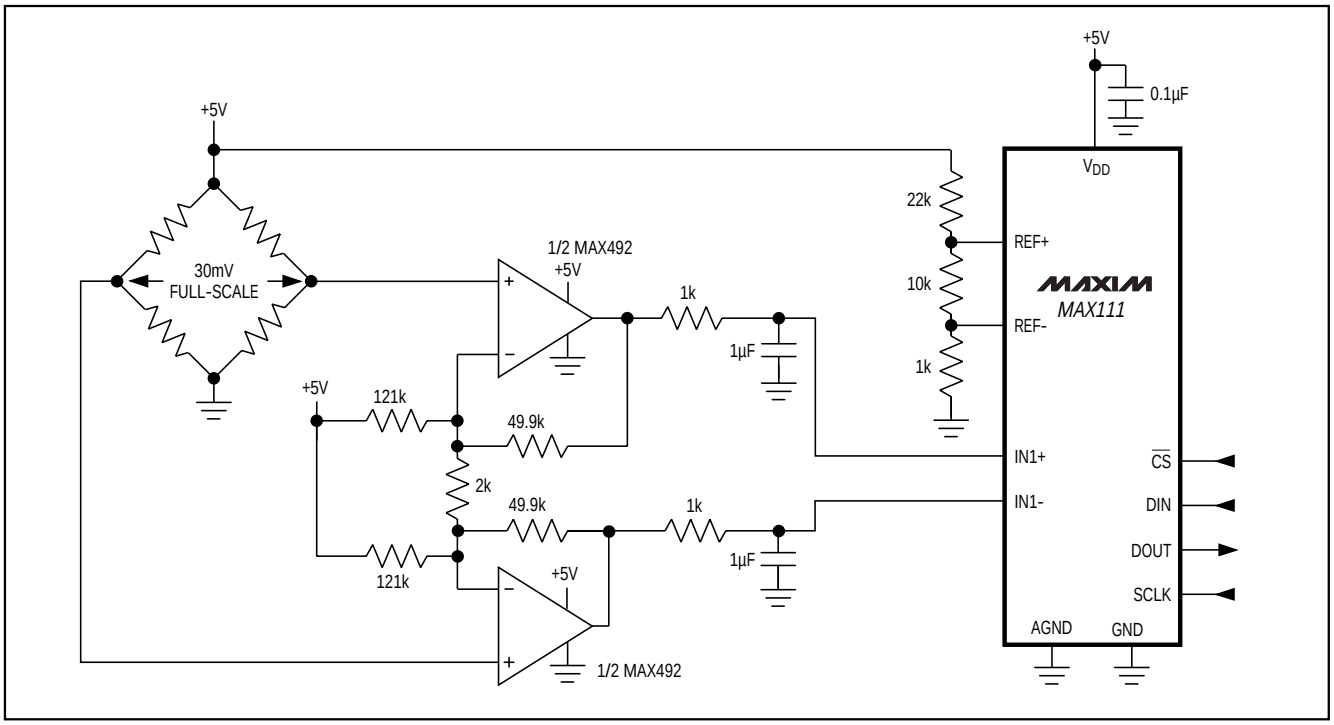


Figure 11. Weigh Scale Application

Capacitive Loading Effects of XCLK in Internal RC-Oscillator Mode

When using the internal RC oscillator, capacitive loading effects on the XCLK pin must be minimized. Stray capacitance causes the V_{DD} power consumption to increase by an amount $p = \frac{1}{2}CV^2f$, where C = stray capacitance, V is the supply voltage, and f is the frequency of the internal RC oscillator.

External Reference

The reference inputs to the ADC are high impedance, allowing both an external voltage reference and ratiometric applications without loading effects. The fully differential analog signal and reference inputs are advantageous for performing ratiometric conversions (Figures 11 and 12). For example, when measuring load cells, the bridge excitation and the ADC reference input both share the same voltage source. As the excitation changes with temperature or voltage, the output of the load cell will change. But since the differential reference voltage also changes, the conversion results remain constant, all else remaining equal.

Weigh Scale Application

The fully differential analog signal and reference inputs make the MAX111 easy to interface to transducers with differential outputs, such as the load cell in Figure 11. Because the ADC input is differential, the load cell only requires differential gain, eliminating the need for the difference amplifier (differential to single-ended converter) of the standard three op-amp instrumentation-amplifier realization.

The 30mV full-scale bridge output is amplified to 2V full-scale and applied to the MAX111 channel-one input. The reference voltage to the ADC is created by a voltage divider connected to the +5V rail. The same 5V provides excitation for the bridge; therefore, as the excitation voltage varies, the reference voltage to the ADC also varies, providing an ADC output that does not depend on the supply voltage.

The two 121kΩ resistors connected to the +5V supplies shift the common-mode voltage from 2.5V (5V/2) to 1.5V to ensure linearity. Match these two resistors to avoid introducing differential offset, or trim the resistor mismatch with a potentiometer. In practice, the scale is “zeroed” or “tared” by storing the average of several conversions in a memory location while the scale is

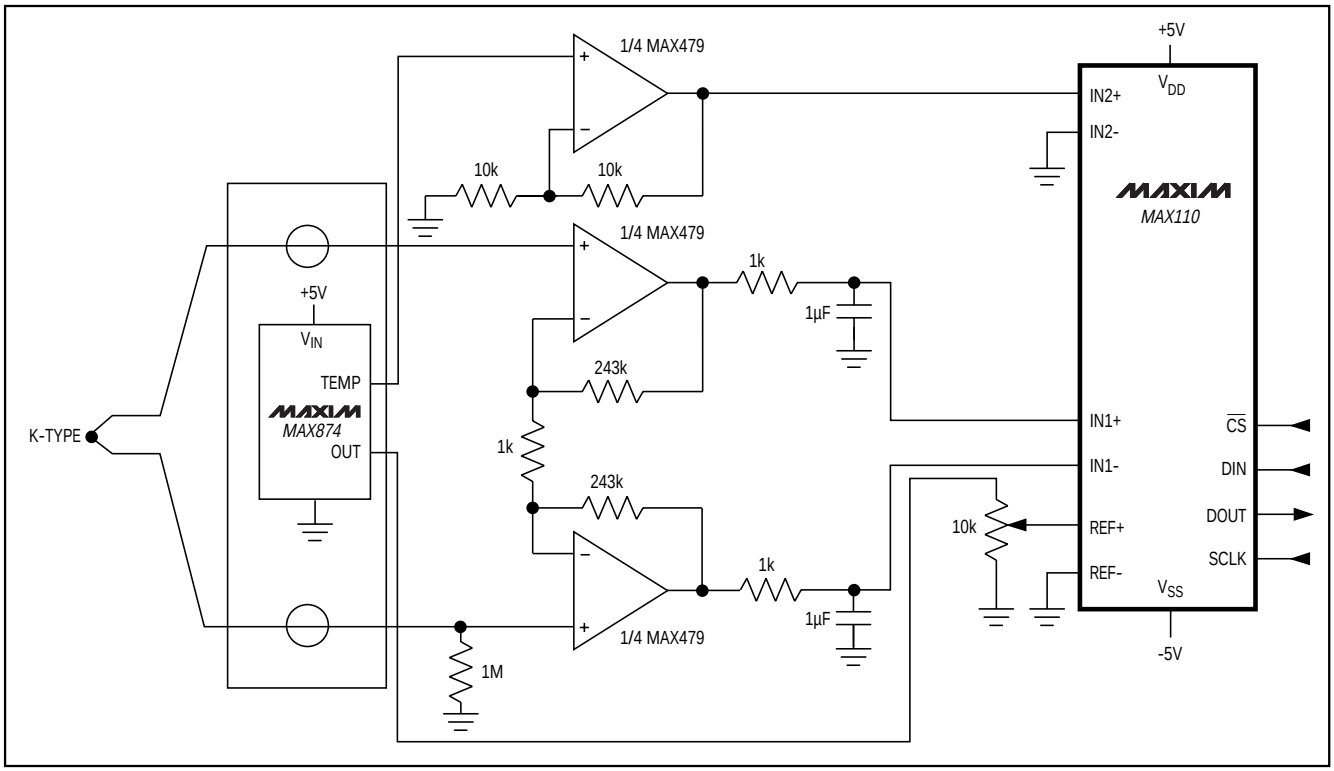


Figure 12. Thermocouple Circuit with Software Compensation

unloaded, and subtracting this value from actual weight measurements. The lowpass filtering action of the MAX111's sigma-delta converter helps minimize noise. The resolution of the weigh scale can be further increased by averaging several conversions.

Thermocouple Circuit with Software Compensation

A thermocouple is created by the junction of dissimilar metals, and generates a voltage proportional to temperature (Seebeck voltage), making it useful for temperature-measurement instruments. When a thermocouple probe is connected to a measurement instrument, other thermoelectric potentials are created between the alloys of the probe and the copper connectors of the instrument. These potentials introduce a temperature-dependent error that must be subtracted from the temperature measurement to obtain an accurate result. According to the law of intermediate metals, the junction of the thermocouple-probe alloys with the copper of the instrument junction block can be treated as another thermocouple of the same type. The voltage measured by the instrument can be expressed as:

$$V = \alpha(T1 - T_{REF})$$

where α is the Seebeck constant for the type of thermocouple, T1 is the temperature being measured, and T_{REF} is the temperature of the junction block. Although one method to obtain T_{REF} is to force the junction block to a known temperature (0°C), a more popular approach is to measure T_{REF} directly using a thermistor or PN junction voltage.

The circuit in Figure 12 shows a k-type thermocouple going through a 54dB gain stage to channel 1 of the MAX110. A MAX874 voltage reference provides both the 3V reference voltage and reference junction temperature information to the MAX110. Armed with the temperature information provided by the MAX874, the thermocouple voltage created at the junction block can be subtracted out in software. The TEMP output of the MAX874 is nominally 690mV at room temperature, and increases with temperature at about 2.3mV/°C. Place the MAX874 as close as possible to the terminal block, and ensure good thermal contact between them. This circuit employs a common k-type thermocouple and, with the component values shown, can indicate temperatures in the range of -150°C to +125°C.

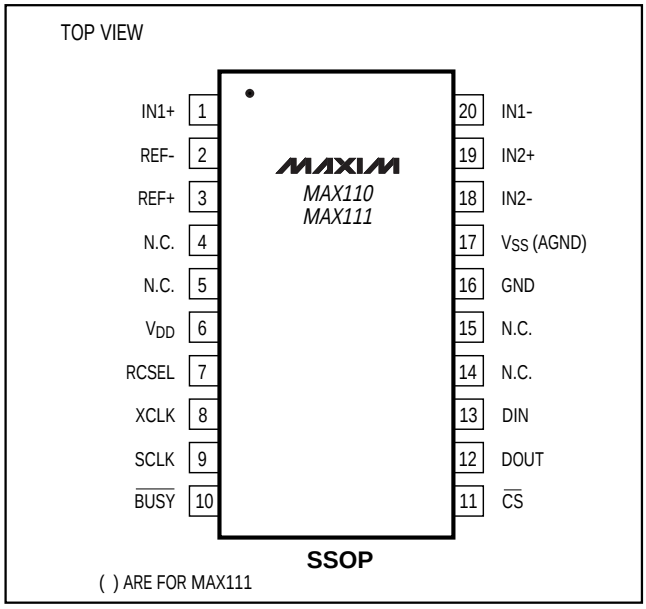
Low-Cost, 2-Channel, ±14-Bit Serial ADCs

_Ordering Information (continued)

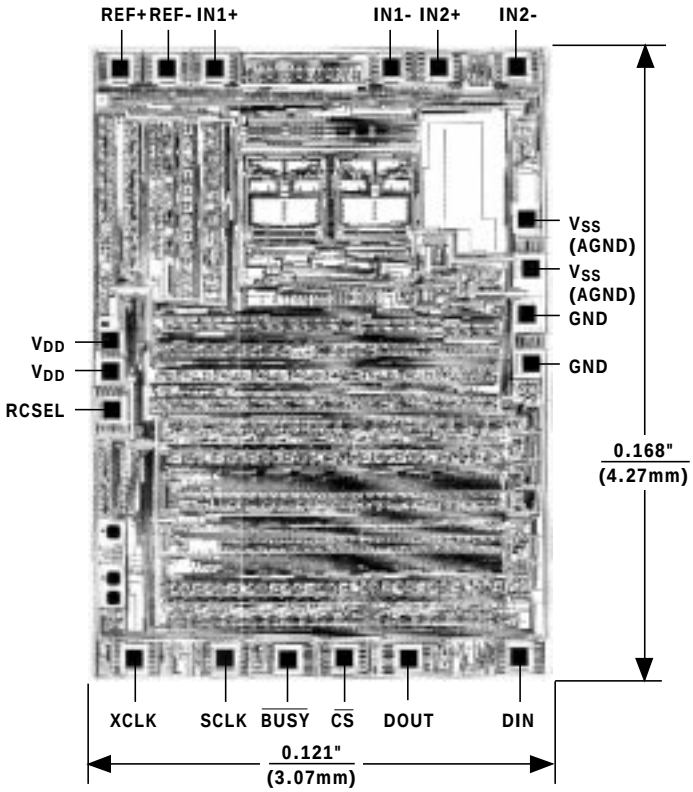
PART	TEMP. RANGE	PIN-PACKAGE	INL(%)
MAX110AEPE	-40°C to +85°C	16 Plastic DIP	±0.03
MAX110BEPE	-40°C to +85°C	16 Plastic DIP	±0.05
MAX110AEWE	-40°C to +85°C	16 Wide SO	±0.03
MAX110BEWE	-40°C to +85°C	16 Wide SO	±0.05
MAX110AEAP	-40°C to +85°C	20 SSOP	±0.03
MAX110BEAP	-40°C to +85°C	20 SSOP	±0.05
MAX110BMJE	-55°C to +125°C	16 CERDIP**	±0.05
MAX111ACPE	0°C to +70°C	16 Plastic DIP	±0.03
MAX111BCPE	0°C to +70°C	16 Plastic DIP	±0.05
MAX111ACWE	0°C to +70°C	16 Wide SO	±0.03
MAX111BCWE	0°C to +70°C	16 Wide SO	±0.05
MAX111ACAP	0°C to +70°C	20 SSOP	±0.03
MAX111BCAP	0°C to +70°C	20 SSOP	±0.05
MAX111BC/D	0°C to +70°C	Dice*	±0.05
MAX111AEPE	-40°C to +85°C	16 Plastic DIP	±0.03
MAX111BEPE	-40°C to +85°C	16 Plastic DIP	±0.05
MAX111AEWE	-40°C to +85°C	16 Wide SO	±0.03
MAX111BEWE	-40°C to +85°C	16 Wide SO	±0.05
MAX111AEAP	-40°C to +85°C	20 SSOP	±0.03
MAX111BEAP	-40°C to +85°C	20 SSOP	±0.05
MAX111BMJE	-55°C to +125°C	16 CERDIP**	±0.05

* *Contact factory for dice specifications.*
** *Contact factory for availability.*

___Pin Configurations (continued)



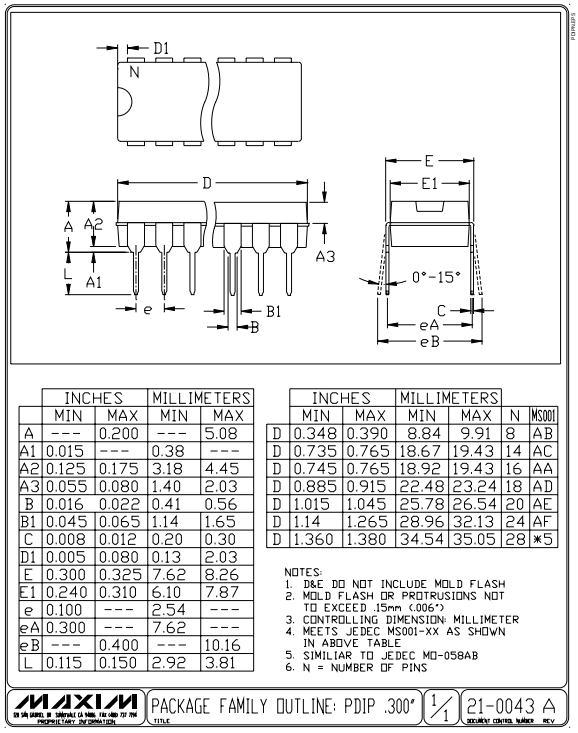
_____Chip Topography



( ) ARE FOR MAX111

TRANSISTOR COUNT: 5849
SUBSTRATE CONNECTED TO V_{DD}

Package Information

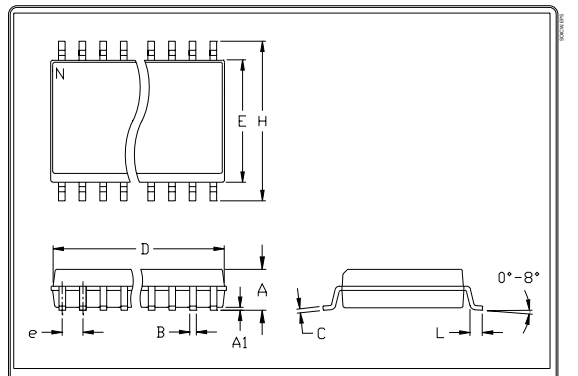


	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	---	0.200	---	5.08
A1	0.015	---	0.38	---
A2	0.125	0.175	3.18	4.45
A3	0.055	0.080	1.40	2.03
B	0.016	0.022	0.41	0.56
B1	0.045	0.065	1.14	1.65
C	0.008	0.012	0.20	0.30
D1	0.005	0.080	0.13	2.03
E	0.300	0.325	7.62	8.26
E1	0.240	0.310	6.10	7.87
e	0.100	---	2.54	---
eA	0.300	---	7.62	---
eB	---	0.400	---	10.16
L	0.115	0.150	2.92	3.81

	INCHES		MILLIMETERS			
	MIN	MAX	MIN	MAX	N	MS001
D	0.348	0.390	8.84	9.91	8	AB
D	0.735	0.765	18.67	19.43	14	AC
D	0.745	0.765	18.92	19.43	16	AA
D	0.885	0.915	22.48	23.24	18	AD
D	1.015	1.045	25.78	26.54	20	AE
D	1.14	1.265	28.96	32.13	24	AF
D	1.360	1.380	34.54	35.05	28	*5

NOTES:
1. D&E DO NOT INCLUDE MOLD FLASH
2. MOLD FLASH OR PROTRUSIONS NOT TO EXCEED .15mm (.006")
3. CONTROLLING DIMENSION: MILLIMETER
4. MEETS JEDEC MS001-XX AS SHOWN IN ABOVE TABLE
5. SIMILIAR TO JEDEC MO-058AB
6. N = NUMBER OF PINS

MAXIM | PROPRIETARY INFORMATION | PACKAGE FAMILY OUTLINE: PDIP .300" | 1/1 | 21-0043 A



	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.093	0.104	2.35	2.65
A1	0.004	0.012	0.10	0.30
B	0.014	0.019	0.35	0.49
C	0.009	0.013	0.23	0.32
e	0.050		1.27	
E	0.291	0.299	7.40	7.60
H	0.394	0.419	10.00	10.65
h	0.010	0.030	0.25	0.75
L	0.016	0.050	0.40	1.27

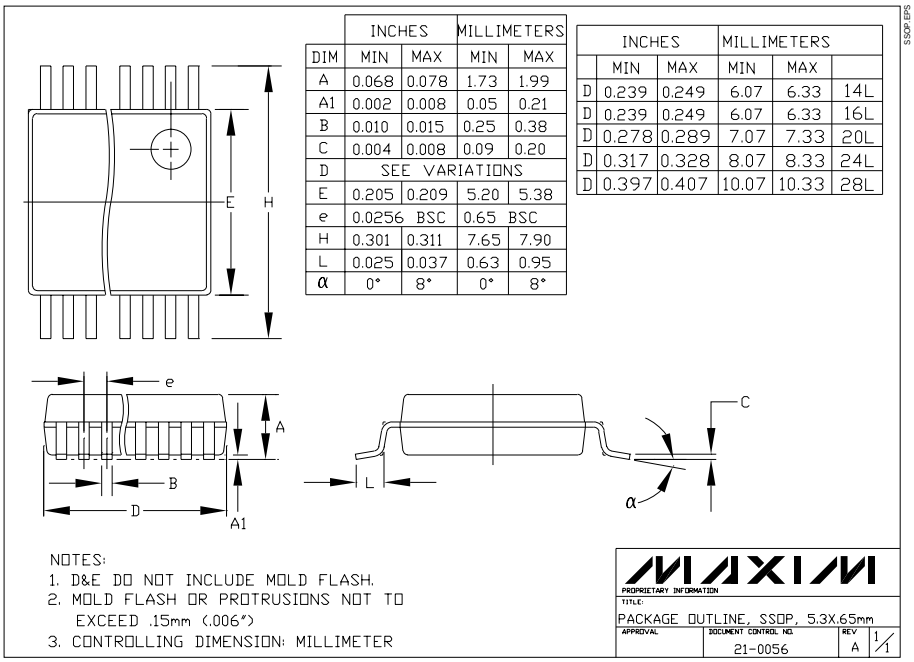
	INCHES		MILLIMETERS			
	MIN	MAX	MIN	MAX	N	MS013
D	0.398	0.413	10.10	10.50	16	AA
D	0.447	0.463	11.35	11.75	18	AB
D	0.496	0.512	12.60	13.00	20	AC
D	0.598	0.614	15.20	15.60	24	AD
D	0.697	0.713	17.70	18.10	28	AE

NOTES:
1. D&E DO NOT INCLUDE MOLD FLASH
2. MOLD FLASH OR PROTRUSIONS NOT TO EXCEED .15mm (.006")
3. LEADS TO BE COPLANAR WITHIN .102mm (.004")
4. CONTROLLING DIMENSION: MILLIMETER
5. MEETS JEDEC MS013-XX AS SHOWN IN ABOVE TABLE
6. N = NUMBER OF PINS

MAXIM | PROPRIETARY INFORMATION | PACKAGE FAMILY OUTLINE: SOIC .300" | 1/1 | 21-0042 A

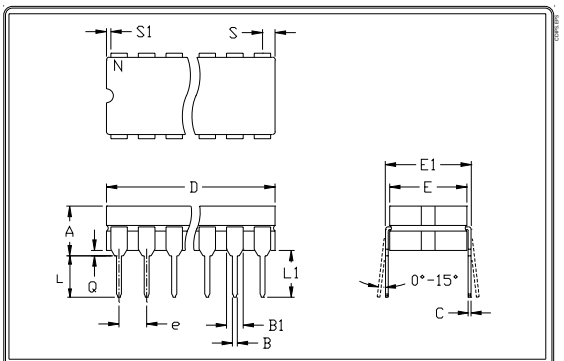
Low-Cost, 2-Channel, ±14-Bit Serial ADCs

Package Information (continued)



DIM	INCHES MIN	INCHES MAX	MILLIMETERS MIN	MILLIMETERS MAX
A	0.068	0.078	1.73	1.99
A1	0.002	0.008	0.05	0.21
B	0.010	0.015	0.25	0.38
C	0.004	0.008	0.09	0.20
D	SEE VARIATIONS			
E	0.205	0.209	5.20	5.38
e	0.0256 BSC		0.65 BSC	
H	0.301	0.311	7.65	7.90
L	0.025	0.037	0.63	0.95
α	0°	8°	0°	8°

	INCHES MIN	INCHES MAX	MILLIMETERS MIN	MILLIMETERS MAX	
D	0.239	0.249	6.07	6.33	14L
D	0.239	0.249	6.07	6.33	16L
D	0.278	0.289	7.07	7.33	20L
D	0.317	0.328	8.07	8.33	24L
D	0.397	0.407	10.07	10.33	28L



	INCHES MIN	INCHES MAX	MILLIMETERS MIN	MILLIMETERS MAX
A	---	0.200	---	5.08
B	0.014	0.023	0.36	0.58
B1	0.038	0.065	0.97	1.65
C	0.008	0.015	0.20	0.38
E	0.220	0.310	5.59	7.87
E1	0.290	0.320	7.37	8.13
e	0.100		2.54	
L	0.125	0.200	3.18	5.08
L1	0.150	---	0.00	---
Q	0.015	0.070	0.38	1.78
S	---	0.098	---	2.49
S1	0.005	---	0.13	---

	INCHES MIN	INCHES MAX	MILLIMETERS MIN	MILLIMETERS MAX	N	CASE
D	---	0.405	---	10.29	8	P:D4
D	---	0.785	---	19.94	14	C:D1
D	---	0.840	---	21.34	16	E:D2
D	---	0.960	---	24.38	18	V:D6
D	---	1.060	---	26.92	20	R:D8
D	---	1.280	---	32.51	24	L:D9

Mouser Electronics

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