

5V, Low-Power, Parallel-Input, Voltage-Output, 10-Bit DAC

ABSOLUTE MAXIMUM RATINGS

V _{DD} to DGND and V _{DD} to AGND	-0.3V, +6V
V _{SS} to DGND and V _{SS} to AGND	-6V, +0.3V
V _{DD} to V _{SS}	-0.3V, +12V
AGND to DGND	-0.3V, +0.3V
REFGND to AGND	-0.3V, (V _{DD} + 0.3V)
Digital Input Voltage to DGND	-0.3V, (V _{DD} + 0.3V)
REFIN	(V _{SS} - 0.3V), (V _{DD} + 0.3V)
REFOUT	(V _{SS} - 0.3V), (V _{DD} + 0.3V)
REFOUT to REFGND	-0.3V, (V _{DD} + 0.3V)
RFB	(V _{SS} - 0.3V), (V _{DD} + 0.3V)
ROFS	(V _{SS} - 0.3V), (V _{DD} + 0.3V)

VOUT to AGND (Note 1)	V _{SS} , V _{DD}
Continuous Current, Any Input	±20mA
Continuous Power Dissipation (T _A = +70°C)	
Narrow Plastic DIP (derate 13.33mW/°C above +70°C)	1067mW
Wide SO (derate 11.76mW/°C above +70°C)	941mW
SSOP (derate 8.00mW/°C above +70°C)	640mW
Operating Temperature Ranges	
MAX503C_G	0°C to +70°C
MAX503E_G	-40°C to +85°C
Storage Temperature Range	-65°C to +165°C
Lead Temperature (soldering, 10sec)	+300°C

Note 1: The output may be shorted to V_{DD}, V_{SS}, DGND, or AGND if the continuous package power dissipation and current ratings are not exceeded. Typical short-circuit currents are 20mA.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS—Single +5V Supply

(V_{DD} = 5V, V_{SS} = 0V, AGND = DGND = REFGND = 0V, REFIN = 2.048V (external), RFB = ROFS = VOUT, C_{REFOUT} = 33μF, R_L = 10kΩ, C_L = 100pF, T_A = T_{MIN} to T_{MAX}, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
STATIC PERFORMANCE						
Resolution	N		10			Bits
Relative Accuracy	INL	(Note 2)			±0.5	LSB
Differential Nonlinearity	DNL	Guaranteed monotonic			±1	LSB
Unipolar Offset Error	V _{OS}		0	0.25	3	LSB
Unipolar Offset Temperature Coefficient	TCV _{OS}			3		ppm/°C
Unipolar Offset-Error Supply Rejection	PSRR	4.5V ≤ V _{DD} ≤ 5.5V		0.1		LSB/V
Gain Error (Note 2)	GE	DAC latch = all 1s, VOUT < V _{DD} - 0.4V (Note 2)			±1	LSB
Gain-Error Temperature Coefficient				1		ppm/°C
Gain-Error Power-Supply Rejection	PSRR	4.5V ≤ V _{DD} ≤ 5.5V		0.1		LSB/V
DAC VOLTAGE OUTPUT (VOUT)						
Output Voltage Range			0	V _{DD} - 0.4		V
Resistive Load		VOUT = 2V, load regulation ≤ ±0.5LSB	2			kΩ
DC Output Impedance				0.2		Ω
Short-Circuit Current	I _{SC}			12		mA
REFERENCE INPUT (REFIN)						
Reference Input Range			0	V _{DD} - 2		V
Reference Input Resistance		Code dependent, minimum at code 0101...	40			kΩ
Reference Input Capacitance		Code dependent (Note 3)	10	50		pF
AC Feedthrough		(Note 4)		-80		dB

5V, Low-Power, Parallel-Input, Voltage-Output, 10-Bit DAC

MAX503

ELECTRICAL CHARACTERISTICS—Single +5V Supply (continued)

($V_{DD} = 5V$, $V_{SS} = 0V$, $AGND = DGND = REFGND = 0V$, $REFIN = 2.048V$ (external), $RFB = ROFS = VOUT$, $C_{REFOUT} = 33\mu F$, $R_L = 10k\Omega$, $C_L = 100pF$, $T_A = T_{MIN}$ to T_{MAX} , unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
REFERENCE OUTPUT (REFOUT)						
Reference Tolerance	V_{REFOUT}	$T_A = +25^\circ C$	2.024	2.048	2.072	V
		MAX503C	2.015		2.081	
		MAX503E	2.011		2.085	
Reference Output Resistance	R_{REFOUT}	(Note 5)			2	Ω
Power-Supply Rejection Ratio	PSRR	$4.5V \leq V_{DD} \leq 5.5V$		200		$\mu V/V$
Noise Voltage	e_n	0.1Hz to 10kHz		400		$\mu Vp-p$
Temperature Coefficient				30		ppm/ $^\circ C$
Required External Capacitor	C_{REFOUT}		3.3			μF
DYNAMIC PERFORMANCE						
Voltage Output Slew Rate		$T_A = +25^\circ C$	0.15	0.25		V/ μs
Voltage Output Settling Time		$T_o \pm 0.5LSB$, $VOUT = 2V$		25		μs
Digital Feedthrough		$\overline{WR} = V_{DD}$, digital inputs all 1s to all 0s		5		nV-s
Signal-to-Noise Plus Distortion Ratio	SINAD	Unity gain (Note 4)		68		dB
		Gain = 2 (Note 4)		68		
DIGITAL INPUTS (S0, S1, D0–D9, LDAC, CLR, CS, WR, A0, A1)						
Logic High Input	V_{IH}		2.4			V
Logic Low Input	V_{IL}				0.8	V
Digital Leakage Current		$V_{IN} = 0V$ or V_{DD}			± 1	μA
Digital Input Capacitance				8		pF
POWER SUPPLIES						
Positive Supply-Voltage Range	V_{DD}		4.5		5.5	V
Positive Supply Current	I_{DD}	Outputs unloaded, all digital inputs = 0V or V_{DD}		250	400	μA
SWITCHING CHARACTERISTICS						
Address to \overline{WR} Setup	t_{AWS}		5			ns
Address to \overline{WR} Hold	t_{AWH}		5			ns
\overline{CS} to \overline{WR} Setup	t_{CWS}		0			ns
\overline{CS} to \overline{WR} Hold	t_{CWH}		0			ns
Data to \overline{WR} Setup	t_{DS}		45			ns
Data to \overline{WR} Hold	t_{DH}		0			ns
\overline{WR} Pulse Width	t_{WR}		45			ns
LDAC Pulse Width	t_{LDAC}		45			ns
\overline{CLR} Pulse Width	t_{CLR}		45			ns
Internal Power-On Reset Pulse Width	t_{POR}	(Note 3)		1.3	10	μs

5V, Low-Power, Parallel-Input, Voltage-Output, 10-Bit DAC

ELECTRICAL CHARACTERISTICS—Dual $\pm 5V$ Supplies

($V_{DD} = 5V$, $V_{SS} = -5V$, $AGND = DGND = REF_{GND} = 0V$, $REF_{IN} = 2.048V$ (external), $R_{FB} = ROFS = V_{OUT}$, $C_{REFOUT} = 33\mu F$, $R_L = 10k\Omega$, $C_L = 100pF$, $T_A = T_{MIN}$ to T_{MAX} , unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
STATIC PERFORMANCE						
Resolution	N		10			Bits
Relative Accuracy	INL				+0.5	LSB
Differential Nonlinearity	DNL	Guaranteed monotonic			± 1	LSB
Bipolar Offset Error	V_{OS}				± 3	LSB
Bipolar Offset Temperature Coefficient	TCV_{OS}			3		ppm/ $^{\circ}C$
Bipolar Offset-Error Power-Supply Rejection	PSRR	$4.5V \leq V_{DD} \leq 5.5V$, $-5.5V \leq V_{SS} \leq -4.5V$		0.1		LSB/V
Gain Error					± 1	LSB
Gain-Error Temperature Coefficient	TC			1		ppm/ $^{\circ}C$
Gain-Error Power-Supply Rejection	PSRR	$4.5V \leq V_{DD} \leq 5.5V$, $-5.5V \leq V_{SS} \leq -4.5V$		0.1		LSB/V
DAC VOLTAGE OUTPUT (V_{OUT})						
Output Voltage Range			$V_{SS} + 0.4$	$V_{DD} - 0.4$		V
Resistive Load		$V_{OUT} = 2V$, load regulation $\leq \pm 0.5LSB$	2			k Ω
DC Output Impedance				0.2		Ω
Short-Circuit Current	I_{SC}			20		mA
REFERENCE INPUT (REF_{IN})						
Reference Input Range			$V_{SS} + 2$	$V_{DD} - 2$		V
Reference Input Resistance		Code dependent, minimum at code 0101...	40			k Ω
Reference Input Capacitance		Code dependent (Note 3)	10		50	pF
AC Feedthrough		(Note 4)		-80		dB
REFERENCE OUTPUT (REF_{OUT}) —Specifications are identical to those under Single +5V Supply						
DYNAMIC PERFORMANCE —Specifications are identical to those under Single +5V Supply						
DIGITAL INPUTS (S₀, S₁, D₀–D₉, LDAC, CLR, CS, WR, A₀, A₁) —Specifications are identical to those under Single +5V Supply						
POWER SUPPLIES						
Positive Supply Voltage	V_{DD}		4.5		5.5	V
Negative Supply Voltage	V_{SS}		-5.5		0	V
Positive Supply Current	I_{DD}	Outputs unloaded, all digital inputs = 0V or V_{DD}		250	400	μA
Negative Supply Current	I_{SS}	Outputs unloaded, all digital inputs = 0V or V_{DD}		150	200	μA
SWITCHING CHARACTERISTICS —Specifications are identical to those under Single +5V Supply						

Note 2: In single supply, INL and GE are calculated from code 3 to code 1023 (code excludes S₀ and S₁).

Note 3: Guaranteed by design.

Note 4: REF_{IN} = 1kHz, 2.0Vp-p.

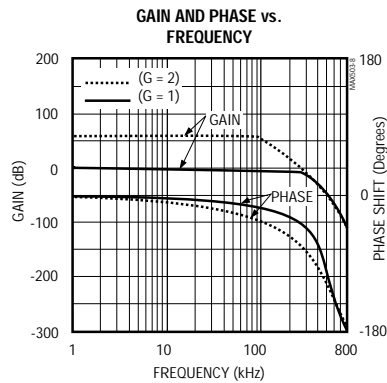
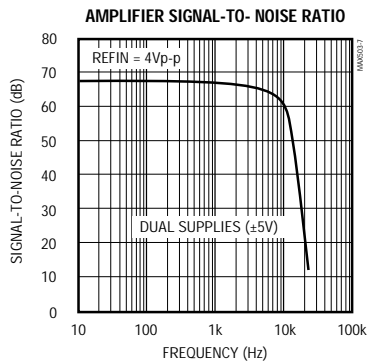
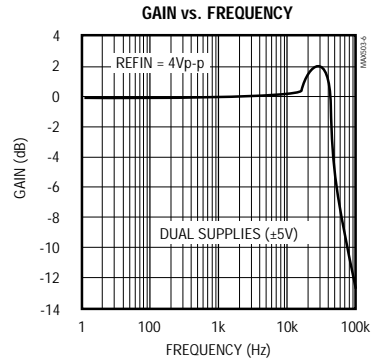
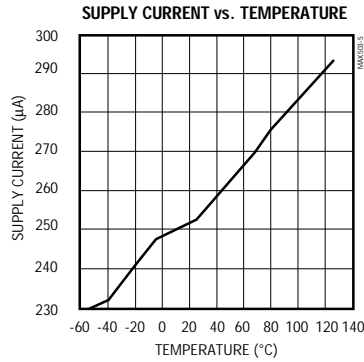
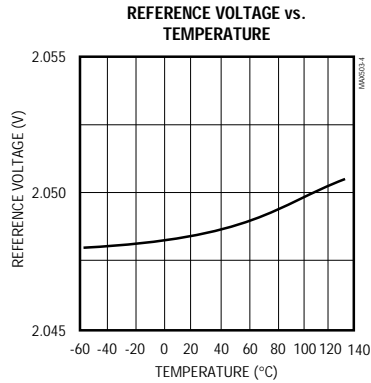
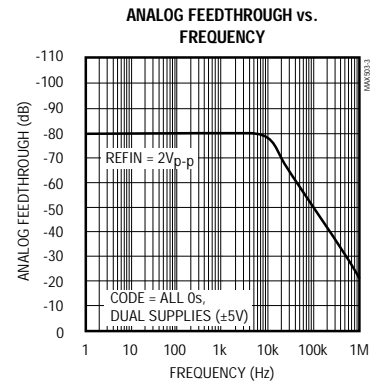
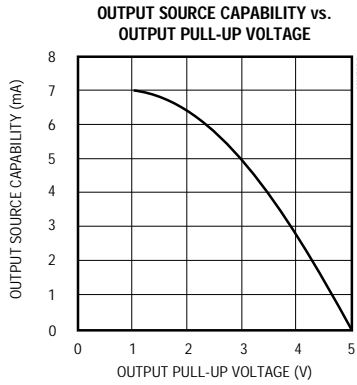
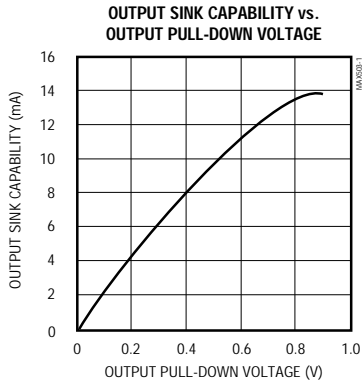
Note 5: Tested at $I_{OUT} = 100\mu A$. The reference can typically source up to 5mA (see *Typical Operating Characteristics*).

5V, Low-Power, Parallel-Input, Voltage-Output, 10-Bit DAC

Typical Operating Characteristics

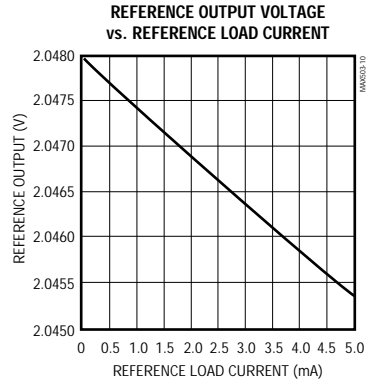
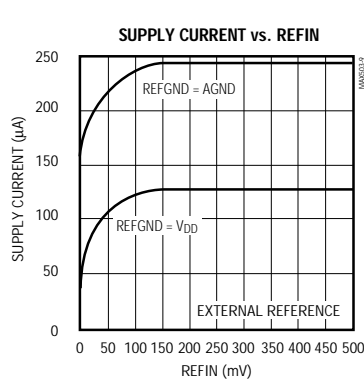
(Single +5V supply, unity gain, code = all 1s, $T_A = +25^\circ\text{C}$, unless otherwise noted.)

MAX503

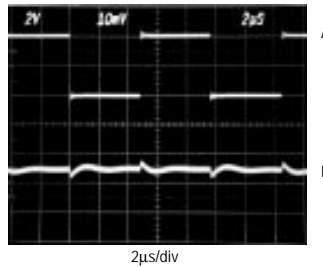


5V, Low-Power, Parallel-Input, Voltage-Output, 10-Bit DAC

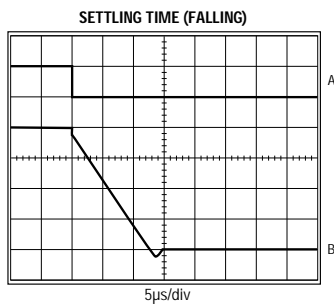
Typical Operating Characteristics (continued)
 (Single +5V supply, unity gain, code = all 1s, $T_A = +25^\circ\text{C}$, unless otherwise noted.)



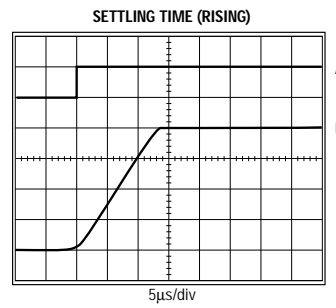
DIGITAL FEEDTHROUGH



2µs/div
 A: S0, S1, D0-D9 = 100kHz, 4Vp-p
 B: VOUT, 10mV/div
 LDAC = CS = HIGH



A: DIGITAL INPUTS FALLING EDGE, 5V/div
 B: VOUT, NO LOAD, 1V/div
 DUAL SUPPLY ($\pm 5\text{V}$)
 LDAC = LOW
 BIPOLAR CONFIGURATION
 $V_{\text{REFIN}} = 2\text{V}$



A: DIGITAL INPUTS RISING EDGE,
 B: VOUT, NO LOAD, 1V/div
 DUAL SUPPLY ($\pm 5\text{V}$)
 LDAC = LOW
 BIPOLAR CONFIGURATION
 $V_{\text{REFIN}} = 2\text{V}$

5V, Low-Power, Parallel-Input, Voltage-Output, 10-Bit DAC

Pin Description

MAX503

PIN	NAME	FUNCTION
1	D7/S1	D7 input when A0 = A1 = 1, or S1 input when A0 = 0 and A1 = 1. Always set S1 to 0.*
2	D8/D0	D8 input when A0 = A1 = 1, or D0 input when A0 = 0 and A1 = 1.*
3	D9/D1	D9 input when A0 = A1 = 1, or D1 input when A0 = 0 and A1 = 1.*
4	D2	D2 Input Data, or tie to S0 and multiplex when A0 = 1 and A1 = 0.*
5	D3	D3 Input Data, or tie to S1 and multiplex when A0 = 1 and A1 = 0.*
6	D4	D4 Input Data, or tie to D0 and multiplex when A0 = 1 and A1 = 0.*
7	D5	D5 Input Data, or tie to D1 and multiplex when A0 = 1 and A1 = 0.*
8	A0	Address Line A0. With A1, used to multiplex 4 of 12 data lines to load low (NBL), middle (NBM), and high (NBH) 4-bit nibbles. (12 bits can also be loaded as 8+4.)
9	A1	Address Line A1. Set A0 = A1 = 0 for NBL and NBM, A0 = 0 and A1 = 1 for NBL, A0 = 1 and A1 = 0 for NBM, or A0 = A1 = 1 for NBH. See Table 2 for complete input latch addressing.
10	\overline{WR}	Write Input (active low). Used with \overline{CS} to load data into the input latch selected by A0 and A1.
11	\overline{CS}	Chip Select (active low). Enables addressing and writing to this chip from common bus lines.
12	DGND	Digital Ground
13	REFIN	Reference Input. Input for the R-2R DAC. Connect an external reference to this pin or a jumper to REFOUT (pin 18) to use the internal 2.048V reference.
14	AGND	Analog Ground
15	\overline{CLR}	Clear (active low). A low on \overline{CLR} resets the DAC latches to all 0s.
16	\overline{LDAC}	Load DAC Input (active low). Driving this asynchronous input low transfers the contents of the input latch to the DAC latch and updates VOUT.
17	REFGND	Reference Ground must be connected to AGND when using the internal reference. Connect to VDD to disable the internal reference and save power.
18	REFOUT	Reference Output. Output of the internal 2.048V reference. Tie to REFIN to drive the R-2R DAC.
19	VSS	Negative Power Supply. Usually ground for single-supply or -5V for dual-supply operation.
20	VOUT	Voltage Output. Op-amp buffered DAC output.
21	RFB	Feedback Pin. Op-amp feedback resistor. Always connect to VOUT.
22	ROFS	Offset Resistor Pin. Connect to VOUT for G = 1, to AGND for G = 2, or to REFIN for bipolar output.
23	VDD	Positive Power Supply (+5V)
24	D6/S0	D6 input when A0 = A1 = 1, or S0 input when A0 = 0 and A1 = 1. Always set S0 to 0.*

* This applies to 4 + 4 + 4 input loading mode. See Table 2 for 8 + 4 input loading mode.

5V, Low-Power, Parallel-Input, Voltage-Output, 10-Bit DAC

MAX503

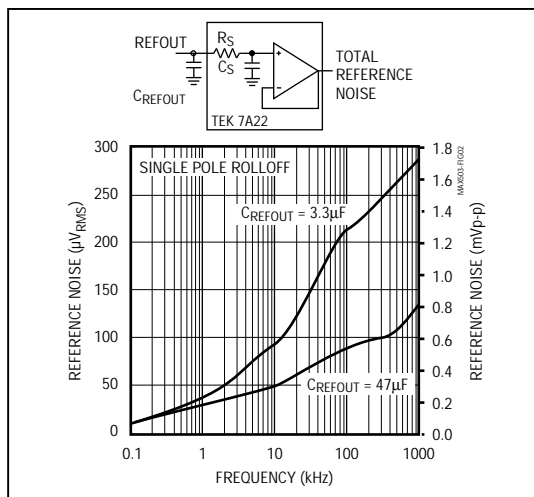


Figure 2. Reference Noise vs. Frequency

Output Buffer

The output amplifier uses a folded cascode input stage and a type AB output stage. Large output devices with low series resistance allow the output to swing to ground in single-supply operation. The output buffer is unity-gain stable. Input offset voltage and supply current are laser trimmed. Settling time is 25µs to 0.01% of final value. The output is short-circuit protected and can drive a 2kΩ load with more than 100pF of load capacitance. The op amp may be placed in unity-gain ($G = 1$), in a gain of two ($G = 2$), or in a bipolar-output mode by using the ROFS and RFB pins. These pins are used to define a DAC output voltage range of 0V to +2.048V, 0V to +4.096V or $\pm 2.048V$, by connecting ROFS to VOUT, GND, or REFIN. RFB is always connected to VOUT. Table 1 summarizes ROFS usage.

Table 1. ROFS Usage

ROFS CONNECTED TO:	DAC OUTPUT RANGE	OP-AMP GAIN
VOUT	0V to 2.048V	$G = 1$
AGND	0V to 4.096V	$G = 2$
REFIN	-2.048V to +2.048V	Bipolar

Note: Assumes RFB = VOUT and REFIN = REFOUT = 2.048V

External Reference

An external reference in the range ($V_{SS} + 2V$) to ($V_{DD} - 2V$) may be used with the MAX503 in dual-supply, unity-gain operation. In single-supply, unity-gain operation, the reference must be positive and may not exceed ($V_{DD} - 2V$). The reference voltage determines the DAC's full-scale output.

If an upgrade to the internal reference is required, the 2.5V MAX873A is ideal: $\pm 15mV$ initial accuracy, 7ppm/°C (max) temperature coefficient.

Power-On Reset

An internal power-on reset (POR) circuit forces the DAC register to reset to all 0s when V_{DD} is first applied. The POR pulse is typically 1.3µs; however, it may take 2ms for the internal reference to charge its large filter capacitor and settle to its trimmed value.

In addition to POR, a clear (\overline{CLR}) pin, when held low, sets the DAC register to all 0s. CLR operates asynchronously and independently from chip select (\overline{CS}). With the DAC input at all 0s, the op-amp output is at zero for unity-gain and $G = 2$ configurations, but it is at $-V_{REF}$ for the bipolar configuration.

Shutdown Mode

The MAX503 is designed for low power consumption. Understanding the circuit allows power consumption management for maximum efficiency. In single-supply mode ($V_{DD} = +5V$, $V_{SS} = GND$) the initial supply current is typically only 160µA, including the reference, op amp, and DAC. This low current occurs when the power-on reset circuit clears the DAC to all 0s and forces the op-amp output to zero (unipolar mode only). See the Supply Current vs. REFIN graph in the *Typical Operating Characteristics*. Under this condition, there is no internal load on the reference (DAC = all 0s, REFIN is open circuit) and the op amp operates at its minimum quiescent current. The CLR signal resets the MAX503 to these same conditions and can be used to control a power-saving mode when the DAC is not being used by the system.

5V, Low-Power, Parallel-Input, Voltage-Output, 10-Bit DAC

MAX503

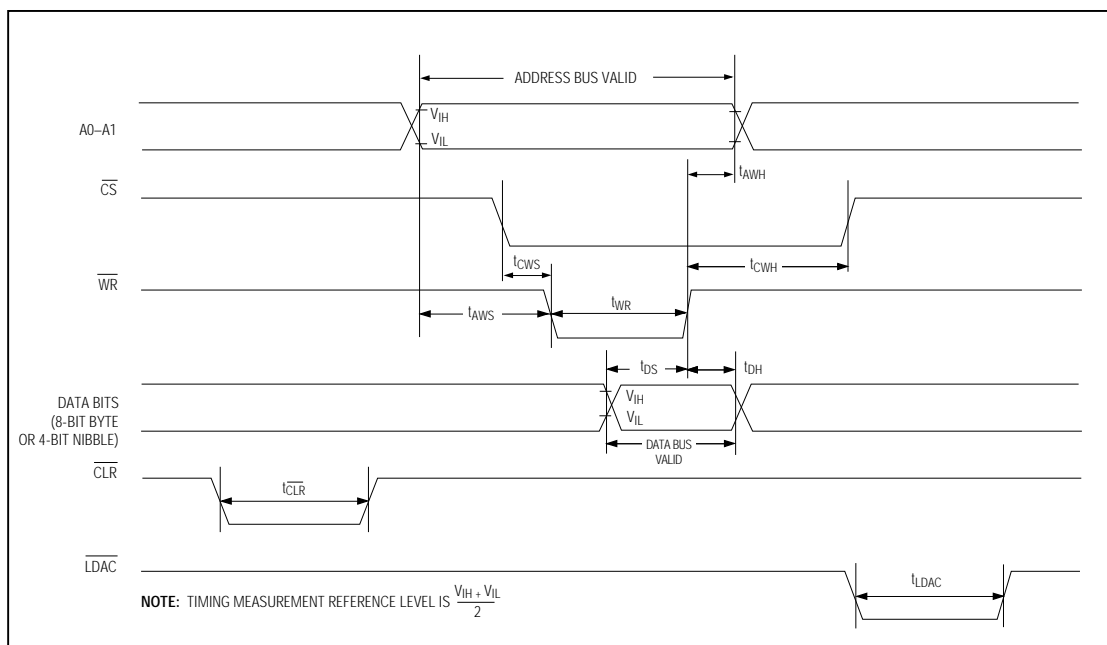


Figure 4. MAX503 Write-Cycle Timing Diagram

A small error voltage is added to the reference output by the reference current flowing through the N-channel pull-down transistor. The switch's on resistance should be less than 5Ω . A typical reference current of $100\mu\text{A}$ would add 0.5mV to REFOUT. Since the reference current and on resistance increase with temperature, the overall temperature coefficient will degrade slightly.

As data is loaded into the DAC and the output moves above GND, the op-amp quiescent current increases to its nominal value and the total operating current averages $250\mu\text{A}$. Using dual supplies ($\pm 5\text{V}$), the op amp is fully biased continuously, and the V_{DD} supply current is more constant at $250\mu\text{A}$. The V_{SS} current is typically $150\mu\text{A}$.

The MAX503 logic inputs are compatible with TTL and CMOS logic levels. However, to achieve the lowest power dissipation, drive the digital inputs with rail-to-rail CMOS logic. With TTL logic levels, the power requirement increases by a factor of approximately 2.

Parallel Logic Interface

In order to provide hardware and software compatibility with the 12-bit MAX530, the MAX503 employs a 12-bit digital interface. As shown in Figure 3, there is actually a 12-bit input latch, and therefore 12 bits of data should be written. The two least significant bits (S1 and S0) are sub-LSB, and must always be 0s. Designed to interface with 4-bit, 8-bit, and 16-bit microprocessors (μPs), the MAX503 uses 8 data pins and double-buffered logic inputs to load data as $4 + 4 + 4$ or $8 + 4$. The 12-bit DAC latch is updated simultaneously through the control signal LDAC. Signals A0, A1, WR, and CS select which input latches to update. The 12-bit data is broken down into nibbles (NB): NBL is the enable signal for the lowest 4 bits (S0, S1, D0, D1), NBM is the enable for the middle 4 bits, and NBH is the enable for the highest and most significant 4 bits. Table 2 lists the address decoding scheme.

Refer to Figure 4 for the MAX503 write-cycle timing diagram.

5V, Low-Power, Parallel-Input, Voltage-Output, 10-Bit DAC

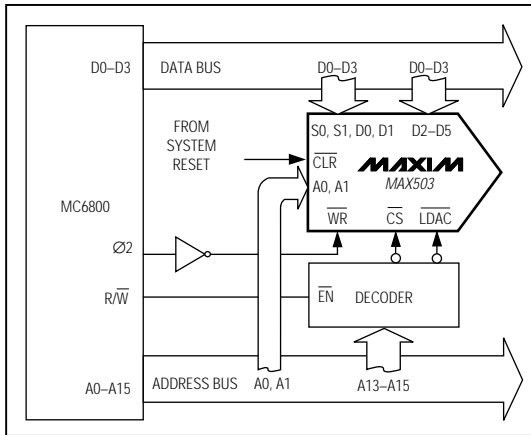


Figure 5. 4-Bit μ P Interface

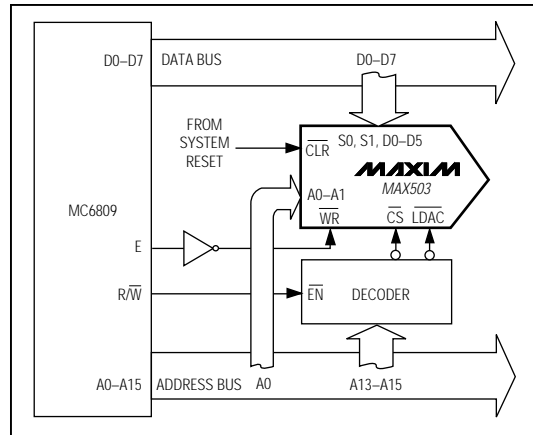


Figure 7. 8-Bit and 16-Bit μ P Interface

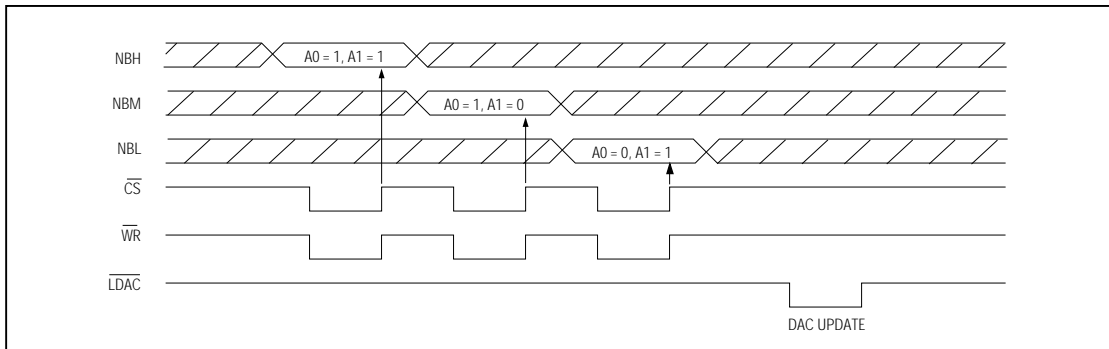


Figure 6. 4-Bit μ P Timing Sequence

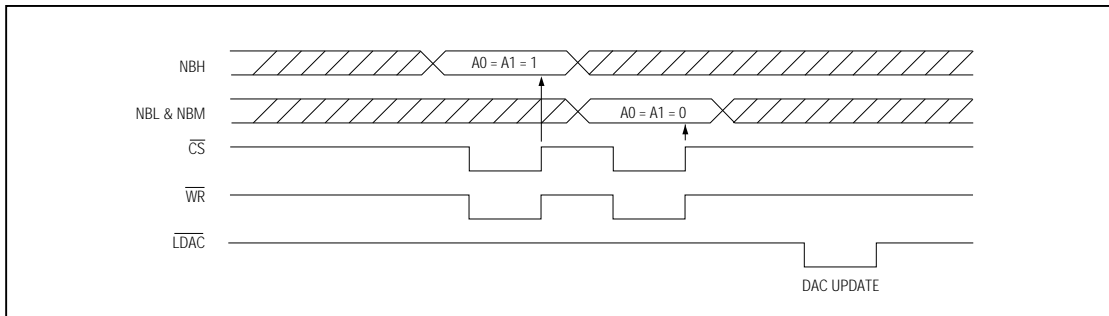


Figure 8a. 8-Bit and 16-Bit μ P Timing Sequence Using LDAC

5V, Low-Power, Parallel-Input, Voltage-Output, 10-Bit DAC

MAX503

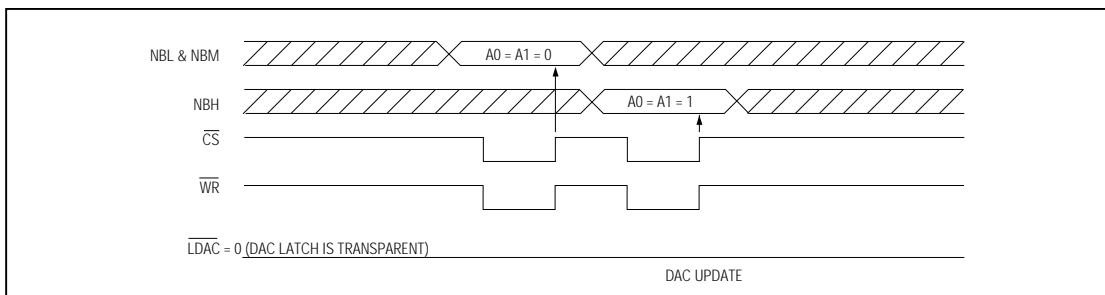


Figure 8b. 8-Bit and 16-Bit μP Timing Sequence with $\overline{LDAC} = 0$

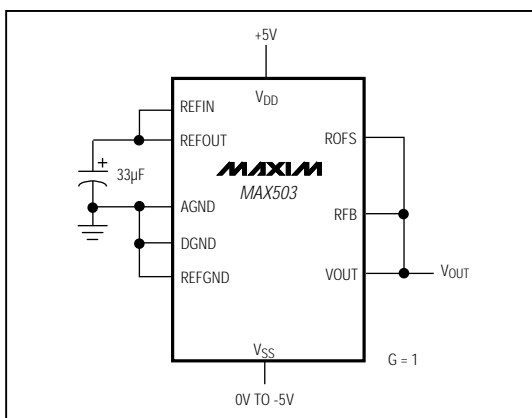


Figure 9. Unipolar Configuration (0V to +2.048V Output)

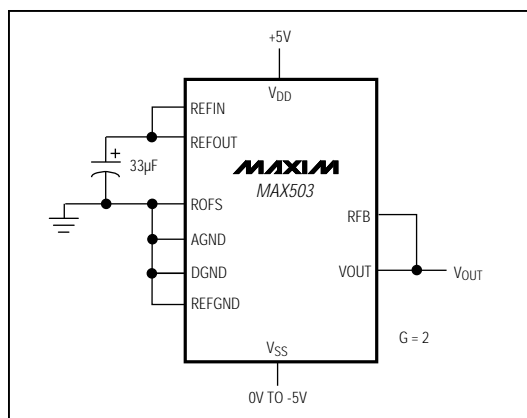


Figure 10. Unipolar Configuration (0V to +4.096V Output)

Figure 5 shows the circuit configuration for a 4-bit μP application. Figure 6 shows the corresponding timing sequence. The 4 low bits (S0, S1, D0, D1) are connected in parallel to the other 4 bits (D2–D5) and then to the μP bus. Address lines A0 and A1 enable the input data latches for the high, middle, or low data nibbles. The μP sends chip select (\overline{CS}) and write (\overline{WR}) signals to latch in each of three nibbles in three cycles when the data is valid.

Figure 7 shows a typical interface to an 8-bit or a 16-bit μP . Connect 8 data bits from the data bus to pins S0, S1, and D0–D5 on the MAX503. With \overline{LDAC} held high, the user can load NBH or NBL + NBM in any order. Figure 8a shows the corresponding timing sequence. For fastest throughput, use Figure 8b's sequence. Address lines A0 and A1 are tied together and the DAC is loaded in 2 cycles as 8 + 4. In this scheme, with \overline{LDAC} held low, the DAC latch is transparent. Always load NBL and NBM first, followed by NBH.

\overline{LDAC} is asynchronous with respect to \overline{WR} . If \overline{LDAC} is brought low before or at the same time \overline{WR} goes high, \overline{LDAC} must remain low for at least 50ns to ensure the correct data is latched. Data is latched into DAC registers on \overline{LDAC} 's rising edge.

Unipolar Configuration

The MAX503 is configured for a 0V to V_{REFIN} unipolar output range by connecting ROFS and RFB to VOUT (Figure 9). The converter operates from either single or dual supplies in this configuration. See Table 3 for the DAC-latch contents (input) vs. the analog VOUT (output). In this range, $1LSB = V_{REFIN}(2^{-10})$.

A 0V to $2V_{REFIN}$ unipolar output range is set up by connecting ROFS to AGND and RFB to VOUT (Figure 10). Table 4 shows the DAC-latch contents vs. VOUT. The MAX503 operates from either single or dual supplies in this mode. In this range, $1LSB = (2)(V_{REFIN})(2^{-10}) = (V_{REFIN})(2^{-9})$.

5V, Low-Power, Parallel-Input, Voltage-Output, 10-Bit DAC

Table 3. Unipolar Binary Code Table (0V to VREFIN Output), Gain = 1

INPUT*	OUTPUT
1111 1111 11(00)	$(V_{REFIN}) \frac{1023}{1024}$
1000 0000 01(00)	$(V_{REFIN}) \frac{513}{1024}$
1000 0000 00(00)	$(V_{REFIN}) \frac{512}{1024} = +V_{REFIN}/2$
0111 1111 11(00)	$(V_{REFIN}) \frac{511}{1024}$
0000 0000 01(00)	$(V_{REFIN}) \frac{1}{1024}$
0000 0000 00(00)	0V

* Write 10-bit data words with two sub-LSB 0s because the DAC input latch is 12 bits wide.

Table 4. Unipolar Binary Code Table (0V to 2VREFIN Output), Gain = 2

INPUT*	OUTPUT
1111 1111 11(00)	$+2 (V_{REFIN}) \frac{1023}{1024}$
1000 0000 01(00)	$+2 (V_{REFIN}) \frac{513}{1024}$
1000 0000 00(00)	$+2 (V_{REFIN}) \frac{512}{1024} = +V_{REFIN}$
0111 1111 11(00)	$+2 (V_{REFIN}) \frac{511}{1024}$
0000 0000 01(00)	$+2 (V_{REFIN}) \frac{1}{1024}$
0000 0000 00(00)	0V

* Write 10-bit data words with two sub-LSB 0s because the DAC input latch is 12 bits wide.

Bipolar Configuration

A $-V_{REFIN}$ to $+V_{REFIN}$ bipolar range is set up by connecting ROFS to REFIN and RFB to VOUT, and operating from dual ($\pm 5V$) supplies (Figure 11). Table 5 shows the DAC-latch contents (input) vs. VOUT (output). In this range, $1LSB = V_{REFIN} (2^{-9})$.

Four-Quadrant Multiplication

The MAX503 can be used as a four-quadrant multiplier by connecting ROFS to REFIN and RFB to VOUT, and using (1) an offset binary digital code, (2) bipolar power supplies, and (3) a bipolar analog input at REFIN within the range $V_{SS} + 2V$ to $V_{DD} - 2V$, as shown in Figure 12.

In general, a 10-bit DAC's output is $D(V_{REFIN})(G)$, where "G" is the gain (1 or 2) and "D" is the binary representation of the digital input divided by 2^{10} or 1,024. This formula is precise for unipolar operation. However, for bipolar, offset binary operation, the MSB is really a polarity bit. No resolution is lost because the number of steps is the same. The output voltage, however, has been shifted from a range of, for example, 0V to 4.096V ($G = 2$) to a range of -2.048V to +2.048V.

Keep in mind that when using the DAC as a four-quadrant multiplier, the scale is skewed. The negative full scale is $-V_{REFIN}$, while the positive full scale is $+V_{REFIN} - 1LSB$.

Table 5. Bipolar (Offset Binary) Code Table ($-V_{REFIN}$ to $+V_{REFIN}$ Output)

INPUT*	OUTPUT
1111 1111 11(00)	$(+V_{REFIN}) \frac{511}{512}$
1000 0000 01(00)	$(+V_{REFIN}) \frac{1}{512}$
1000 0000 00(00)	0V
0111 1111 11(00)	$(-V_{REFIN}) \frac{1}{512}$
0000 0000 01(00)	$(-V_{REFIN}) \frac{511}{512}$
0000 0000 00(00)	$(-V_{REFIN}) \frac{512}{512} = -V_{REFIN}$

* Write 10-bit data words with two sub-LSB 0s because the DAC input latch is 12 bits wide.

5V, Low-Power, Parallel-Input, Voltage-Output, 10-Bit DAC

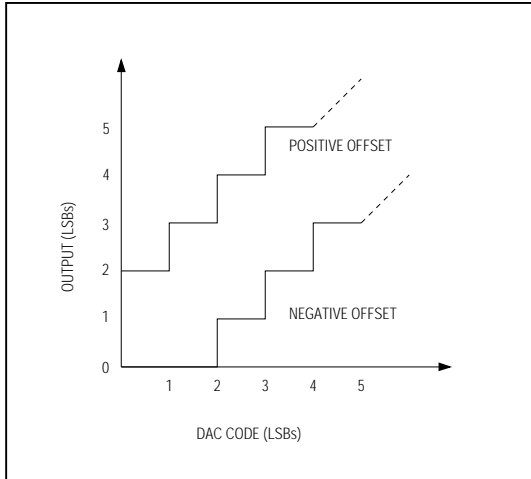


Figure 13. Single-Supply DAC Transfer Function

Maxim cannot assume responsibility for use of any circuitry other than circuitry entirely embodied in a Maxim product. No circuit patent licenses are implied. Maxim reserves the right to change the circuitry and specifications without notice at any time.

16 _____ Maxim Integrated Products, 120 San Gabriel Drive, Sunnyvale, CA 94086 (408) 737-7600

© 1994 Maxim Integrated Products

Printed USA

MAXIM is a registered trademark of Maxim Integrated Products.

Mouser Electronics

Authorized Distributor

Click to View Pricing, Inventory, Delivery & Lifecycle Information:

Maxim Integrated:

[MAX503CNG+](#) [MAX503CWG+](#) [MAX503CAG+](#) [MAX503CAG+T](#) [MAX503CWG+T](#) [MAX503EAG+](#) [MAX503EAG+T](#)
[MAX503ENG+](#) [MAX503EWG+](#) [MAX503EWG+T](#)