

Table 3. Electrical Characteristics ($T_C = 25^\circ\text{C}$ unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
Off Characteristics					
Drain-Source Breakdown Voltage ($V_{GS} = 0\text{ Vdc}$, $I_D = 20\ \mu\text{Adc}$)	$V_{(BR)DSS}$	65	—	—	Vdc
Zero Gate Voltage Drain Current ($V_{DS} = 28\text{ Vdc}$, $V_{GS} = 0\text{ Vdc}$)	I_{DSS}	—	—	10	μAdc
Gate-Source Leakage Current ($V_{GS} = 20\text{ Vdc}$, $V_{DS} = 0\text{ Vdc}$)	I_{GSS}	—	—	1	μAdc
On Characteristics					
Gate Threshold Voltage ($V_{DS} = 10\text{ Vdc}$, $I_D = 300\ \mu\text{Adc}$)	$V_{GS(th)}$	2	3	4	Vdc
Gate Quiescent Voltage ($V_{DS} = 26\text{ Vdc}$, $I_D = 400\ \text{mAdc}$)	$V_{GS(Q)}$	3	4	5	Vdc
Drain-Source On-Voltage ($V_{GS} = 10\text{ Vdc}$, $I_D = 1\text{ Adc}$)	$V_{DS(on)}$	—	0.15	0.6	Vdc
Forward Transconductance ($V_{DS} = 10\text{ Vdc}$, $I_D = 2\text{ Adc}$)	g_{fs}	2	3	—	S
Dynamic Characteristics					
Input Capacitance (1) ($V_{DS} = 26\text{ Vdc}$, $V_{GS} = 0$, $f = 1\text{ MHz}$)	C_{iss}	—	130	—	pF
Output Capacitance ($V_{DS} = 26\text{ Vdc}$, $V_{GS} = 0$, $f = 1\text{ MHz}$)	C_{oss}	41	47	52	pF
Reverse Transfer Capacitance ($V_{DS} = 26\text{ Vdc}$, $V_{GS} = 0$, $f = 1\text{ MHz}$)	C_{rss}	2.4	3	3.4	pF
Functional Tests (In Freescale Test Fixture)					
Output Power ($V_{DD} = 26\text{ Vdc}$, $I_{DQ} = 400\text{ mA}$, $f = 940\text{ MHz}$)	P1dB	73	80	—	W
Common-Source Amplifier Power Gain @ P1dB (Min) ($V_{DD} = 26\text{ Vdc}$, $I_{DQ} = 400\text{ mA}$, $f = 940\text{ MHz}$)	G_{ps}	14	16	18	dB
Drain Efficiency @ $P_{out} = 50\text{ W}$ ($V_{DD} = 26\text{ Vdc}$, $I_{DQ} = 400\text{ mA}$, $f = 940\text{ MHz}$)	η_1	47	51	—	%
Drain Efficiency @ P1dB ($V_{DD} = 26\text{ Vdc}$, $I_{DQ} = 400\text{ mA}$, $f = 940\text{ MHz}$)	η_2	—	58	—	%
Input Return Loss @ $P_{out} = 50\text{ W}$ ($V_{DD} = 26\text{ Vdc}$, $I_{DQ} = 400\text{ mA}$, $f = 940\text{ MHz}$)	IRL	—	—	-15	dB

1. Value excludes the input matching.

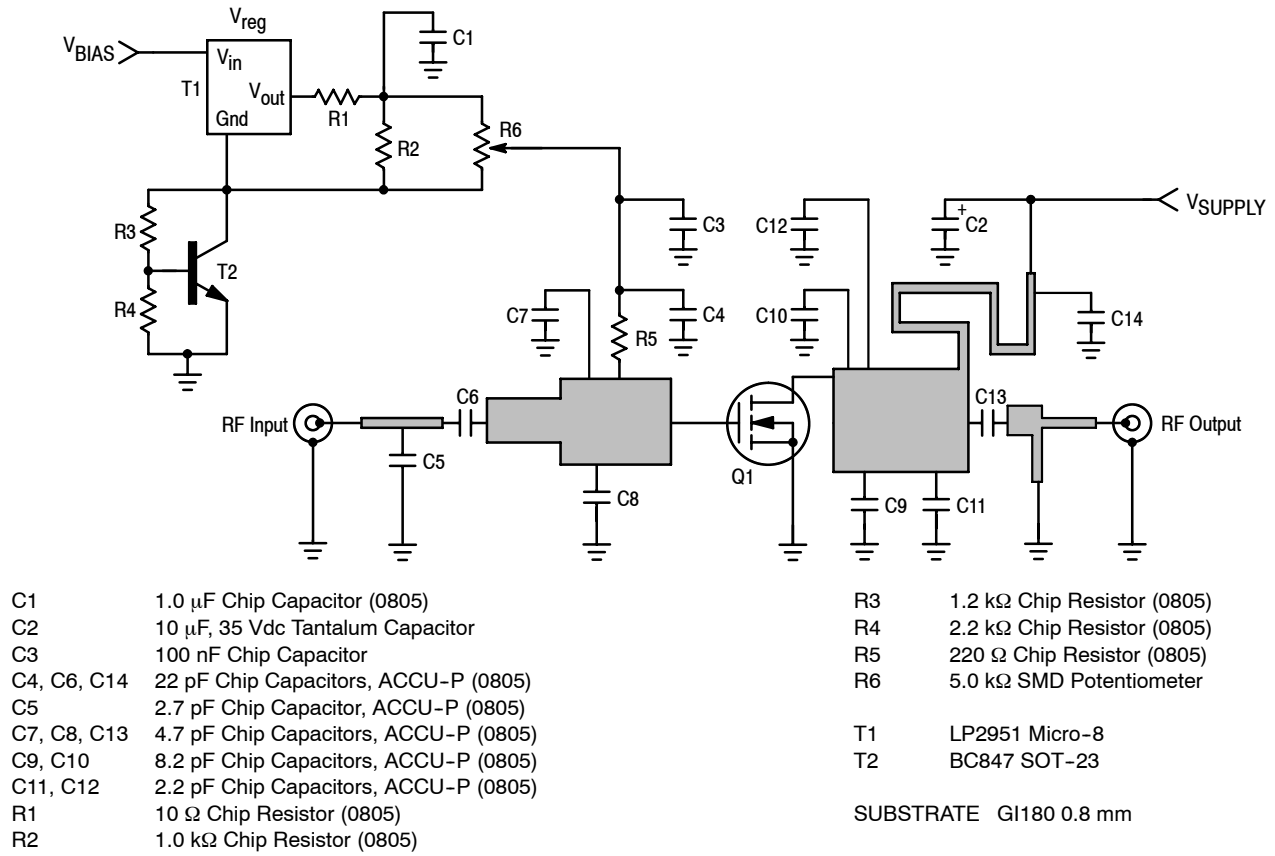
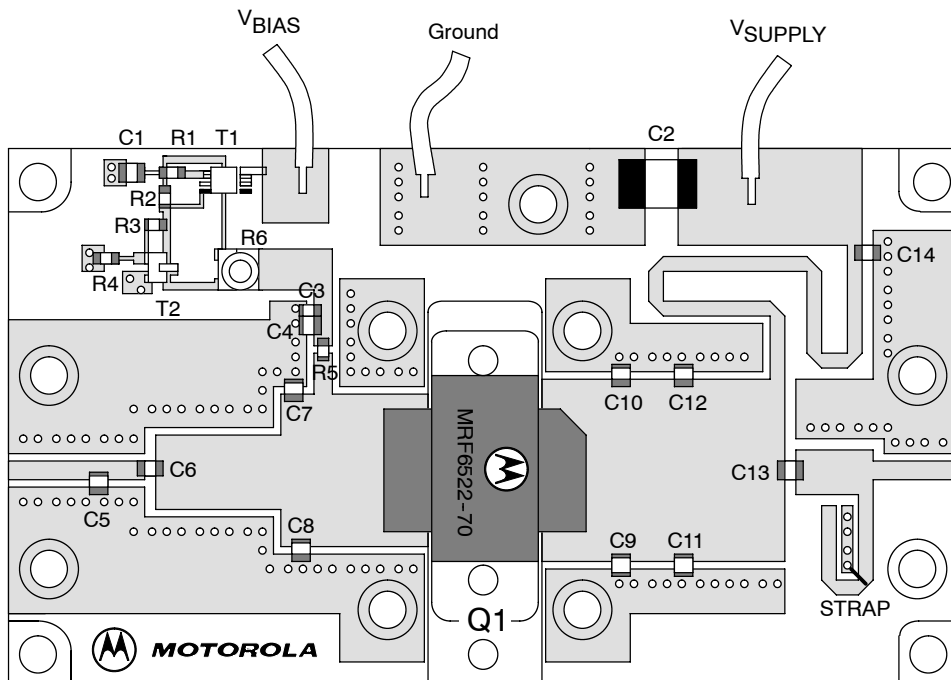


Figure 1. MRF6522-70 Test Circuit Schematic



Freescale has begun the transition of marking Printed Circuit Boards (PCBs) with the Freescale Semiconductor signature/logo. PCBs may have either Motorola or Freescale markings during the transition period. These changes will have no impact on form, fit or function of the current product.

Figure 2. MRF6522-70 Test Circuit Component Layout

TYPICAL CHARACTERISTICS

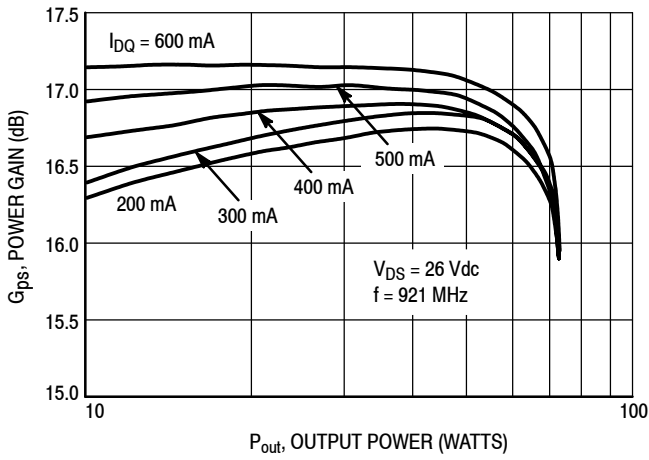


Figure 3. Power Gain versus Output Power

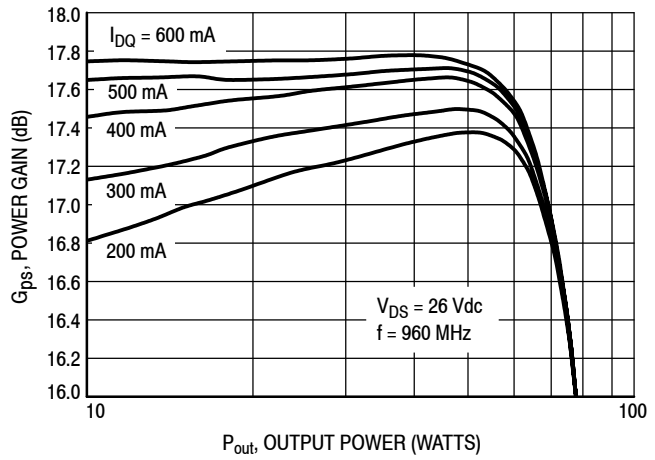


Figure 4. Power Gain versus Output Power

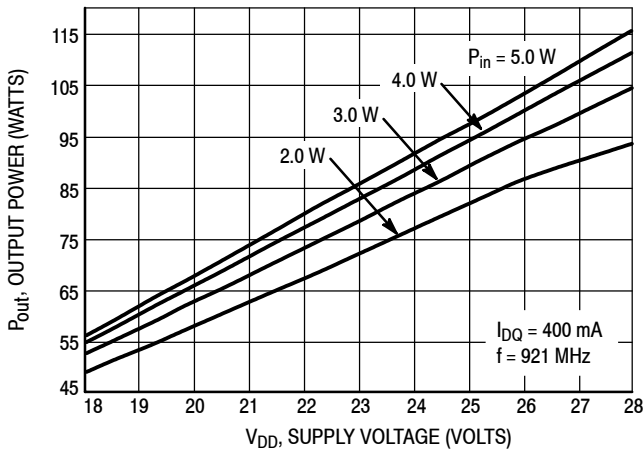


Figure 5. Output Power versus Supply Voltage

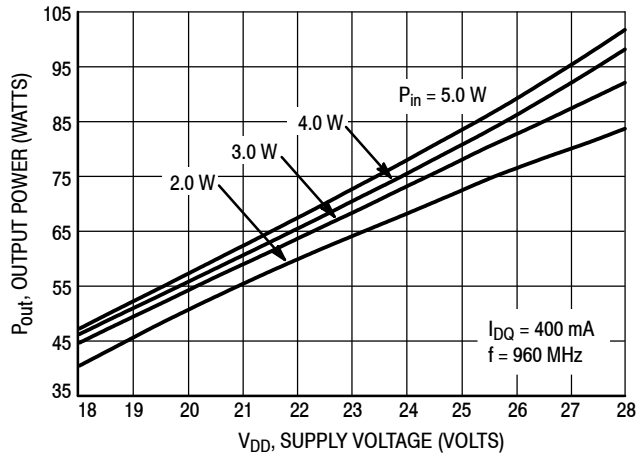


Figure 6. Output Power versus Supply Voltage

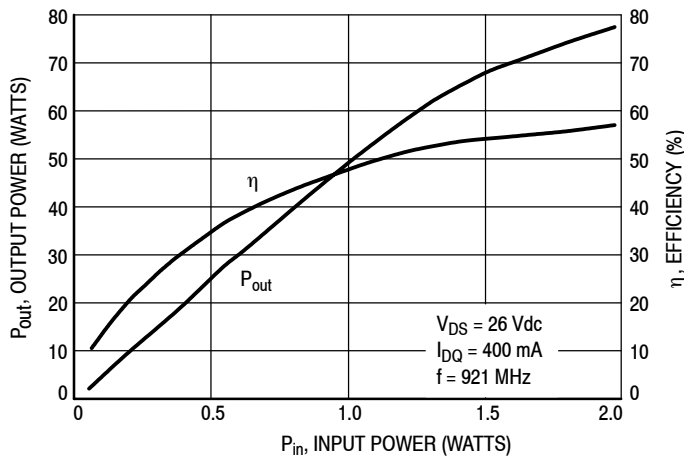


Figure 7. Efficiency and Output Power versus Input Power

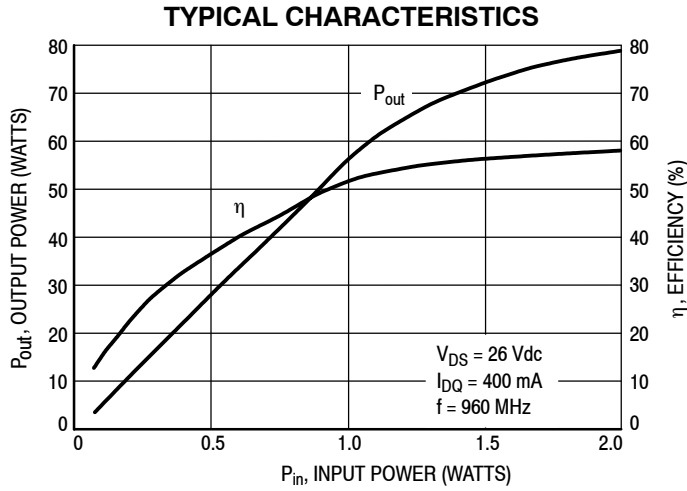


Figure 8. Efficiency and Output Power versus Input Power

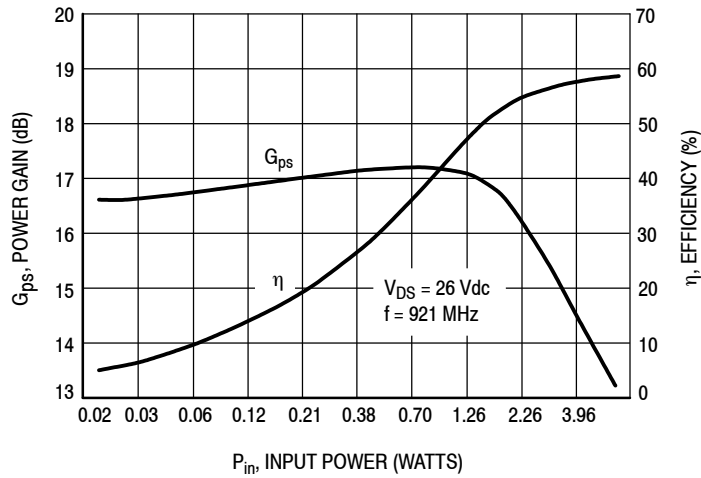


Figure 9. Power Gain and Efficiency versus Input Power

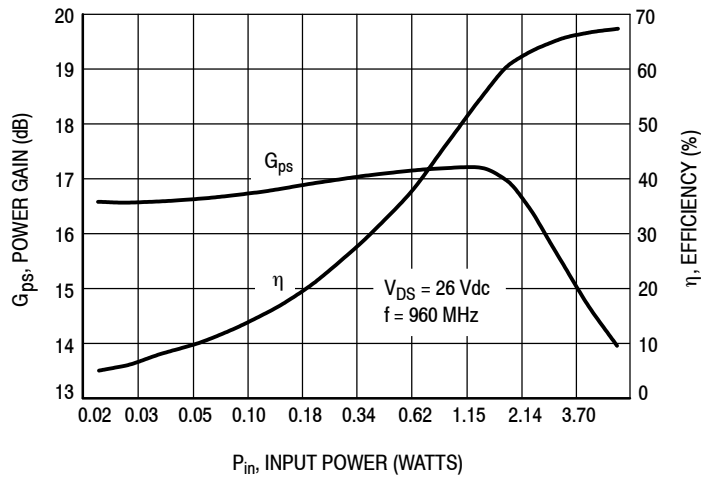


Figure 10. Power Gain and Efficiency versus Input Power

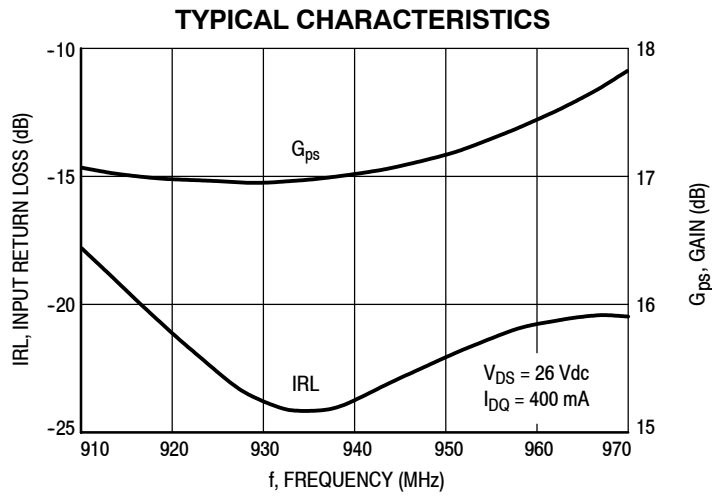
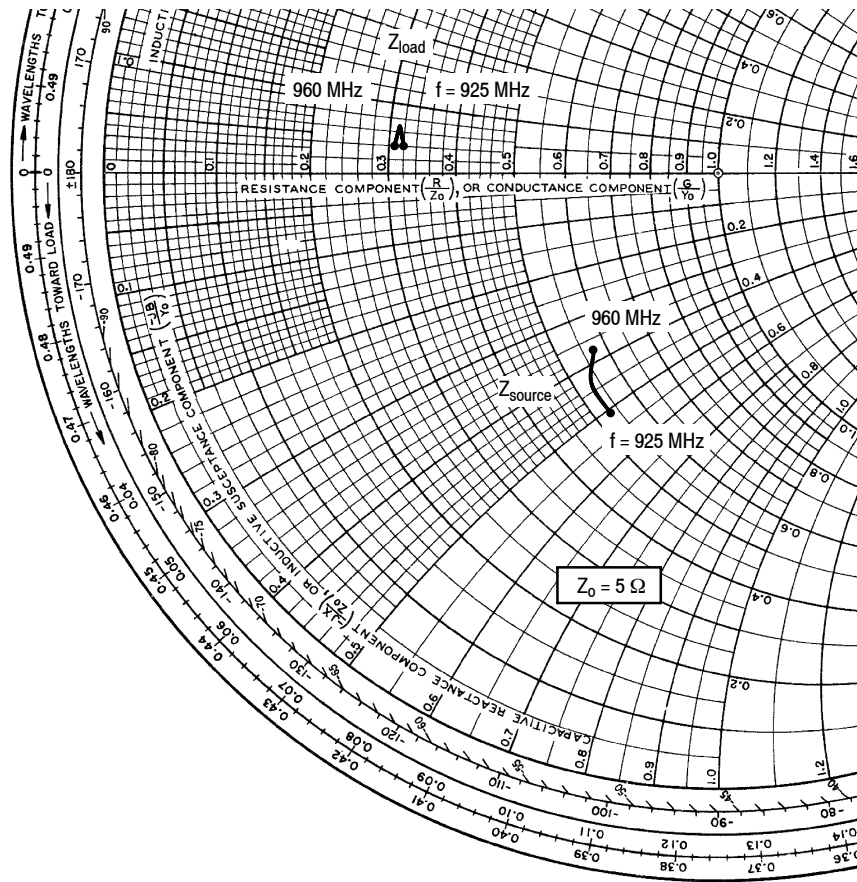


Figure 11. Performance in Broadband Circuit (at Small Signal)



$V_{SUPPLY} = 26 \text{ Vdc}$, $I_{BIAS} = 400 \text{ mA}$, $CW = \text{Room Temperature}$

f MHz	Z_{source} Ω	Z_{load} Ω
925	$2.65 - j2.53$	$1.62 + j0.2$
940	$2.67 - j2.14$	$1.56 + j0.34$
960	$2.85 - j1.87$	$1.55 + j0.2$

Z_{source} = Test circuit impedance as measured from gate to ground.

Z_{load} = Test circuit impedance as measured from drain to ground.

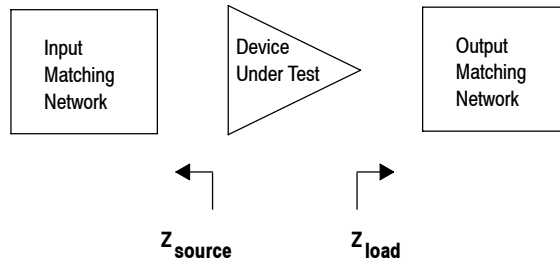
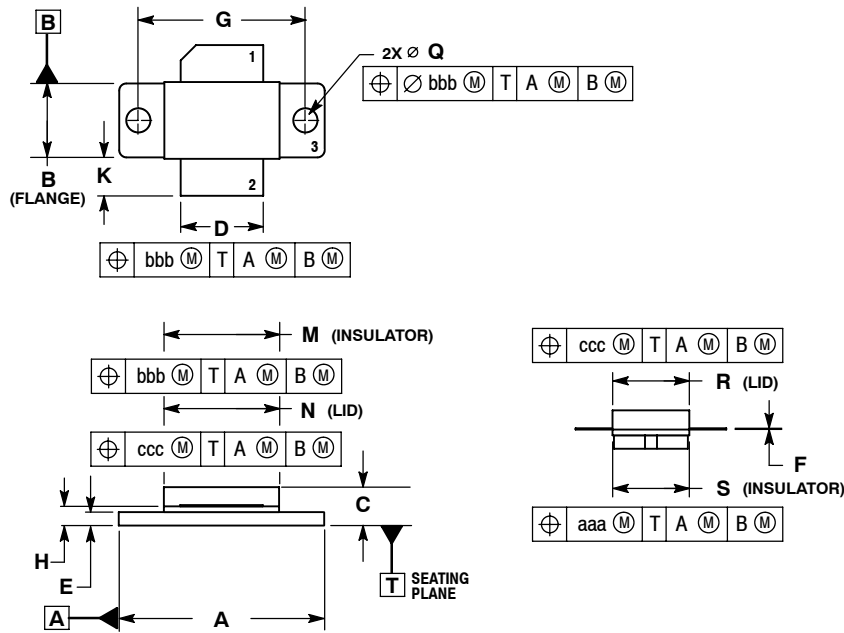


Figure 12. Series Equivalent Source and Load Impedance

PACKAGE DIMENSIONS



- NOTES:
1. INTERPRET DIMENSIONS AND TOLERANCES PER ANSI Y14.5M-1994.
 2. CONTROLLING DIMENSION: INCH.
 3. DIMENSION H IS MEASURED 0.030 (0.762) AWAY FROM PACKAGE BODY.

DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	1.065	1.075	27.05	27.30
B	0.380	0.390	9.65	9.91
C	0.160	0.205	4.06	5.21
D	0.425	0.435	10.80	11.05
E	0.060	0.070	1.52	1.78
F	0.004	0.006	0.10	0.15
G	0.870 BSC		22.10 BSC	
H	0.096	0.106	2.44	2.69
K	0.190	0.223	4.83	5.66
M	0.594	0.606	15.09	15.39
N	0.591	0.601	15.01	15.27
Q	0.124	0.130	3.15	3.30
R	0.394	0.404	10.01	10.26
S	0.395	0.405	10.03	10.29
aaa	0.005 REF		0.13 REF	
bbb	0.010 REF		0.25 REF	
ccc	0.015 REF		0.38 REF	

- STYLE 1:
 PIN 1. DRAIN
 2. GATE
 3. SOURCE

**CASE 465D-05
 ISSUE D
 NI-600**

PRODUCT DOCUMENTATION

Refer to the following documents to aid your design process.

Engineering Bulletins

- EB212: Using Data Sheet Impedances for RF LDMOS Devices

REVISION HISTORY

The following table summarizes revisions to this document.

Revision	Date	Description
9	Oct. 2008	<ul style="list-style-type: none">• Modified data sheet to reflect RF Test Reduction described in Product and Process Change Notification number, PCN12779, p. 1, 2• Added Product Documentation and Revision History, p. 9
	Dec. 2010	<ul style="list-style-type: none">• Data sheet archived. Part no longer manufactured.

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