ABSOLUTE MAXIMUM RATINGS

Voltage Range on Any Pin Relative to Ground	-0.3V to +6V
Operating Temperature Range	-40°C to +85°C
Storage Temperature Range	-55°C to +125°C
Soldering Temperature	See IPC/JEDECJ-STD-020A

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to the absolute maximum rating conditions for extended periods may affect device reliability.

RECOMMENDED DC OPERATING CONDITIONS

(V_{DD} = 2.5V to 4.5V, T_A = -20°C to +70°C.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Supply Voltage	V_{DD}	(Note 1)	+2.5		+4.5	V
Data I/O Pins	SCL, SDA	(Note 1)	-0.3		+5.5	V
Programmable I/O Pin	PIO	(Note 1)	-0.3		+5.5	V
V_{IN}, AIN0, AIN1 Pin	V_{IN}, AIN0, AIN1	(Note 1)	-0.3		V_{DD} + 0.3	V

DC ELECTRICAL CHARACTERISTICS

(V_{DD} = 2.5V to 4.5V, T_A = -20°C to +70°C.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Active Current	I_{ACTIVE}			70	100	µA
		V_{DD} = 4.5V			105	
Sleep-Mode Current	I_{SLEEP}	V_{DD} = 2.0V, SCL, SDA = Vss		0.5	1.0	µA
		SCL, SDA = Vss		1	3	
Current Resolution	I_{LSB}			6.25		µV
Current Full-Scale Magnitude	I_{FS}	(Note 1)		±51.2		mV
Current Offset	I_{OERR}	(Note 2)	-12.5		+12.5	µV
Current Gain Error	I_{GERR}	(Note 11)	-1.5		+1.5	% of reading
Timebase Accuracy	t_{ERR}	V_{DD} = 3.6V at +25°C	-1		+1	%
		T_A = 0°C to +70°C	-2		+2	
		T_A = -20°C to +70°C	-3		+3	
Voltage Error	V_{GERR}	V_{DD} = V_{IN} = 3.6V	-10		+10	mV
			-20		+20	
Input Resistance V_{IN}, AIN0, AIN1	R_{IN}		15			MΩ
AIN0, AIN1 Error	AIN_{GERR}	(Note 10)	-8		+8	LSB
V_{OUT} Output Drive		I_O = 1mA	V_{DD} -0.1			V
V_{OUT} Precharge Time	t_{PRE}	V_{ODIS} bit = 0	13.3		14.2	ms
Input Logic High: SCL, SDA	V_{IH}	(Note 1)	1.5			V
Input Logic Low: SCL, SDA	V_{IL}	(Note 1)			0.6	V
Output Logic Low: SDA	V_{OL}	I_{OL} = 4mA, (Note 1)			0.4	V
Pulldown Current:	I_{PD}	V_{DD} = 4.2V,		0.2		µA

SCL, SDA		V_{PIN} = 0.4V			
Input Capacitance: SCL, SDA	C_{BUS}			50	pF
Bus Low Timeout	t_{SLEEP}	(Note 3)	1.5	2.2	S

DC ELECTRICAL CHARACTERISTICS: 2-WIRE INTERFACE

(V_{DD} = 2.5V to 4.5V, T_A = -20°C to +70°C.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
SCL Clock Frequency	f_{SCL}	(Note 4)	0		400	KHz
Bus Free Time Between a STOP and START Condition	t_{BUF}		1.3			µs
Hold Time (Repeated) START Condition	$t_{HD:STA}$	(Note 5)	0.6			µs
Low Period of SCL Clock	t_{LOW}		1.3			µs
High Period of SCL Clock	t_{HIGH}		0.6			µs
Setup Time for a Repeated START Condition	$t_{SU:STA}$		0.6			µs
Data Hold Time	$t_{HD:DAT}$	(Note 6, 7)	0		0.9	µs
Data Setup Time	$t_{SU:DAT}$	(Note 6)	100			ns
Rise Time of Both SDA and SCL Signals	t_R		20 + 0.1C_B		300	ns
Fall Time of Both SDA and SCL Signals	t_F		20 + 0.1C_B		300	ns
Setup Time for STOP Condition	$t_{SU:STO}$		0.6			µs
Spike Pulse Widths Suppressed by Input Filter	t_{SP}	(Note 8)	0		50	ns
Capacitive Load for Each Bus Line	C_B	(Note 9)			400	pF
SCL, SDA Input Capacitance	C_{BIN}				60	pF

Note 1: All voltages are referenced to V_{SS}.
Note 2: Offset specified after auto-calibration cycle and Current Offset Bias register = 0x00.
Note 3: The DS2746 enters the sleep mode 1.5s to 2.2s after (SCL < V_{il}.) AND (SDA < V_{il}).
Note 4: Timing must be fast enough to prevent the DS2746 from entering sleep mode due to bus low for period > t_{SLEEP}.
Note 5: f_{SCL} must meet the minimum clock low time plus the rise/fall times.
Note 6: The maximum $t_{HD:DAT}$ has only to be met if the device does not stretch the LOW period (t_{LOW}) of the SCL signal.
Note 7: This device internally provides a hold time of at least 100ns for the SDA signal (referred to the VIHmin of the SCL signal) to bridge the undefined region of the falling edge of SCL.
Note 8: Filters on SDA and SCL suppress noise spikes at the input buffers and delay the sampling instant.
Note 9: C_b – total capacitance of one bus line in pF.
Note 10: The AIN_{GERR} spec is only valid when this equation is satisfied: (V_{AINx} + 2V_{OUT}) ≤ (11.6V - (T_A - 25°C)10mV/°C). See Figure 1.
Note 11: Accuracy specification valid for V_{SS} - SNS ≥ ±2.5mV, below which offset error is dominant.

Figure 1. Valid Range for AIN_{GERR} Accuracy Specification

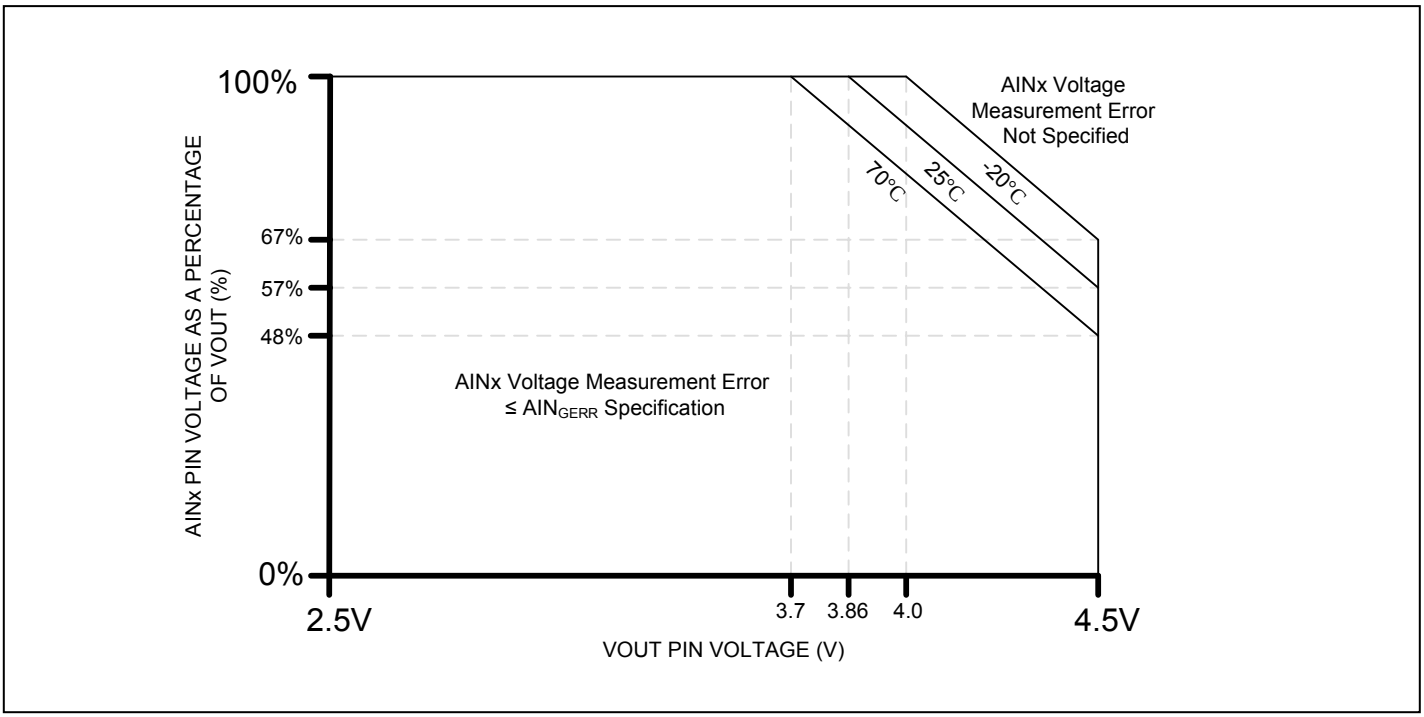
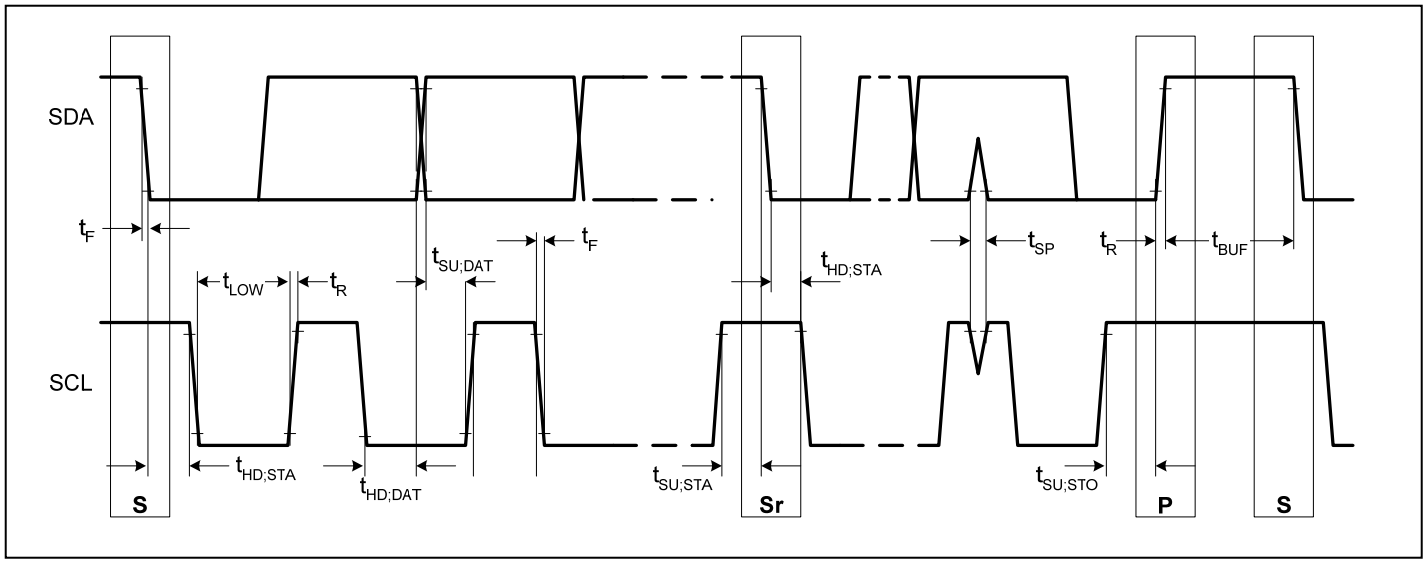


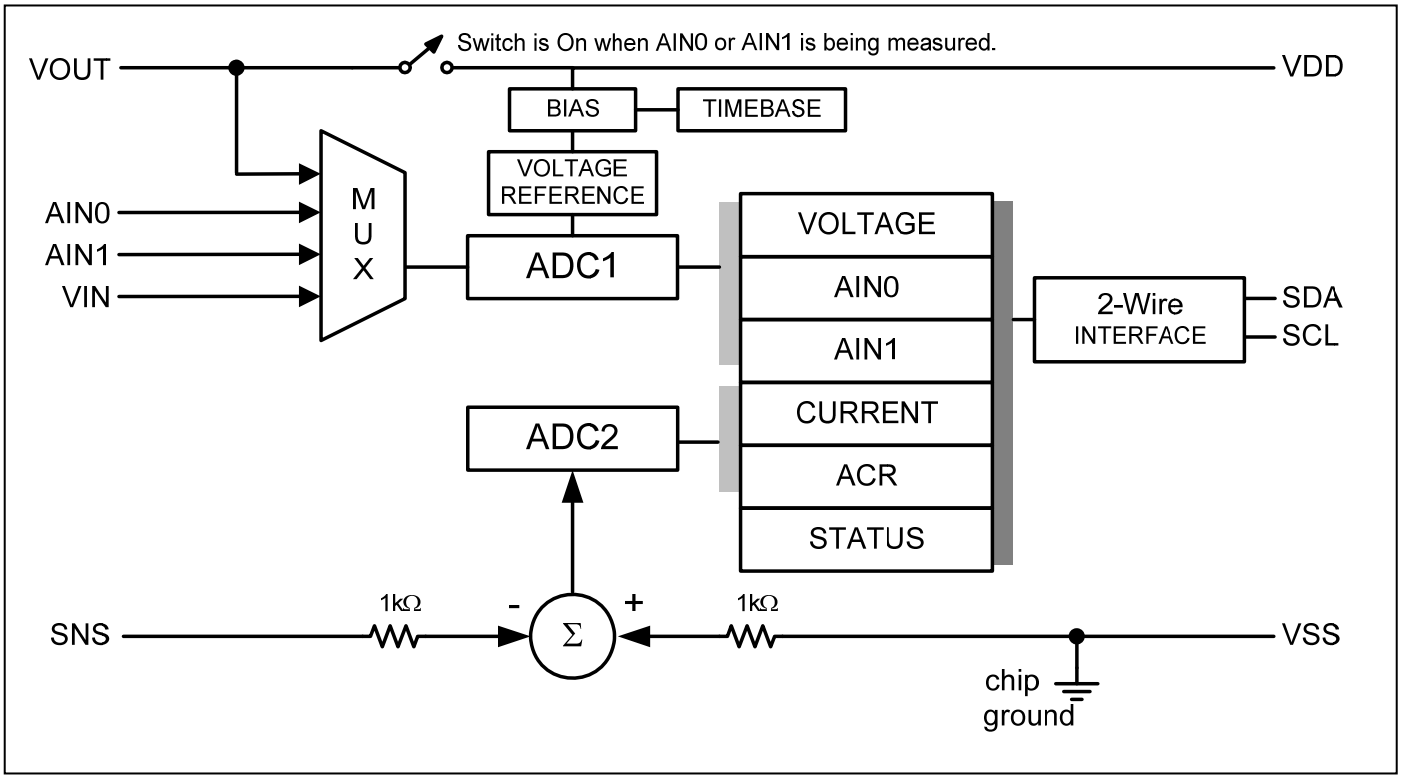
Figure 2. 2-Wire Bus Timing Diagram



PIN DESCRIPTION

PIN	NAME	FUNCTION
1	AIN1	**Aux Voltage Input Number 1.**
2	AIN0	**Aux Voltage Input Number 0.**
3	SCL	**Serial Clock Input.** Input only 2-wire clock line. Connect this pin to the CLOCK signal of the 2-wire interface. This pin has a 0.2µA typical pulldown to sense disconnection.
4	SDA	**Serial Data Input / Output.** Open drain 2-wire data line. Connect this pin to the DATA signal of the 2-wire interface. This pin has a 0.2µA typical pulldown to sense disconnection.
5	SNS	**Current-Sense Input.** Connect to the handset side of the sense resistor.
6	V_{SS}	**Device Ground.** Connect to the battery side of the sense resistor.
7	CTG	**Connect to Ground.** Connect to the battery side of the sense resistor.
8	V_{OUT}	**Voltage Out.** Supply for Aux input voltage Measurement dividers. Connect to high side of resistor divider circuits.
9	V_{IN}	**Battery Voltage Input.** The voltage of the cell pack is measured through this pin.
10	V_{DD}	**Power-Supply Input.** 2.5V to 4.5V input range. Connect to system power through a decoupling network.
PAD	PAD	**Exposed Pad.** Connect to V_{SS}.

Figure 3. Block Diagram



DETAILED DESCRIPTION

The DS2746 operates either in active mode where cell voltage, system current, and auxiliary inputs are monitored, or in a low power sleep mode to conserve energy when the system is idle. While in active mode, the DS2746 contantly measures current flow through an external sense resistor. Each current measurement is reported with sign and magnitude in a two-byte Current register. Offset bias and offset blanking features remove offset error from the current A/D to improve measurement accuracy. Each current measurement is integrated into the Accumulated Current register (ACR) to maintain a sum of all charge entering and exiting the cell.

The DS2746 has two auxiliary inputs to allow voltage sampling of resistor divider circuits. These can be used to measure a thermistor or an ID resistor located inside the battery pack. The V_{OUT} output provides the pullup voltage for the resistor divider networks. The DS2746 disables V_{OUT} after measuring the auxiliary inputs to reduce power use by the measurement system. V_{OUT} operation can be disabled through software to further reduce power consumption when the auxiliary inputs are not in use.

A dedicated voltage A/D measures voltage of the cell and the auxiliary inputs. A mux on the input to the A/D cycles through the V_{IN}, AIN0, and AIN1 pins repeatedly in that order. An internal reference is used to measure V_{IN} voltage. AIN0 and AIN1 are measured as a percentage of V_{OUT}. This ratiometric measurement of the Auxiliary inputs prevents noise in the supply from affecting accuracy of the readings

The DS2746 measurements can be used directly to provide accurate fuel gauging in typical use conditions, or along with FuelPack™ algorithms to form a complete and accurate solution for estimating remaining capacity over wide temperature and operating conditions.

Through its 2-Wire interface, the DS2746 allows a host system read/write access to the Status/Configuration register and Measurement registers. If sleep mode operation is enabled, holding both interface lines low forces the DS2746 into a low power sleep mode where A/D measurements are paused and the ACR register is maintained.

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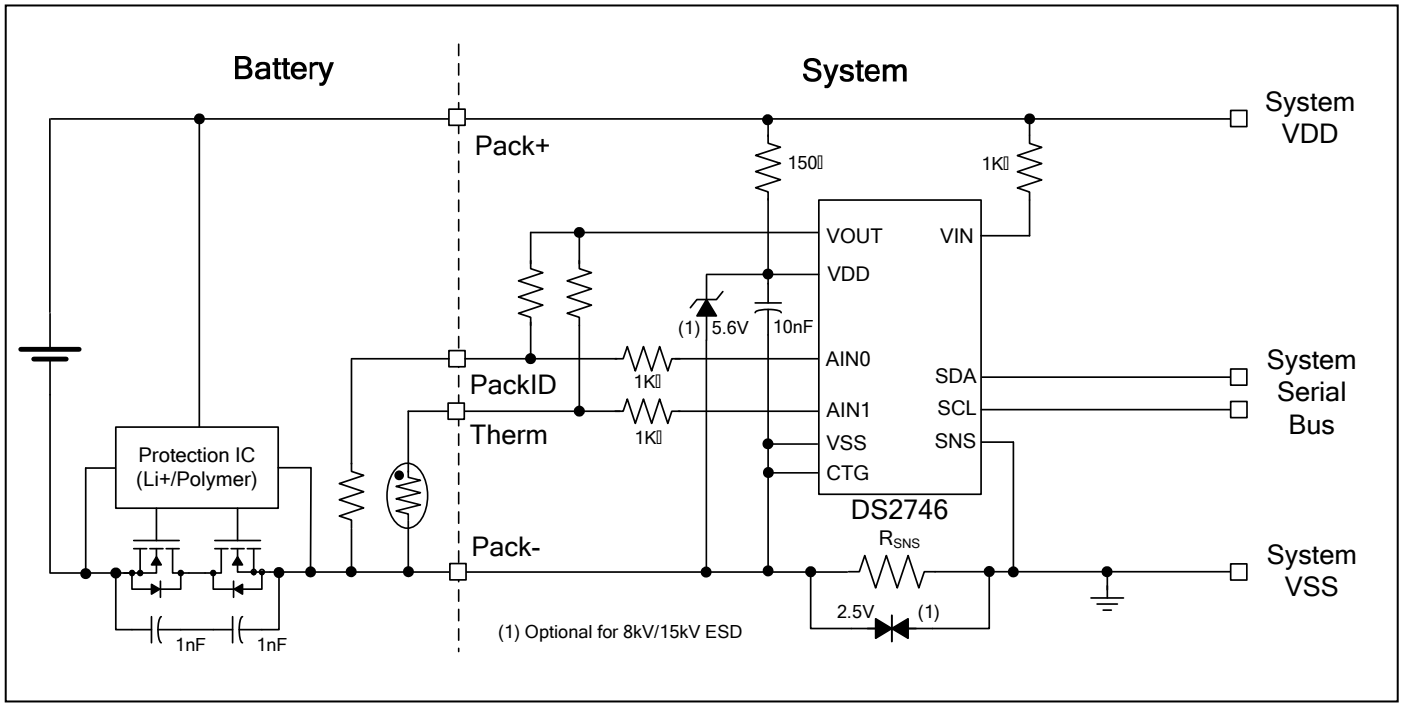
Figure 4. APPLICATION EXAMPLE



POWER MODES

The DS2746 operates in one of two power modes: active and sleep. While in active mode, the DS2746 operates as a high-precision battery monitor with voltage, auxiliary inputs, current and accumulated current measurements acquired continuously and the resulting values updated in the measurement registers. Read and write access is allowed to all registers. In sleep mode, the DS2746 operates in a low-power mode with no measurement activity.

The DS2746 operating mode transitions from SLEEP to ACTIVE when:

$$(SCL > V_{IH}) OR (SDA > V_{IH})$$

The DS2746 operating mode transitions from ACTIVE to SLEEP when:

$$SMOD = 1 AND [(SCL < V_{IL}) AND (SDA < V_{IL})] for t_{SLEEP}$$

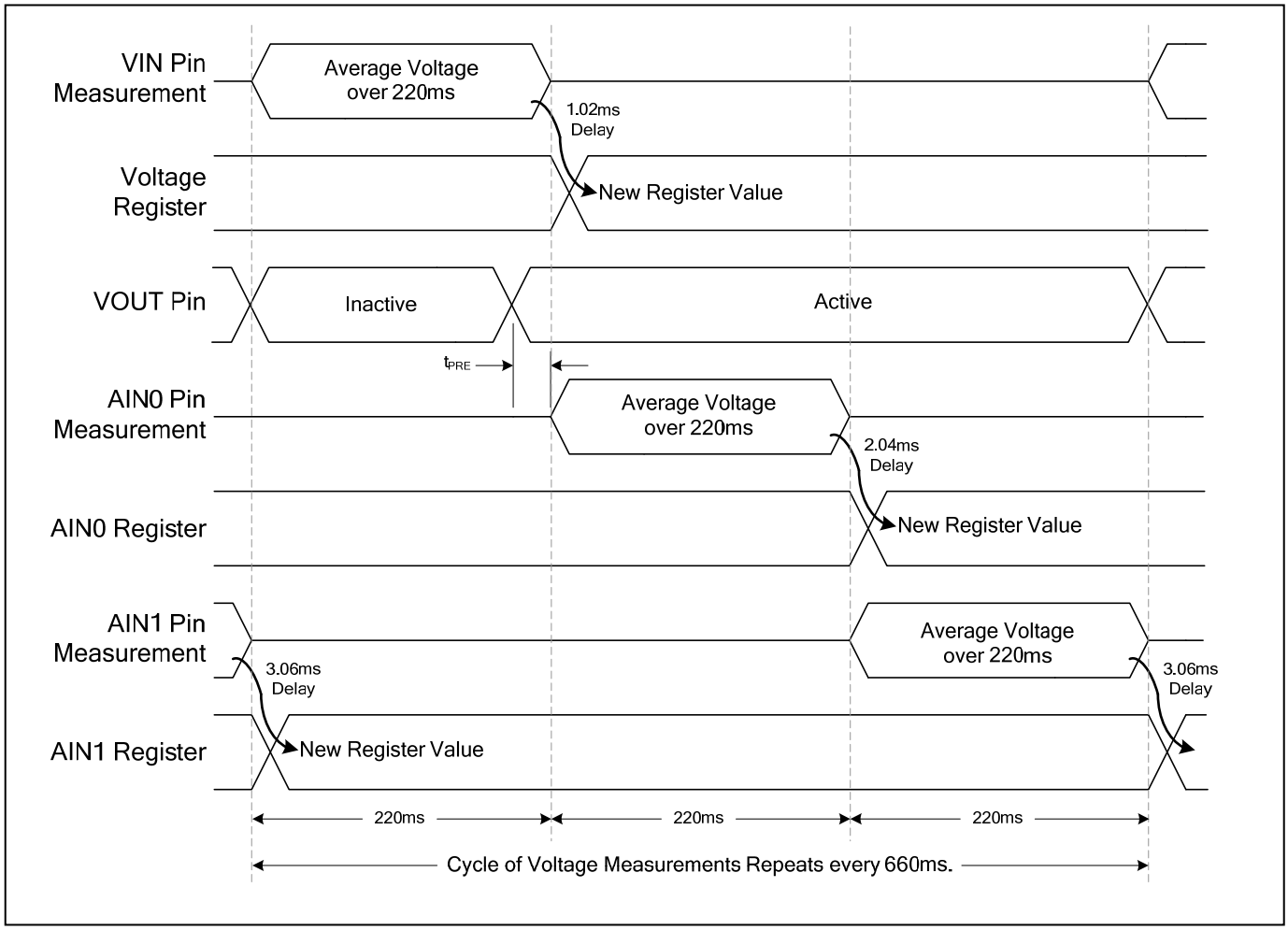
***CAUTION**: If SMOD = 1, a pull-up resistor is required on SCL and SDA in order to ensure that the DS2746 transitions from SLEEP to ACTIVE mode when the battery is charged. If the bus is not pulled up, the DS2746 remains in SLEEP and cannot accumulate the charge current.*

MEASUREMENT SEQUENCE

The DS2746 uses seperate A/D converters to make voltage and current measurements. Each A/D converter operates completely independent of the other, allowing measurements of voltage and current to be made in parallel. Current Measurements are made at a resolution of 13 bits plus sign bit. The current register is updated every 878ms with the average for that time period.

All Voltage Measurements are made at a resolution of 11 bits plus sign bit. The DS2746 continouly cycles through measuring V_{IN}, AIN0, and AIN1 in that order. Voltage measurement of each input requires 220ms to complete. A full sequence of voltage measurements requires 660ms to complete. V_{OUT} is active for a precharge time of t_{PRE} before the AIN0 measurement time occurs. The V_{OUT} pin is enabled during the entire AIN0 and AIN1 measurement sequence as long as the V_{ODIS} (V_{OUT} Disable) bit is cleared. See Figure 5.

Figure 5. Measurement Timing



VOLTAGE MEASUREMENT

Battery voltage is measured at the V_{IN} input with respect to V_{SS} over a range of 0V to 4.997V (limited by VDD pin voltage) and with a resolution of 2.44mV. The result is updated every 660ms with the average voltage over the last 220ms and placed in the VOLTAGE register in two's compliment form. Voltages above the maximum register value are reported as 7FFFh.

Figure 6. Voltage Register Format

MSB—Address 0Ch

S	2^{10}	2^9	2^8	2^7	2^6	2^5	2^4

MSb LSb

LSB—Address 0Dh

2^3	2^2	2^1	2^0	X	X	X	X

MSb LSb

"S": sign bit(s), "X": reserved

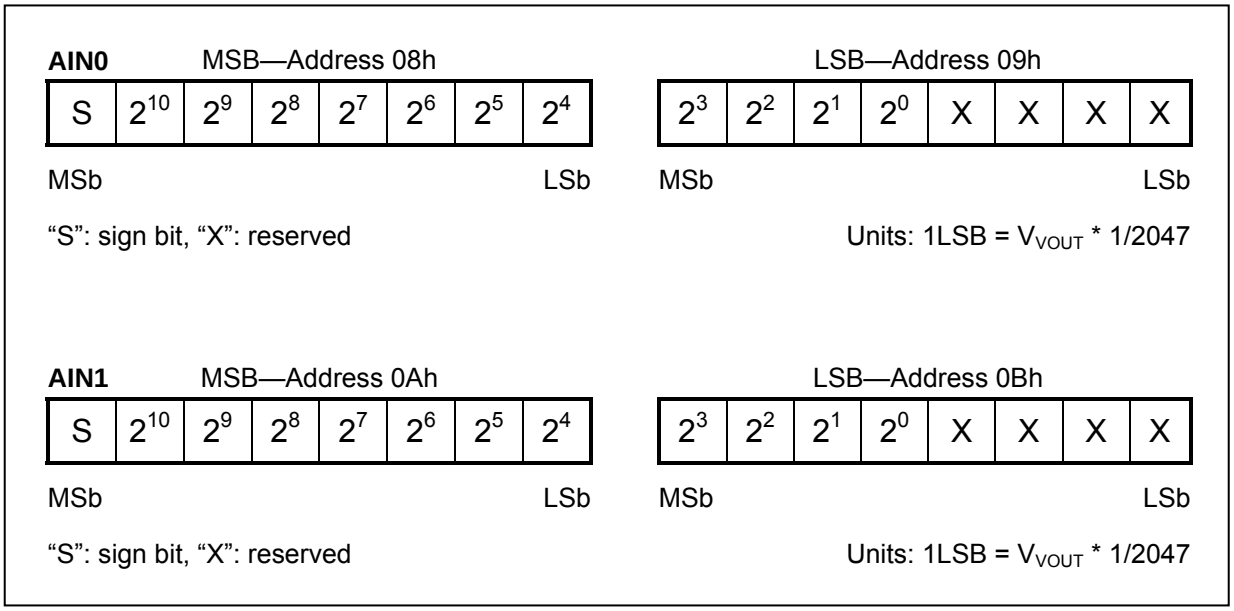
Units: 2.44mV

The input impedance of V_{IN} is sufficiently large (>15MΩ) to be connected to a high impedance voltage divider in order to support multiple cell applications. The pack voltage should be divided by the number of series cells to present a single cell average voltage to the V_{IN} input.

AUXILARY INPUT MEASUREMENTS

The DS2746 allows for measuring two auxiliary measurement inputs, AIN0 and AIN1, with respect to V_{SS}. These inputs are designed for measuring resistor ratios, particularly useful for measuring thermistor or pack identification resistors. At a time of t_{PRE} prior to the beginning of a measurement cycle on AIN0 or AIN1, the V_{OUT} pin puts out a reference voltage in order to drive a resistive divider formed by a known resistor value, and the unknown resistance to be measured. Making these measurements ratiometric with respect to V_{OUT} removes reference tolerance from the error calculations. Each auxiliary input measurement is updated every 660ms with the average voltage over the 220ms conversion period and placed in the AIN0 and AIN1 Registers in two's complement form. The input impedances of AIN0 and AIN1 are sufficiently large (>15MΩ) to be connected to a wide range of voltage divider resistances.

Figure 7. Auxiliary Input Registers Format



CURRENT MEASUREMENT

In the active mode of operation, the DS2746 continually measures the current flow into and out of the battery by measuring the voltage drop across a low-value current-sense resistor, R_{SNS}, connected between the SNS and V_{SS} pins. The voltage sense range between SNS and V_{SS} is ±51.2mV. Note that positive current values occur when V_{SNS} is less than V_{SS}, and negative current values occur when V_{SNS} is greater than V_{SS}. Peak signal amplitudes up to 102mV are allowed at the input as long as the continuous or average signal level does not exceed ±51.2mV over the conversion period. The ADC samples the input differentially and updates the current register at the completion of each conversion. The result is updated every 878ms with the average voltage and placed in the CURRENT register in two's compliment form. The current measurement register format is shown in Figure 8 and specifications for several different sense resistor options are shown in Tables 1 and 2. Charge currents above the maximum register value are reported at the maximum value (7FFFh = +51.2mV). Discharge currents below the minimum register value are reported at the minimum value (8000h = -51.2mV).

Figure 8. Current Register Formats

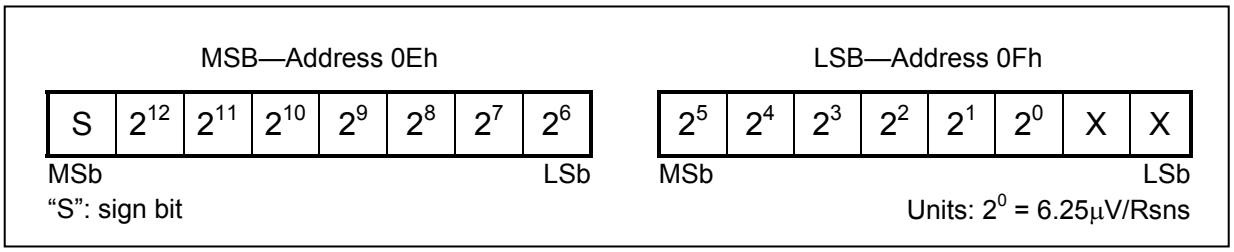


Table 1. Current Resolution for Various RSNS Values

CURRENT RESOLUTION (1 LSB)				
V_{SS} - V_{SNS}	R_{SNS}			
	20mΩ	15mΩ	10mΩ	5mΩ
6.25µV	312.5µA	416.7µA	625µA	1.25mA

Table 2. Current Range for Various RSNS Values

CURRENT INPUT RANGE				
V_{SS} - V_{SNS}	R_{SNS}			
	20mΩ	15mΩ	10mΩ	5mΩ
±51.2mV	±2.56A	±3.41A	±5.12A	±10.24A

Every 1024th conversion, the ADC measures its input offset to facilitate offset correction. Offset correction occurs approximately once per hour. The resulting correction factor is applied to the subsequent 1023 measurements. During the offset correction conversion, the ADC does not measure the SNS to V_{SS} signal. A maximum error of 1/1024 in the accumulated current register (ACR) is possible, however, to reduce the error, the current measurement just prior to the offset conversion is displayed in the current register and is substituted for the dropped current measurement in the current accumulation process. The error due to offset correction is typically much less than 1/1024 of the expected reading.

CURRENT ACCUMULATION

The Accumulated Current register (ACR) serves as an up/down counter holding a running count of charge stored in the battery. Current measurement results, plus a programmable bias value are internally summed, or accumulated, at the completion of each current measurement conversion period with the results displayed in the ACR. The ACR has a range of 0mVh to +409.6mVh with an LSb of 6.25µVh. Additional registers hold fractional results of each accumulation, however, these bits are not user accessible. The ACR count clamps at FFFFh when accumulating charge values and at 0000h when accumulating discharge values.

Read and write access is allowed to the ACR. Whenever the ACR is written, fractional accumulation results are cleared. A write to the ACR also forces the ADC to measure its offset and update the offset correction factor. Current measurement and accumulation resume (using the new offset correction) with the second conversion following the write to the ACR. Figure 9 describes the ACR address, format, and resolution. Table 3 shows the ACR's dynamic range for several different sense resistor options.

Figure 9. Accumulated Current Register Format

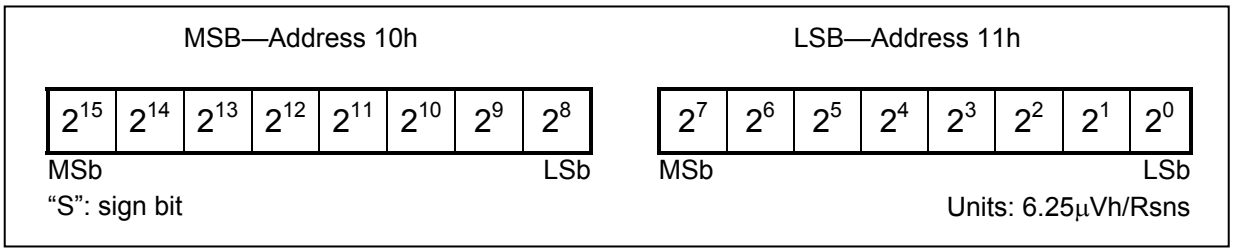


Table 3. Accumulated Current Range for Various RSNS Values

ACR RANGE				
V_{SS} - V_{SNS}	R_{SNS}			
	20mΩ	15mΩ	10mΩ	5mΩ
409.6mVh	20.48Ah	27.31Ah	40.96Ah	81.92Ah

CURRENT OFFSET BIAS

The Current Offset Bias register (COBR) allows a programmable offset value to be added to raw current measurements. The result of the raw current measurement plus the COBR value is displayed as the current measurement result in the CURRENT register, and is used for current accumulation. The COBR value can be used to correct for a static offset error, or can be used to intentionally skew the current results and therefore the current accumulation.

Read and write access is allowed to COBR. Whenever the COBR is written, the new value is applied to all subsequent current measurements. COBR can be programmed in 1.56μV steps to any value between +198μV and -200μV. The COBR value is stored as a two's complement value in volatile memory, and must be initialized via the interface on power-up. Figure 10 describes the COBR address, format, and resolution.

Figure 10. Current Offset Bias Register Format

Address 61h

S	2^6	2^5	2^4	2^3	2^2	2^1	2^0

MSb LSb

"S": sign bit Units: 1.56μV/Rsns

CURRENT BLANKING

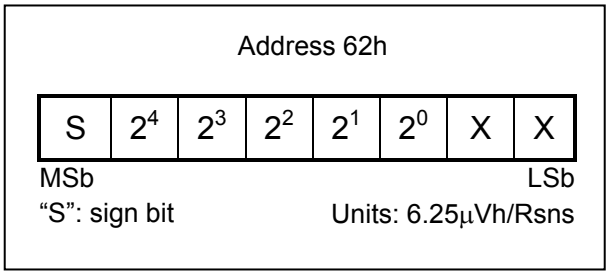
The Current Blanking feature modifies current measurement result prior to being accumulated in the ACR. Current Blanking occurs conditionally when a current measurement (raw current + COBR) falls in one of two defined ranges. The first range prevents charge currents less than $100\mu V/R_{SNS}$ from being accumulated. The second range prevents discharge currents less than $25\mu V/R_{SNS}$ in magnitude from being accumulated. Charge current blanking is always performed, however, discharge current blanking must be enabled by setting the NBEN bit in the Status/Config register. See the register description for additional information.

ACCUMULATION BIAS

The Accumulation Bias register (ABR) allows a programmable offset value to be added to the current accumulation process. The new ACR value results from the addition of the Current register value plus ABR plus the previous ACR value. ABR can be used to intentionally skew the current accumulation to estimate system stand-by currents that are too small to measure. ABR value is not subject to the Current Blanking thresholds.

Read and write access is allowed to the ABR. Whenever the ABR is written, the new value is applied to all subsequent current measurements. ABR can be set to any value between +193.75μV and -200μV in 6.25μV steps. The ABR value is stored as a two's complement value in volatile memory, and must be initialized via the interface on power-up. The lower two bits of the ABR register have no effect on the data. Figure 11 describes the ABR address, format, and resolution.

Figure 1. Accumulation Bias Register Format



MEMORY

The DS2746 has memory space with registers for instrumentation, status, and control. When the MSB of a two-byte register is read, both the MSB and LSB are latched and held for the duration of the read data command to prevent updates during the read and ensure synchronization between the two register bytes. For consistent results, always read the MSB and the LSB of a two-byte register during the same read data command sequence.

Table 4. Memory Map

ADDRESS (HEX)	DESCRIPTION	READ/WRITE	POR DEFAULT
00	Reserved	—	
01	Status/Config Register	R/W	X1110X00b
02 to 07	Reserved	—	
08	Auxiliary Input 0 Register MSB	R	00h
09	Auxiliary Input 0 Register LSB	R	00h
0A	Auxiliary Input 1 Register MSB	R	00h
0B	Auxiliary Input 1 Register LSB	R	00h
0C	Voltage Register MSB	R	00h
0D	Voltage Register LSB	R	00h
0E	Current Register MSB	R	00h
0F	Current Register LSB	R	00h
10	Accumulated Current Register MSB	R/W	Undefined
11	Accumulated Current Register LSB	R/W	Undefined
12 to 60	Reserved	—	
61	Offset Bias Register	R/W	00h
62	Accumulation Bias Register	R/W	00h
63 to FF	Reserved	—	

STATUS/CONFIG REGISTER

The Status/Config register is read/write with individual bits designated as read only. Bit values indicate status as well as program or select device functionality.

Figure 12. Status/Config Register Format

ADDRESS 01

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
X	PORF	SMOD	NBEN	VODIS	X	AIN1	AIN0

X — Reserved.

PORF — The Power-On-Reset Flag is set to indicate initial power-up. PORF is not cleared internally. The user must write this flag value to a 0 in order to use it to indicate subsequent power-up events. If PORF indicates a power-on-reset, the ACR could be misaligned with the actual battery state of charge. The system can request a charge to full in order to synchronize the ACR with the battery charge state. PORF is read/write-to-zero.

SMOD — SLEEP Mode Enable. A value of 1 allows the DS2746 to enter sleep mode when SCL AND SDA are low for t_{SLEEP}. A value of 0 disables the transition to sleep mode. The power-up default is SMOD = 1.

NBEN — Negative Blanking Enable. A value of 1 enables blanking of negative current values up to 25µV. A value of 0 disables blanking of negative currents. The power-up default is NBEN = 1.

V_{ODIS} – V_{OUT} Disable. When set to 0 this output is driven t_{PRE} before the AIN0 conversion begins, and disabled after the AIN1 conversion ends. The power-up default is V_{ODIS} = 0, a value of 1 disables the V_{OUT} output.

AIN1 – AIN1 Conversion Valid. This read only bit indicates that the V_{OUT} output was enabled, and a conversion has occurred on the AIN1 pin. When using the V_{ODIS} bit, before reading the AIN1 registers, read the AIN1 bit. Only once the AIN1 bit is set, should the AIN1 register be read.

AIN0 – AIN0 Conversion Valid. This read only bit indicates that the V_{OUT} output was enabled, and a conversion has occurred on the AIN0 pin. When using the V_{ODIS} bit, before reading the AIN0 registers, read the AIN0 bit. Only once the AIN0 bit is set, should the AIN0 register be read.

2-WIRE BUS SYSTEM

The 2-Wire bus system supports operation as a slave-only device in a single or multislave, and single or multimaster system. The 2-wire interface consists of a serial data line (SDA) and serial clock line (SCL). SDA and SCL provide bidirectional communication between the DS2746 slave device and a master device at speeds up to 400 kHz. The DS2746's SDA pin operates bidirectionally, that is, when the DS2746 receives data, SDA operates as an input, and when the DS2746 returns data, SDA operates as an open drain output, with the host system providing a resistive pullup. The DS2746 always operates as a slave device, receiving and transmitting data under the control of a master device. The master initiates all transactions on the bus and generates the SCL signal as well as the START and STOP bits which begin and end each transaction.

Bit Transfer

One data bit is transferred during each SCL clock cycle, with the cycle defined by SCL transitioning low-to-high and then high-to-low. The SDA logic level must remain stable during the high period of the SCL clock pulse. Any change in SDA when SCL is high is interpreted as a START or STOP control signal.

Bus Idle
The bus is defined to be idle, or not busy, when no master device has control. Both SDA and SCL remain high when the bus is idle. The STOP condition is the proper method to return the bus to the idle state.

START and STOP Conditions
The master initiates transactions with a START condition (S), by forcing a high-to-low transition on SDA while SCL is high. The master terminates a transaction with a STOP condition (P), a low-to-high transition on SDA while SCL is high. A REPEATED START condition (Sr) can be used in place of a STOP then START sequence to terminate one transaction and begin another without returning the bus to the idle state. In multimaster systems, a REPEATED START allows the master to retain control of the bus. The START and STOP conditions are the only bus activities in which the SDA transitions when SCL is high.

Acknowledge Bits
Each byte of a data transfer is acknowledged with an Acknowledge bit (A) or a No Acknowledge bit (N). Both the master and the DS2746 slave generate acknowledge bits. To generate an Acknowledge, the receiving device must pull SDA low before the rising edge of the acknowledge-related clock pulse (ninth pulse) and keep it low until SCL returns low. To generate a No Acknowledge (also called NAK), the receiver releases SDA before the rising edge of the acknowledge-related clock pulse and leaves SDA high until SCL returns low. Monitoring the acknowledge bits allows for detection of unsuccessful data transfers. An unsuccessful data transfer can occur if a receiving device is busy or if a system fault has occurred. In the event of an unsuccessful data transfer, the bus master should re-attempt communication.

Data Order
A byte of data consists of 8 bits ordered most significant bit (msb) first. The least significant bit (lsb) of each byte is followed by the Acknowledge bit. DS2746 registers composed of multibyte values are ordered most significant byte (MSB) first. The MSB of multibyte registers is stored on even data memory addresses.

Slave Address
A bus master initiates communication with a slave device by issuing a START condition followed by a Slave Address (SAddr) and the read/write (R/W) bit. When the bus is idle, the DS2746 continuously monitors for a START condition followed by its slave address. When the DS2746 receives a slave address that matches its Slave Address, it responds with an Acknowledge bit during the clock period following the R/W bit. The 7-bit Slave Address is fixed.

DS2746 Slave Address	0110110

Read/Write Bit
The R/W bit following the slave address determines the data direction of subsequent bytes in the transfer. R/W = 0 selects a write transaction, with the following bytes being written by the master to the slave. R/W = 1 selects a read transaction, with the following bytes being read from the stave by the master.

Bus Timing
The DS2746 is compatible with any bus timing up to 400kHz. No special configuration is required to operate at any speed.

2-Wire Command Protocols
The command protocols involve several transaction formats. The simplest format consists of the master writing the START bit, slave address, R/W bit, and then monitoring the acknowledge bit for presence of the DS2746. More complex formats such as the Write Data, Read Data and Function command protocols write data, read data and execute device specific operations. All bytes in each command format require the slave or host to return an Acknowledge bit before continuing with the next byte. Each function command definition outlines the required transaction format. The following key applies to the transaction formats.

Table 5. 2-Wire Protocol Key

KEY	DESCRIPTION	KEY	DESCRIPTION
S	START bit	Sr	Repeated START
SAddr	Slave Address (7-bit)	W	R/W bit = 0
FCmd	Function Command byte	R	R/W bit = 1
MAddr	Memory Address byte	P	STOP bit
Data	Data byte written by master	Data	Data byte returned by slave
A	Acknowledge bit - Master	A	Acknowledge bit - Slave
N	No Acknowledge - Master	N	No Acknowledge - Slave

Basic Transaction Formats

Write: S SAddr W A MAddr A Data0 A P

A write transaction transfers one or more data bytes *to* the DS2746. The data transfer begins at the memory address supplied in the MAddr byte. Control of the SDA signal is retained by the master throughout the transaction, except for the Acknowledge cycles.

Read: S SAddr W A MAddr A Sr SAddr R A Data0 N P

Write Portion Read Portion

A read transaction transfers one or more bytes *from* the DS2746. Read transactions are composed of two parts, a write portion followed by a read portion, and is therefore inherently longer than a write transaction. The write portion communicates the starting point for the read operation. The read portion follows immediately, beginning with a REPEATED START, Slave Address with R/W set to a 1. Control of SDA is assumed by the DS2746 beginning with the Slave Address Acknowledge cycle. Control of the SDA signal is retained by the DS2746 throughout the transaction, except for the Acknowledge cycles. The master indicates the end of a read transaction by responding to the last byte it requires with a No Acknowledge. This signals the DS2746 that control of SDA is to remain with the master following the Acknowledge clock.

Write Data Protocol

The write data protocol is used to write to register and shadow RAM data to the DS2746 starting at memory address MAddr. Data0 represents the data written to MAddr, Data1 represents the data written to MAddr + 1 and DataN represents the last data byte, written to MAddr + N. The master indicates the end of a write transaction by sending a STOP or REPEATED START after receiving the last acknowledge bit.

S SAddr W A MAddr A Data0 A Data1 A … DataN A P

The msb of the data to be stored at address MAddr can be written immediately after the MAddr byte is acknowledged. Because the address is automatically incremented after the least significant bit (lsb) of each byte is received by the DS2746, the msb of the data at address MAddr + 1 is can be written immediately after the acknowledgement of the data at address MAddr. If the bus master continues an auto-incremented write transaction beyond address 4Fh, the DS2746 ignores the data. Data is also ignored on writes to read-only addresses and reserved addresses, locked EEPROM blocks as well as a write that auto increments to the Function Command register (address FEh). Incomplete bytes and bytes that are Not Acknowledged by the DS2746 are not written to memory. As noted in the Memory Section, writes to unlocked EEPROM blocks modify the shadow RAM only.

Read Data Protocol

The Read Data protocol is used to read register and shadow RAM data from the DS2746 starting at memory address specified by MAddr. Data0 represents the data byte in memory location MAddr, Data1 represents the data from MAddr + 1 and DataN represents the last byte read by the master.

S SAddr W A MAddr A Sr SAddr R A Data0 A Data1 A … DataN N P

Data is returned beginning with the most significant bit (msb) of the data in MAddr. Because the address is automatically incremented after the least significant bit (lsb) of each byte is returned, the msb of the data at address MAddr + 1 is available to the host immediately after the acknowledgement of the data at address MAddr. If the bus master continues to read beyond address FFh, the DS2746 outputs data values of FFh. Addresses labeled "Reserved" in the memory map return undefined data. The bus master terminates the read transaction at any byte boundary by issuing a No Acknowledge followed by a STOP or REPEATED START.

PACKAGE INFORMATION

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PACKAGE TYPE	PACKAGE CODE	DOCUMENT NO.
10 TDFN	T1033+1	**21-0137**

REVISION HISTORY

REVISION DATE	DESCRIPTION	PAGES CHANGED
051209	Changed the V_{DD} maximum operating range in the *Electrical Characteristics* table to 4.5V.	2, 3
	Added "V_{IN} pin is limited to V_{DD} voltage" text in the *Voltage Measurement* section.	8

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