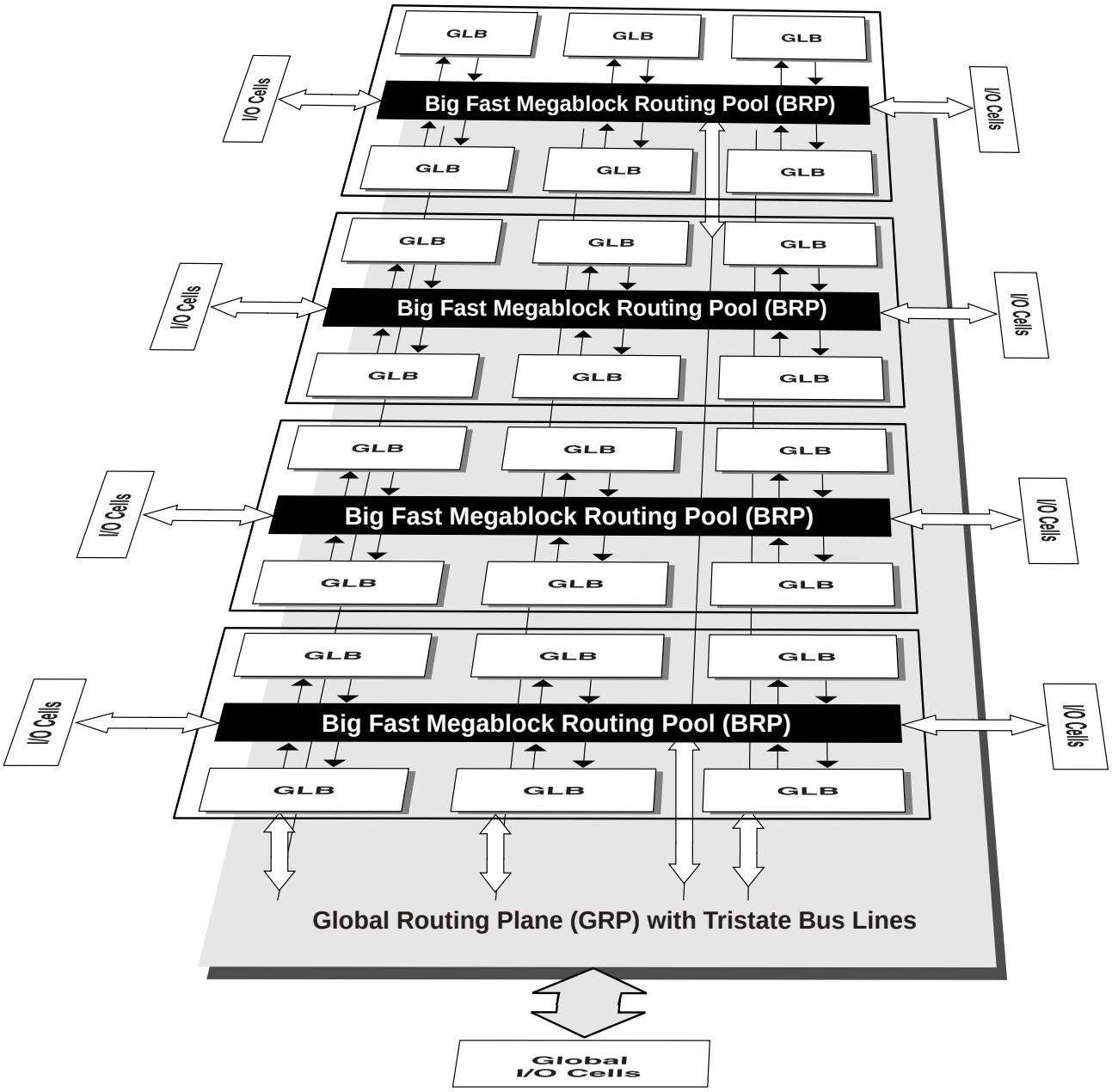
Functional Block Diagram

Figure 1. ispLSI 8840 Functional Block Diagram (Perspective)



ispLSI 8000 Family Description (Continued)

any or all the Big Fast Megablocks in the device. This mechanism allows fast, efficient connections, both within the Big Fast Megablocks and between them.

Each GLB contains 20 macrocells and a fully populated, programmable AND-array with 82 logic product terms. The GLB has 44 inputs from the Big Fast Megablock Routing Pool which are available in both true and complement form for every product term. Up to 20 of these inputs can be switched to provide local feedback into the GLB for logic functions that require it. The 80 general-purpose product terms can be grouped into 20 sets of four and sent into a Product Term Sharing Array (PTSA) which allows sharing up to a maximum of 28 product terms for a single function. Alternatively, the PTSA can be bypassed for functions of four product terms or less.

The 20 registered macrocells in the GLB are driven by the 20 outputs from the PTSA or the PTSA bypass. Each macrocell contains a programmable XOR gate, a programmable register/latch/toggle flip-flop and the necessary clocks and control logic to allow combinatorial or registered operation. Each macrocell has two outputs, one output can be fed back inside the GLB to the AND-array, while the other output drives both the Big Fast Megablock Routing Pool and the Global Routing Plane. This dual output capability from the macrocell allows efficient use of the hardware resources. One output can be a registered function for example, while the other output can be an unrelated combinatorial function.

Macrocell registers can be clocked from one of several global, local or product term clocks available on the device. A global, local and product term clock enable is also provided, eliminating the need to gate the clock to the macrocell registers. Reset and preset for the macrocell register is provided from both global and product term signals. The polarity of all of these control signals is selectable on an individual macrocell basis. The macrocell register can be programmed to operate as a D-type register, a D-type flow-through latch or a T-type flip flop.

The 20 outputs from the GLB can drive both the Big Fast Megablock Routing Pool within the Big Fast Megablock and the Global Routing Plane between the Big Fast Megablocks. The Big Fast Megablock Routing Pool contains general purpose tracks which interconnect the six GLBs within the Big Fast Megablock and dedicated tracks for the signals from the Big Fast Megablock I/O cells. The Global Routing Plane contains general purpose tracks that interconnect the Big Fast Megablocks and also carry the signals from the I/Os connected to the Global Routing Plane.

Control signals for the I/O cell registers are generated using an extra product term within each GLB, or using dedicated input pins. Each GLB has two extra product terms beyond the 80 available for the macrocell logic. The first additional product term is used as an optional shared product term clock for all the macrocells within the GLB. The second additional product term is then routed to an I/O Control Bus using a separate routing structure from the Big Fast Megablock Routing Pool and Global Routing Plane. Use of a separate control bus routing structure allows the I/O registers to have many control signals with no impact on the interconnection of the GLBs and Big Fast Megablocks. The I/O Control Bus is split into four quadrants, each servicing the I/O cell control requirements for one edge of the device. Signals in the control bus can be independently selected by any or all I/O cells to act as clock, clock enable, output enable, reset or preset.

Each Big Fast Megablock has 24 I/O cells. The Global Routing Pool has 144 I/O cells. Each I/O cell can be configured as a combinatorial input, combinatorial output, registered input, registered output or bidirectional I/O. I/O cell registers can be clocked from one of several global, local or product term clocks which are selected from the I/O control bus. A global and product term clock enable is also provided, eliminating the need for the user to gate the clock to the I/O cell registers. Reset and preset for the I/O cell register is provided from both global and product term signals. The polarity of all of these control signals is selectable on an individual I/O cell basis. The I/O cell register can be programmed to operate as a D-type register or a D-type latch.

Inputs and outputs are PCI compatible. The input threshold is fixed at TTL levels. The output driver can source 4mA and sink 8mA. The output drivers have a separate VCCIO power supply which is independent of the main VCC supply for the device. This feature allows the output drivers to run from either 5V or 3.3V while the device logic is always powered from 5V. The output drivers also provide individually programmable edge rates and open drain capability. A programmable pullup resistor is provided to tie off unused inputs and a programmable bus-hold latch is available to hold tristate outputs in their last valid state until the bus is driven again by another device.

The ispLSI 8000 Family features 5V, non-volatile in-system programmability for both the logic and the interconnect structures, providing the means to develop truly reconfigurable systems. Programming is achieved

ispLSI 8000 Family Description (Continued)

through the industry standard IEEE 1149.1-compliant Boundary Scan interface using either the JTAG protocol or Lattice proprietary ISP protocol. Boundary Scan test is also supported through the same interface.

An enhanced, multiple cell security scheme is provided that prevents reading of the JEDEC programming file when secured. After the device has been secured using this mechanism, the only way to clear the security is to execute a bulk-erase instruction.

ispLSI 8840 Description

The ispLSI 8840 device has seven Big Fast Megablocks for a total of 7 x 120 = 840 macrocells.

Each Big Fast Megablock has a total of 24 I/O cells and the Global Routing Plane has a total of 144 I/O cells. This gives (7 x 24) + 144 = 312 I/Os.

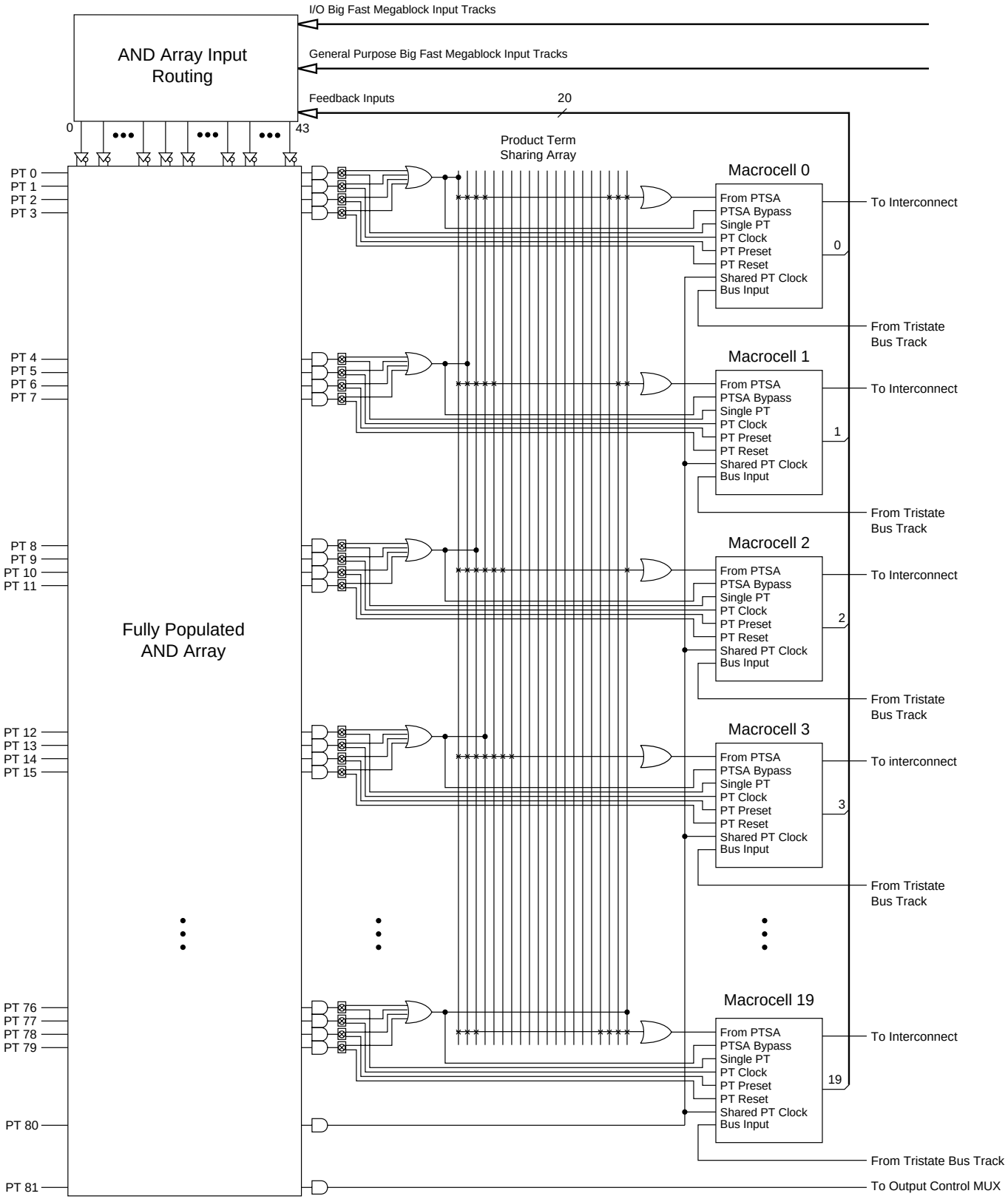
The total registers in the device is the sum of macrocells plus I/O cells, 840 + 312 = 1152 registers.

Embedded Tristate Bus

There is a 108-line embedded internal tristate bus as part of the Global Routing Plane (GRP), enabling multiple GLBs to drive the same tracks. This bus can be partitioned into various bus widths such as twelve 9-line buses, six 18-line buses or three 36-line buses. The GLBs can dynamically share a subset of the Global Routing Plane tracks. This feature eliminates the need to convert tristate buses to wide multiplexers on the programmable device. Up to 18 macrocells per GLB can participate in driving the embedded tristate bus. The remaining two macrocells per GLB are used to generate the internal tristate driver control signals on each data byte (with parity). The embedded tristate bus can also be configured as an extension of an external tristate bus using the bidirectional capability of the I/O cells connected to the Global Routing Plane. The Global Routing Plane I/Os 0-8 and 15-23 from each group (I/OGx as defined in the I/O Pin Location Table) can connect to the internal tristate bus as well as the unidirectional/non-tristate global routing channels. I/Os 9-14 connect only to the global routing channel.

The embedded tristate bus has internal bus hold and arbitration features in order to make the function more “user friendly”. The bus hold feature keeps the internal bus at the previously driven logic state when the bus is not driven to eliminate bus float. The bus arbitration is performed on a “first come, first served” priority. In other words, once a logic block drives the bus, other logic blocks cannot drive the bus until the first releases the bus. This arbitration feature prevents internal bus contention when there is an overlap between two bus enable signals. Typically, it takes about 3ns to resolve one bus signal coming off the bus to another bus signal driving the bus. The arbitration feature combined with the predictability of CPLD, makes the embedded tristate bus the most practical for the real world bus implementations.

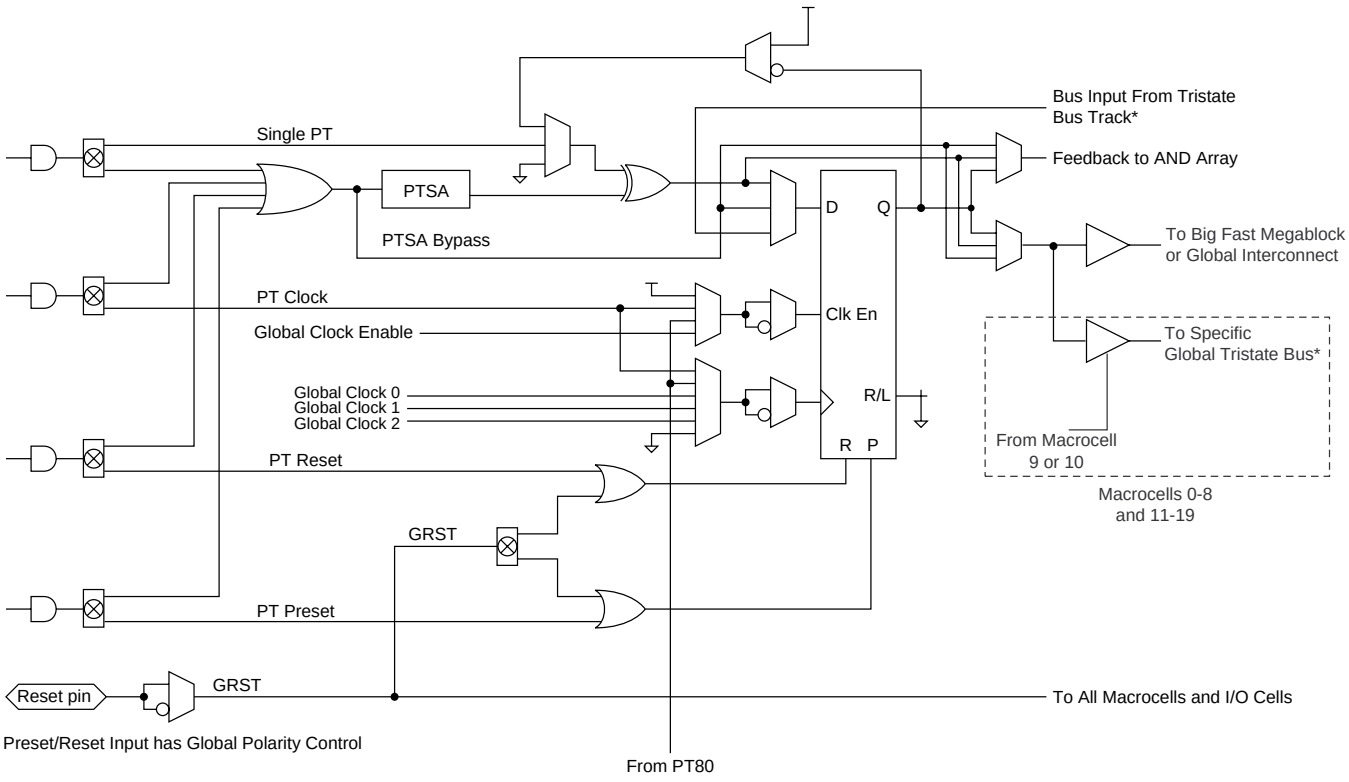
Figure 2. ispLSI 8000 GLB Overview



Note: Macrocells 9 and 10 do not support Tristate Bus Feedback.

⊠ Function Selector (E^2 Cell Controlled)

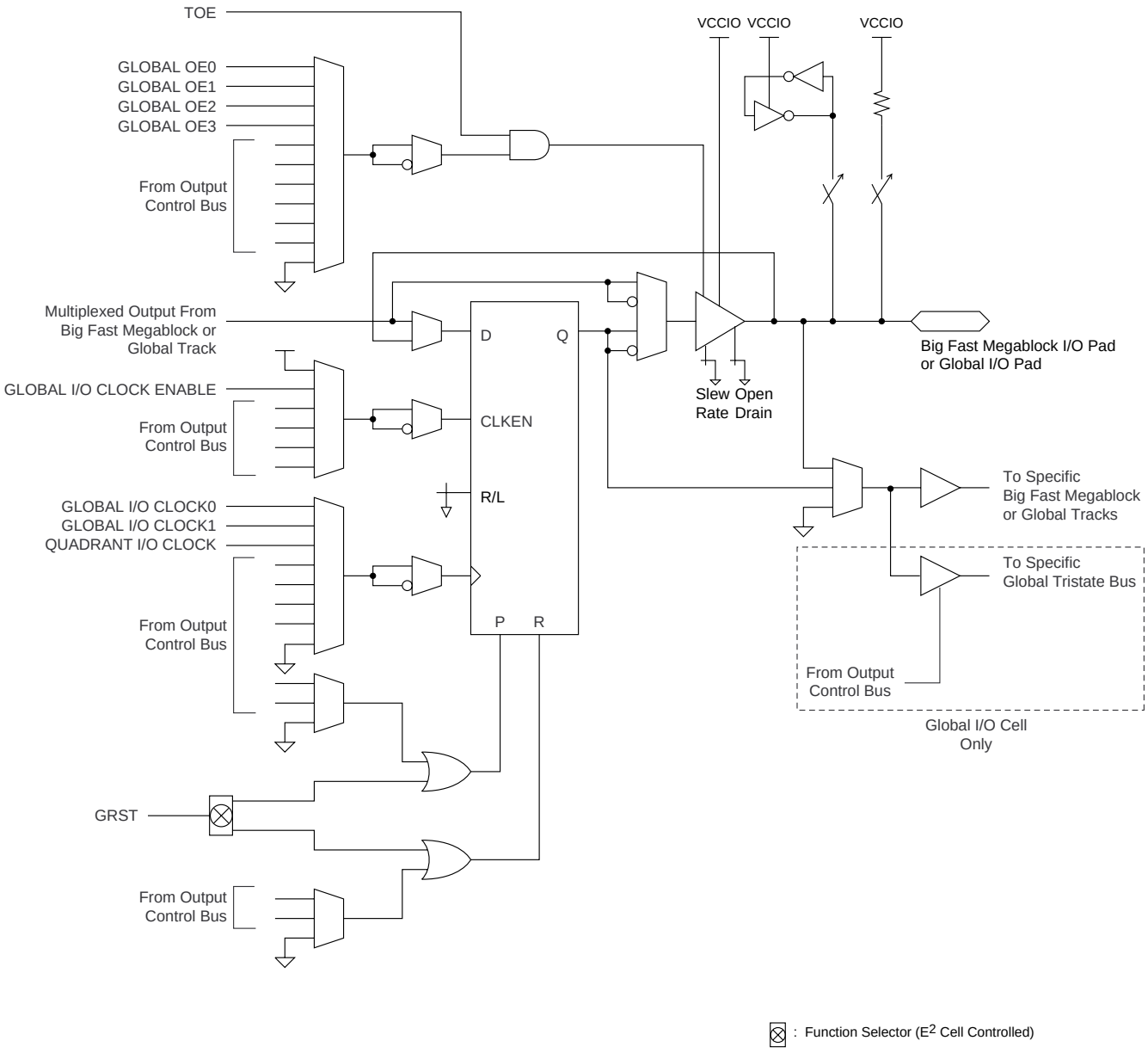
Figure 3. ispLSI 8000 Macrocell Overview



*Not available for Macrocells 9 and 10.

⊗ : Function Selector (E^2 Cell Controlled)

Figure 4. ispLSI 8000 I/O Cell



Output Control Organization

In addition to the data input and output to the I/O cells, each I/O cell can have up to six different I/O cell control signals. In addition to the internal OE control, the five control signals for each I/O cell consist of pin OE control, clock enable, clock input, asynchronous preset and asynchronous reset. All of the I/O control signals can be driven either from the dedicated external input pins or from the internal control bus.

The output enable of each I/O cell can be driven by 21 different sources – 16 from the output control bus, four from the Global OE pins and one from the Test OE pin. The Global OE signals and Test OE signal are driven from the dedicated external control input pins.

The 16-bit wide output control buses are organized in four different quadrants as shown in Figure 5. Since each GLB is capable of generating the output control signals, each of the output control bus signals can be driven from a unique GLB. The 42 GLBs can generate a total of 42 unique I/O control signals. Referring to Figure 2, the GLB generates its output control signal from control product term (PT81).

Figure 5 also illustrates how the quadrant clocks are routed to the appropriate quadrant I/O cells.

Figure 5. Output Control Bus and Quadrant Organization

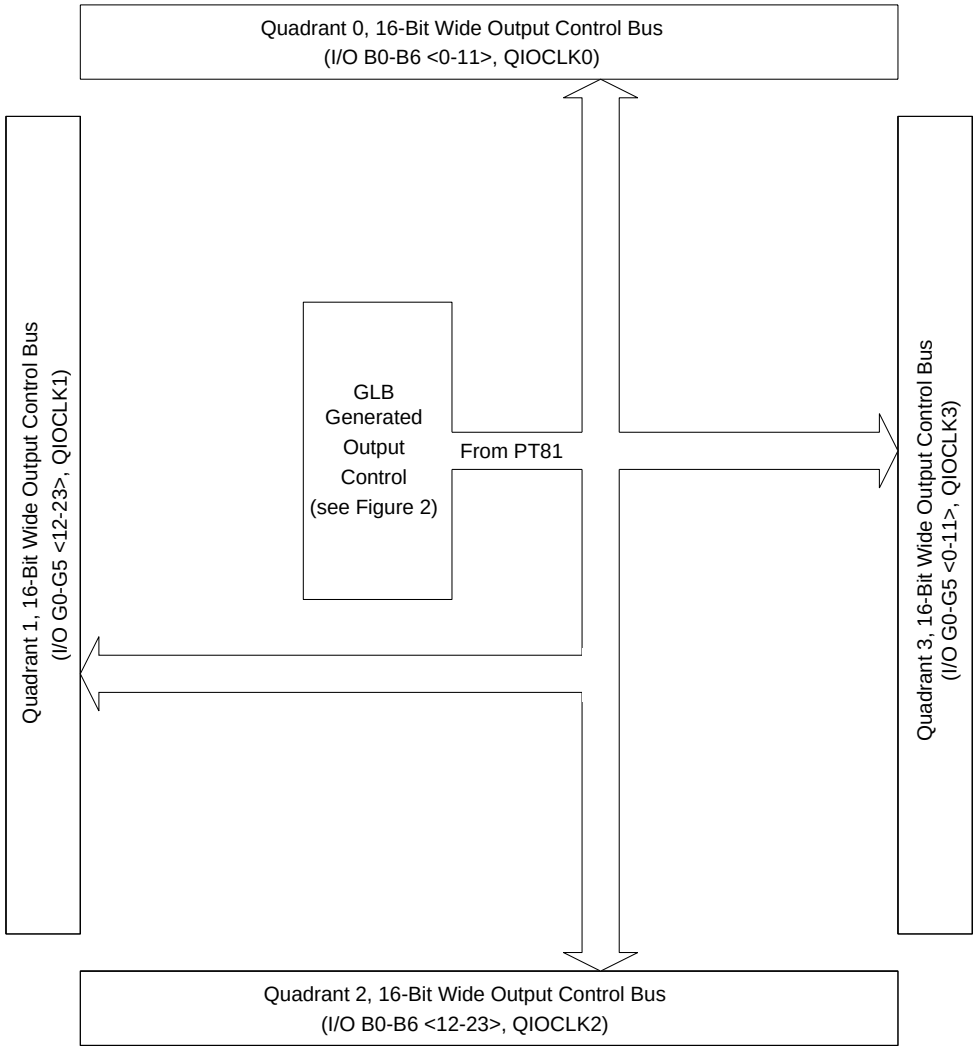
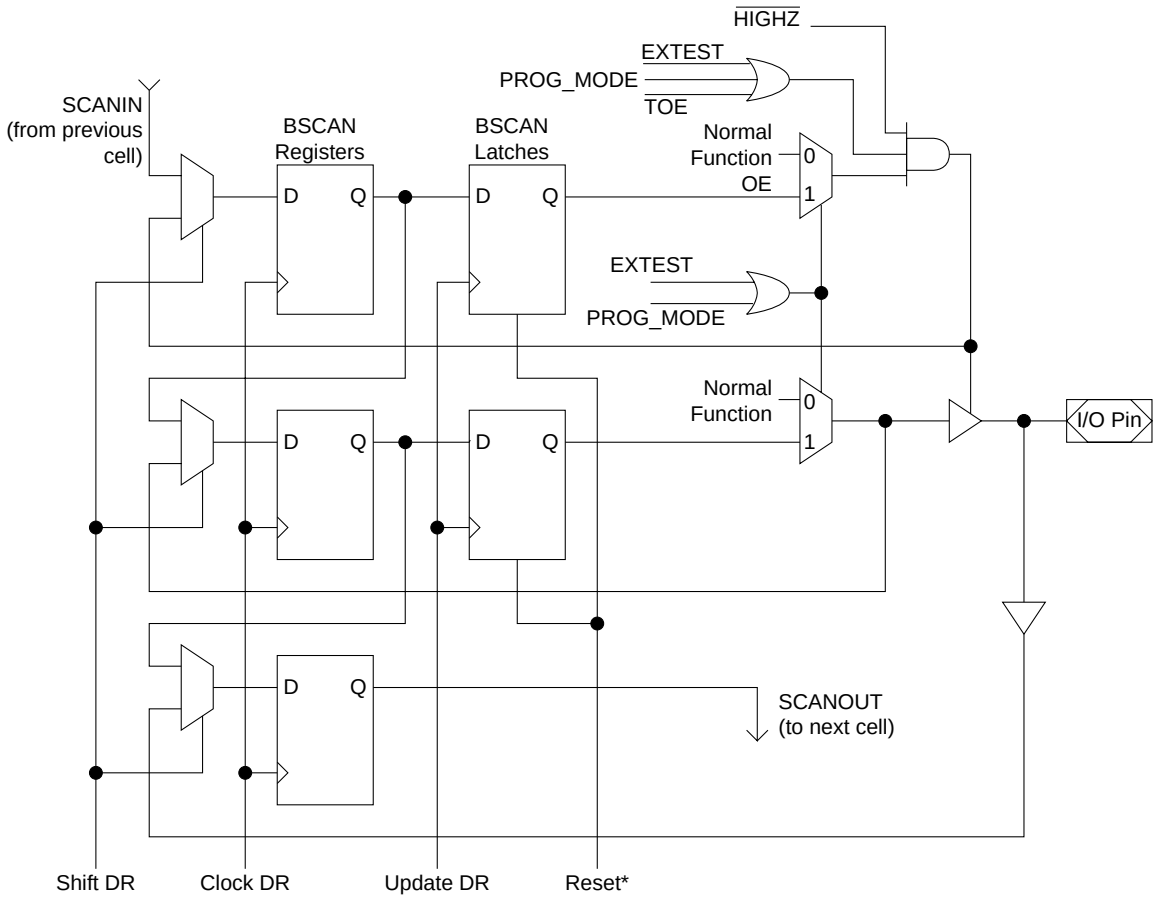


Figure 6. Boundary Scan Register Circuit for I/O Pins



*Internal power-up reset signal. Not connected to external reset pin.

Figure 7. Boundary Scan Register Circuit for Input-Only Pins

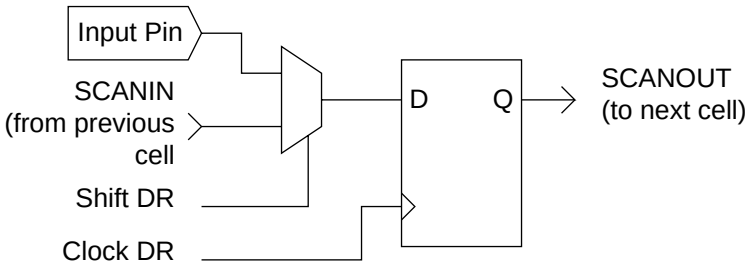
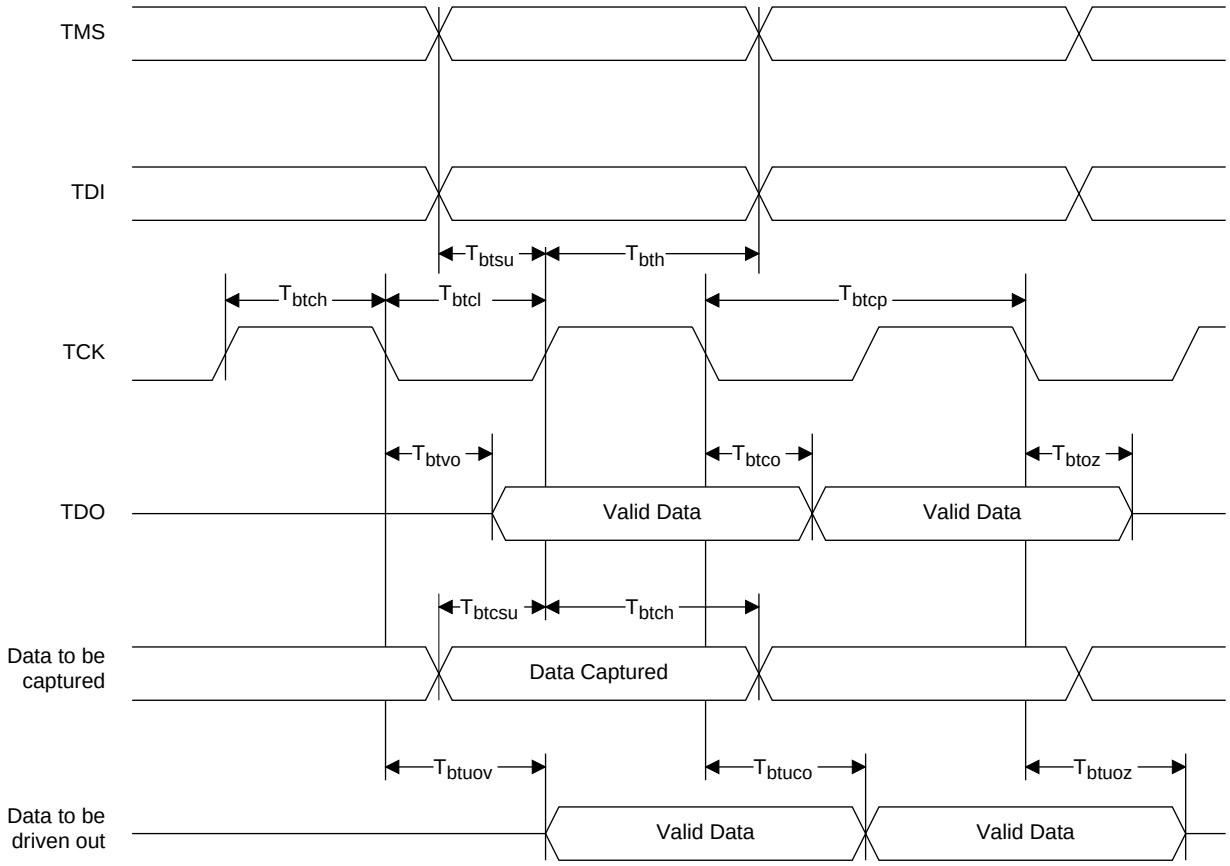


Figure 8. Boundary Scan Waveforms and Timing Specifications



SYMBOL	PARAMETER	MIN	MAX	UNITS
tbtcp	TCK Clock Pulse Width	0.1	400	µs
tbtch	TCK Pulse Width High	0.05	200	µs
tbtcl	TCK Pulse Width Low	0.05	200	µs
tbtsu	TDI, TMS Setup Time to TCK	25	—	ns
tbth	TDI, TMS Hold Time from TCK	25	—	ns
trf	TCK, TDI, TMS Rise and Fall Time	50	—	mV/ns
tbtco	TAP Controller, TCK to TDO Valid	—	25	ns
tbtoz	TAP Controller, TCK to TDO High-Impedance	—	25	ns
tbtvo	TAP Controller, TCK to TDO High-Impedance to Valid Output	—	25	ns
tbtcsu	BSCAN Test Capture Register Setup Time	20	—	ns
tbtch	BSCAN Test Capture Register Hold Time	25	—	ns
tbtuco	BSCAN Test Update Register Clock to Valid Output	—	25	ns
tbtuoz	BSCAN Test Update Register Clock to High-Impedance	—	25	ns
tbtuov	BSCAN Test Update Register High-Impedance to Valid Output	—	25	ns

Table 2-0010/8840

Absolute Maximum Ratings [1,2]

Supply Voltage V_{CC} ..... -0.5 to +7.0V

Input Voltage Applied ..... -2.5 to V_{CC} +1.0V

Tri-Stated Output Voltage Applied .... -2.5 to V_{CC} +1.0V

Storage Temperature ..... -65 to 150°C

Case Temp. with Power Applied ..... -55 to 125°C

Max. Junction Temp. (T_J) with Power Applied ... 140°C

1. Stresses above those listed under the "Absolute Maximum Ratings" may cause permanent damage to the device. Functional operation of the device at these or at any other conditions above those indicated in the operational sections of this specification is not implied (while programming, follow the programming specifications).
2. Compliance with the Thermal Management section of the Lattice Semiconductor Data Book or CD-ROM is a requirement.

DC Recommended Operating Condition

SYMBOL	PARAMETER		MIN.	MAX.	UNITS
V_{CC}	Supply Voltage	Commercial T_A = 0°C to 70°C	4.75	5.25	V
V_{CCIO}	Output Supply Voltage		3.0	5.25	V
V_{IH}	Input High Voltage		2.0	V_{CC} +1	V
V_{IL}	Input Low Voltage		0.0	0.8	V
V_{OH}	Output High Voltage		2.4	—	V
V_{OL}	Output Low Voltage		—	0.4	V

Table 2-0005/8840

Capacitance (T_A=25°C,f=1.0 MHz)

SYMBOL	PARAMETER	TYPICAL	UNITS	TEST CONDITIONS
C_1	I/O Capacitance	10	pf	V_{CC} = 5.0V, $V_{I/O}$ = 2.0V
C_2	Clock Capacitance	10	pf	V_{CC} = 5.0V, V_{CK} = 2.0V
C_3	Global Input Capacitance	10	pf	V_{CC} = 5.0V, V_G = 2.0V

Table 2-0006/8840

Erase/Reprogram Specification

PARAMETER	MINIMUM	MAXIMUM	UNITS
ispLSI Erase/Reprogram Cycles	10000	–	Cycles

Table 2-0008/3320

Switching Test Conditions

Input Pulse Levels	GND to 3.0V
Input Rise and Fall Time	≤ 1.5 ns 10% to 90%
Input Timing Reference Levels	1.5V
Ouput Timing Reference Levels	1.5V
Output Load	See Figure 2

Table 2-0003/8840

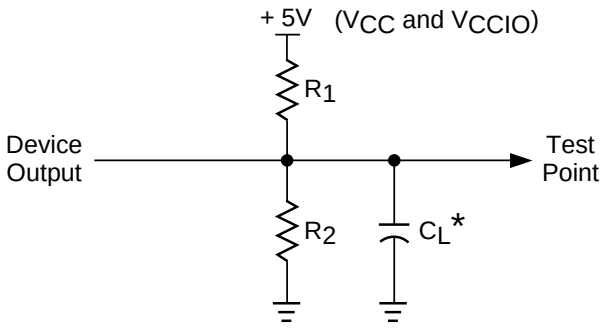
3-state levels are measured 0.5V from steady-state active level.

Output Load Conditions (See Figure 9)

TEST CONDITION		R1	R2	CL
A		470Ω	390Ω	35pF
B	Active High	∞	390Ω	35pF
	Active Low	470Ω	390Ω	35pF
C	Active High to Z at V_{OH} -0.5V	∞	390Ω	5pF
	Active Low to Z at V_{OL} +0.5V	470Ω	390Ω	5pF

Table 2-0004A/8840

Figure 9. Test Load



*C_L includes Test Fixture and Probe Capacitance.

0213A/8840

DC Electrical Characteristics

Over Recommended Operating Conditions

SYMBOL	PARAMETER	CONDITION		MIN.	TYP.[3]	MAX.	UNITS
V_{OL}	Output Low Voltage	I_{OL} = 8 mA		–	–	0.4	V
V_{OH}	Output High Voltage	I_{OH} = -4 mA		2.4	–	–	V
I_{IL}	Input or I/O Low Leakage Current	0.0V ≤ V_{IN} ≤ 0.8V		–	–	-10	µA
I_{IH}	Input or I/O High Leakage Current	3.5V ≤ V_{IN} ≤ V_{CC} V_{CCIO} = 5V		–	–	10	µA
		(V_{CCIO} - 0.2) ≤ V_{IN} ≤ V_{CCIO} V_{CCIO} = 3.3V		–	–	10	µA
		V_{CCIO} < V_{IN} ≤ 5.25V V_{IN} >V_{CCIO}		–	–	10	µA
I_{PU}	Active Pullup Current, Input or I/O	0V ≤ V_{IN} ≤ 2.0V		-10	–	-250	µA
I_{BHL}	Bus-Hold Low Sustaining Current	V_{IN} = 0.8V		50	–	–	µA
I_{BHH}	Bus-Hold High Sustaining Current	V_{IN} = 2.0V		-50	–	–	µA
I_{BHLO}	Bus-Hold Low, Overdrive Current	0V ≤ V_{IN} ≤ V_{CCIO}		–	–	550	µA
I_{BHHO}	Bus-Hold High, Overdrive Current	0V ≤ V_{IN} ≤ V_{CCIO}		–	–	-550	µA
V_{BHT}	Bus-Hold Trip Point (1.4V Nominal)			0.8	–	2.0	V
I_{OS}[1]	Output Short Circuit Current	V_{CC} = 5V, V_{OUT} = 0.5V		–	–	-200	mA
I_{CC}[2,4]	Operating Power Supply Current	V_{IL} = 0.0V, V_{IH} = 3.0V	High Speed Mode	–	630	–	mA
		f_{CLOCK} = 1MHz	Low Power Mode	–	340	–	mA

Table 2-0007/8840

1. One output at a time for a maximum duration of one second. V_{OUT} = 0.5V was selected to avoid test problems by tester ground degradation. Characterized but not 100% tested.
2. Measured using 42 20-bit counters.
3. Typical values are at V_{CC} = 5V and T_A = 25°C.
4. Maximum I_{CC} varies widely with specific device configuration and operating frequency.

External Switching Characteristics[1]

Over Recommended Operating Conditions

PARAMETER	TEST COND.[4]	#[2]	DESCRIPTION	-110		-90		-60		UNITS
				MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
t_{pd1}	A	1	Prop Delay, BFM Input to Same BFM Output, 4 PT Bypass	–	8.5	–	10.0	–	15.0	ns
t_{pd2}	A	2	Prop Delay, Global Input to Global Output	–	13.5	–	16.0	–	24.0	ns
f_{max}	–	3	Clk Frequency, Local Feedback, Same GLB [3]	110	–	90.0	–	60.0	–	MHz
t_{suq}	–	4	I/O Cell Reg, Data Setup Time, Quadrant I/O Clock	6.0		8.0	–	12.0	–	ns
t_{hq}	–	5	I/O Cell Reg, Data Hold Time, Quadrant I/O Clock	0.0	–	0.0	–	0.0	–	ns
t_{coq}	A	6	I/O Cell Reg, Quadrant Clock to Output Delay	–	4.5	–	6.0	–	9.0	ns
t_{sug}	–	7	I/O Cell Reg, Data Setup Time, Global I/O Clock	4.5	–	6.0	–	9.0	–	ns
t_{hg}	–	8	I/O Cell Reg, Data Hold Time, Global I/O Clock	0.0	–	0.0	–	0.0	–	ns
t_{cog}	A	9	I/O Cell Reg, Global Clock to Output Delay	–	6.0	–	7.5	–	11.0	ns
t_{su1}	–	10	GLB Reg Setup, BFM Input to Same BFM GLB, 4 PT Bypass	5.0	–	7.0	–	10.0	–	ns
t_{h1}	–	11	GLB Reg Hold Time, BFM Input to Same BFM GLB	0.0	–	0.0	–	0.0	–	ns
t_{co1}	A	12	GLB Reg, Global Clock to Same BFM Output Delay	–	8.0	–	10.0	–	15.0	ns
t_{suceq}	–	13	I/O Cell Reg, CLKEN Setup Time, Quadrant I/O Clock	5.0	–	6.5	–	9.5	–	ns
t_{hceq}	–	14	I/O Cell Reg, CLKEN Hold Time, Quadrant I/O Clock	0.0	–	0.0	–	0.0	–	ns
t_{suceg}	–	15	GLB Reg, CLKEN Setup Time, Global Clock	3.5	–	4.5	–	6.5	–	ns
t_{hceg}	–	16	GLB Reg, CLKEN Hold Time, Global Clock	0.0	–	0.0	–	0.0	–	ns
t_{goe}	B/C	17	Global Output Enable/Disable Delay	–	8.0	–	10.0	–	15.0	ns
t_{rglb}	–	18	Global Reset/Preset Time, GLB Reg	–	12.0	–	15.0	–	22.0	ns
t_{rio}	–	19	Global Reset/Preset Time, I/O Cell Reg	–	8.0	–	10.0	–	15.0	ns
t_{rw}	–	20	Global Reset/Preset Pulse Duration	5.0	–	6.5	–	9.5	–	ns
t_{wh}	–	21	Global or Quadrant Clock Pulse, High Duration	4.0	–	6.0	–	9.0	–	ns
t_{wl}	–	22	Global or Quadrant Clock Pulse, Low Duration	4.0	–	6.0	–	9.0	–	ns

Table 2-0030/8840

1. Unless noted otherwise, all parameters use PTSA and CLK0.
2. Refer to Timing Model in this data sheet for further details.
3. Standard 20-bit counter with local feedback.
4. Refer to Switching Test Conditions section.

Internal Timing Parameters

Over Recommended Operating Conditions

PARA-METER	#[2]	DESCRIPTION	-110		-90		-60		UNITS
			MIN	MAX	MIN	MAX	MIN	MAX	
I/O Cell Delay									
tidcom	23	Input Pad and Input Buffer, Combinatorial Input	–	0.1	–	0.1	–	0.2	ns
tidreg	24	Input Pad and Input Buffer, Registered Input	–	8.0	–	9.4	–	13.9	ns
tobp	25	Output Register/Latch Bypass to Output Buffer	–	0.0	–	0.0	–	0.0	ns
tibp	26	Input Register/Latch Bypass to BFM Routing or GRP	–	0.2	–	0.2	–	0.4	ns
tiolat	27	I/O Cell Latch, Transparent Mode	–	2.0	–	2.4	–	3.6	ns
tioco	28	I/O Cell Register/Latch, Clk/Gate to Output	–	1.0	–	1.2	–	2.0	ns
tiosu	29	I/O Cell Register/Latch, Setup Time	0.4	–	0.7	–	1.4	–	ns
tioh	30	I/O Cell Register/Latch, Hold Time	4.1	–	4.4	–	6.9	–	ns
tiorst	31	I/O Cell Register/Latch, Reset or Set Time	–	2.3	–	2.9	–	4.4	ns
tiosuce	32	I/O Cell Register/Latch, Setup Time for Clk Enable	2.6	–	2.7	–	3.8	–	ns
tiohce	33	I/O cell Register/Latch, Hold Time for Clk Enable	1.9	–	1.9	–	2.9	–	ns
todreg	34	I/O Cell Output Buffer Delay, Registered Output	–	1.1	–	1.3	–	1.9	ns
todcom	35	I/O Cell Output Buffer Delay, Combinatorial Output	–	1.7	–	2.0	–	3.0	ns
todz	36	Output Driver Disable Time	–	2.0	–	2.3	–	3.5	ns
tslf	37	Slew Rate Adder, Fast Slew Rate	–	0.0	–	0.0	–	0.0	ns
tsls	38	Slew Rate Adder, Slow Slew Rate	–	5.0	–	5.0	–	7.5	ns
GLB / Macrocell Delay									
tandhs	39	AND Array, High Speed Mode	–	3.6	–	4.2	–	6.4	ns
tandlp	40	AND Array, Low Power Mode	–	7.1	–	8.4	–	12.6	ns
t1pt	41	Single Product Term Bypass	–	3.6	–	4.3	–	6.2	ns
t4ptcom	42	Four Product Term Bypass, Combinatorial Macrocell	–	0.2	–	0.3	–	0.4	ns
t4ptreg	43	Four Product Term Bypass, Registered Macrocell	–	3.4	–	4.4	–	6.1	ns
tptsa	44	Product Term Sharing Array	–	3.7	–	4.5	–	6.8	ns
tmbp	45	Macrocell Register/Latch Bypass	–	0.0	–	0.0	–	0.0	ns
tmlat	46	Macrocell Latch, Transparent Mode	–	0.2	–	0.3	–	0.9	ns
tmco	47	Macrocell Register/Latch, Clk/Gate to Output	–	0.2	–	0.3	–	0.5	ns
tmsu	48	Macrocell Register/Latch, Setup Time	0.4	–	0.8	–	1.2	–	ns
tmh	49	Macrocell Register/Latch, Hold Time	3.8	–	4.5	–	6.1	–	ns
tmrst	50	Macrocell Register/Latch, Reset or Set Time	–	4.0	–	5.2	–	7.3	ns
tmsuce	51	Macrocell Register/Latch, Setup Time for Clk Enable	1.7	–	1.8	–	2.4	–	ns
tmhce	52	Macrocell Register/Latch, Hold Time for Clk Enable	1.0	–	0.9	–	1.3	–	ns
tftog	53	Toggle Flip-Flop Feedback	–	3.9	–	4.7	–	6.8	ns
tfloc	54	Local Feedback to AND Array	–	1.1	–	1.3	–	1.9	ns
tpck	55	Single Product Term, Clk	1.0	2.5	1.5	3.5	2.3	5.3	ns
tpcken	56	Single Product Term, Clk Enable	–	2.6	–	3.1	–	4.6	ns
tsck	57	Shared Product Term, Clk	1.6	2.4	1.8	2.5	2.7	3.8	ns
tscken	58	Shared Product Term, Clk Enable	–	2.4	–	2.5	–	3.8	ns
tprst	59	Single Product Term, Reset or Set Delay	–	1.7	–	2.0	–	3.0	ns
trdir	60	Macrocell Register, Direct Input from GRP	–	1.8	–	2.1	–	2.7	ns

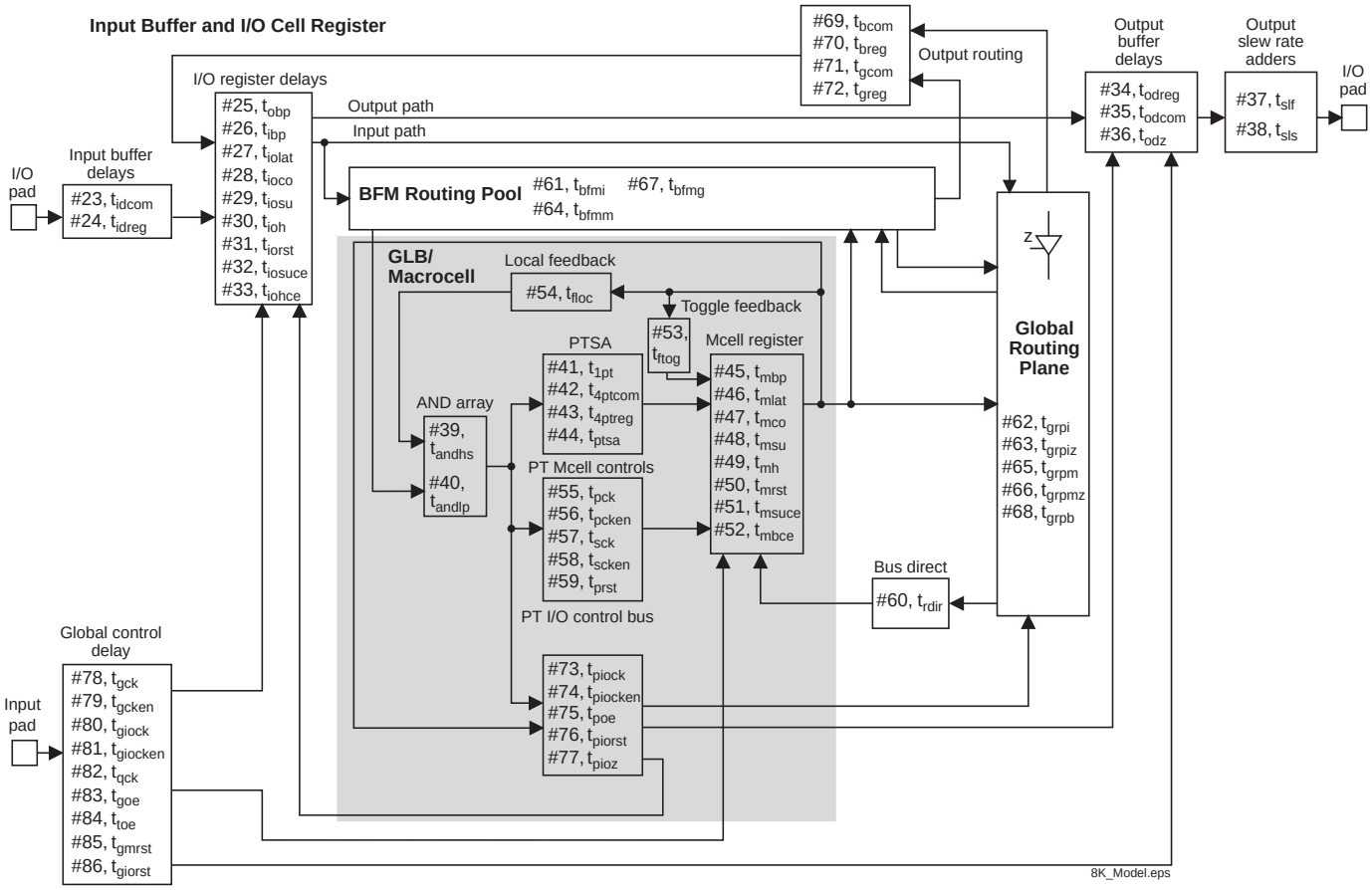
Internal Timing Parameters

Over Recommended Operating Conditions

PARA-METER	#[2]	DESCRIPTION	-110		-90		-60		UNITS
			MIN	MAX	MIN	MAX	MIN	MAX	
BFM / Global Routing Pool Delay									
tbfmi	61	BFM Routing Delay, Signal from I/O Cell	–	0.2	–	0.3	–	0.4	ns
tgrpi	62	GRP Delay, Signal from I/O Cell	–	0.2	–	0.2	–	0.4	ns
tgrpiz	63	Internal Tristate Bus Enable/Disable, I/O Cell Buffer	–	2.2	–	2.5	–	3.8	ns
tbfmm	64	BFM Routing Delay, Signal from Macrocell	–	1.9	–	2.3	–	3.4	ns
tgrpm	65	GRP Delay, Signal from Macrocell	–	2	–	2.4	–	3.5	ns
tgrpmz	66	Internal Tristate Bus Enable/Disable, Macrocell Buffer	–	4	–	4.7	–	7.1	ns
tbfmg	67	BFM Routing Delay, Signal from GRP	–	1.6	–	1.8	–	2.8	ns
tgrpb	68	GRP Delay, Signal from BFM Routing	–	2.5	–	3.0	–	4.4	ns
tbcom	69	BFM Routing to I/O Cell, Combinatorial Path	–	0.5	–	0.6	–	0.8	ns
tbreg	70	BFM Routing to I/O Cell, Registered Path	–	3.5	–	4.1	–	6.1	ns
tgcom	71	GRP to I/O Cell, Combinatorial Path	–	0.4	–	0.4	–	0.6	ns
tgreg	72	GRP to I/O Cell, Registered Path	–	3.4	–	3.9	–	5.9	ns
I/O Control Bus Delay									
tpiock	73	Product Term as I/O Cell Register Clock	–	6.5	–	7.7	–	11.6	ns
tpiocken	74	Product Term as I/O Cell Register Clock Enable	–	6.5	–	7.7	–	11.6	ns
tpoe	75	Product Term as Output Buffer Enable/Disable	–	6.7	–	7.9	–	11.9	ns
tpiorst	76	Product Term as I/O Cell Register Reset or Set Delay	–	7.3	–	8.8	–	13.2	ns
tpioz	77	Internal Tristate Bus Control Signal for I/O Cell Buffer	–	6.0	–	7.1	–	10.7	ns
Global Control Delay									
tgck	78	Global Macrocell Register Clk	2.9	3.7	3.1	4.9	4.6	7.3	ns
tgcken	79	Global Macrocell Register Clk Enable	4.7	4.7	5.8	5.8	8.7	8.7	ns
tgiock	80	Global I/O Register Clk	3.9	3.9	4.1	5.0	6.2	7.0	ns
tgiocken	81	Global I/O Register Clk Enable	4.8	4.8	5.9	5.9	8.9	8.9	ns
tqck	82	Quadrant I/O Register Clk	2.4	2.4	2.1	3.5	3.2	5.1	ns
tgoe	83	Global Output Enable	–	6	–	7.7	–	11.5	ns
ttoe	84	Test Output Enable	–	7.3	–	8.6	–	12.9	ns
tgmrst	85	Global GLB Register Reset	–	4	–	5.1	–	7.6	ns
tgiorst	86	Global I/O Cell Register Reset	–	4.6	–	5.9	–	8.8	ns

1. Internal Timing Parameters are not tested and are for reference only.
2. Refer to Timing Model in this data sheet for further details.

ispLSI 8840 Timing Model



Example Timing Calculations

tpd1 = (BFM Input Path Delay) + (GLB Delay) + (Output Path Delay)
= (**t**idcom + **t**ibp + **t**bfmi) + (**t**andhs + **t**4ptcom + **t**mbp) + (**t**bfmm + **t**bcom + **t**obp + **t**odcom + **t**slf)
= (#23 + #26 + #61) + (#39 + #42 + #45) + (#64 + #69 + #25 + #35 + #37)
= (0.1 + 0.2 + 0.2) + (3.6 + 0.2 + 0.0) + (1.9 + 0.5 + 0.0 + 1.7 + 0.0)
= 8.4 ns

tpd (within BFM)
= (BFM Delay) + (GLB Delay)
= (**t**bfmm) + (**t**andhs + **t**4ptcom + **t**mbp)
= (#64) + (#39 + #42 + #45)
= (1.9) + (3.6 + 0.2 + 0.0)
= 5.7 ns

tpd (between BFMs)
= (GRP Delay) + (BFM Delay) + (GLB Delay)
= (**t**grpm) + (**t**bfmg) + (**t**andhs + **t**4ptcom + **t**mbp)
= (#65) + (#67) + (#39 + #42 + #45)
= (2.0) + (1.6) + (3.6 + 0.2 + 0.0)
= 7.4 ns

BFM I/O to internal tri-state Enable/Disable
= (BFM Input Path Delay) + (GLB Delay, 1PT) + (Tri-state Control Delay)
= (**t**idcom + **t**ibp + **t**bfmi) + (**t**andhs + **t**1pt + **t**mbp) + (**t**grpmz)
= (#23 + #26 + #61) + (#39 + #41 + #45) + (#66)
= (0.1 + 0.2 + 0.2) + (3.6 + 3.6 + 0.0) + (4.0)
= 11.7 ns

tsu1 = (BFM Input Path Delay) + (GLB Setup Time) - (Min. Global Clock Delay)
= (**t**idcom + **t**ibp + **t**bfmi) + (**t**andhs + **t**4ptreg + **t**msu) – (**t**gck min)
= (#23 + #26 + #61) + (#39 + #43 + #48) – (#78)
= (0.1 + 0.2 + 0.2) + (3.6 + 3.4 + 0.4) – (2.9)
= 5 ns

1/**F**max = (Global Clk to MC Output) + (Local Feedback) + (GLB Setup Time)
= (**t**mco) + (**t**floc) + (**t**andhs + **t**ptsa + **t**msu)
= (#47) + (#54) + (#39 + #44 + #48)
= (0.2) + (1.1) + (3.6 + 3.7 + 0.4)
= 9 ns

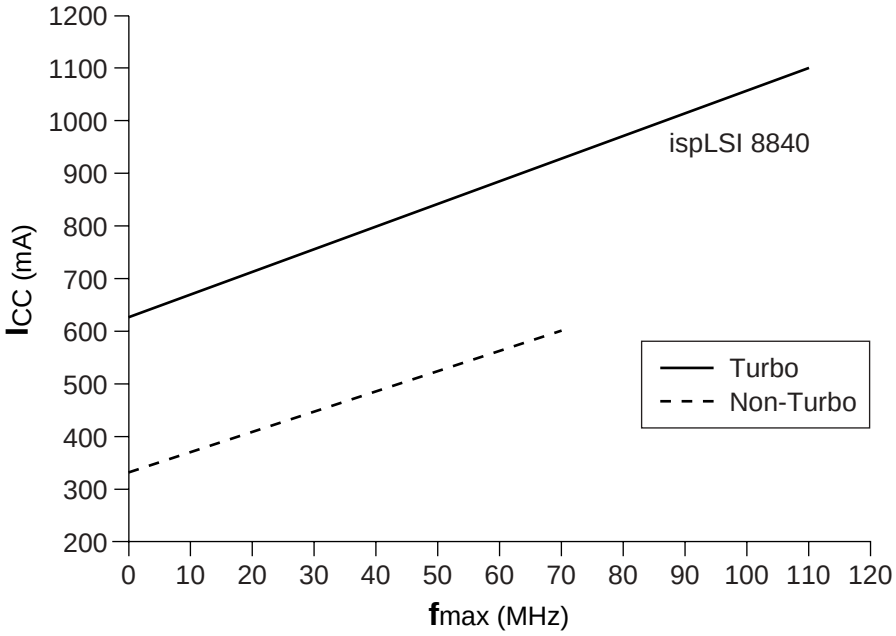
Fmax = 111 MHz

Note: Calculations are based upon timing specifications for the ispLSI 8840-110L

Power Consumption

Power consumption in the ispLSI 8840 device depends on two primary factors: the speed at which the device is operating and the number of product terms used. The product terms have a fuse-selectable speed/power tradeoff setting. Each group of four product terms has a single speed/power tradeoff control fuse that acts on the complete group of four. The fast "high-speed" setting operates product terms at their normal full power consumption. For portions of the logic that can tolerate longer propagation delays, selecting the slower "low-power" setting will significantly reduce the power dissipation for these product terms. Figure 10 shows the relationship between power and operating speed.

Figure 10. Typical Device Power Consumption vs fmax



Notes: Configuration of 42 20-bit counters
Typical current at 5V, 25° C

I_{CC} can be estimated for the ispLSI 8840 using the following equation:

I_{CC} = 48.0 + (# of Turbo PTs * 0.346) + (# of Non-Turbo PTs * 0.165) + (# of Macrocells Used * fmax * AF * 0.049)
# of Turbo PTs = Number of Turbo Product Terms Used in Design
# of Non-Turbo PTs = Number of Non-Turbo Product Terms Used in Design
fmax = Maximum Operating Frequency

$$\text{AF (Activity Factor)} = \frac{\text{Average Macrocell Toggle Frequency}}{\text{Fmax}}$$

Note: An Activity Factor of 1.0 means all macrocell registers toggle at Fmax. An Activity Factor of 0.5 means the average macrocell registers toggle at half of fmax.

The I_{CC} estimate is based on typical conditions (V_{CC} = 5.0V, room temperature) and an assumption of two GLB loads on average exists. These values are for estimates only. Since the value of I_{CC} is sensitive to operating conditions and the program in the device, the actual I_{CC} should be verified.

0127/8840

Signal Descriptions

Signal Name	Description
CLK0, CLK1, CLK2	Dedicated clock input for the GLB registers only. These clock inputs are connected to one of the clock inputs of all GLB registers in the device.
CLKEN	Dedicated clock enable input for the GLB registers only. This input is available as a clock enable for each GLB register in the device. Use of the clock enable input eliminates the need for the user to gate the clock to the register.
GIOCLK0, GIOCLK1	Dedicated clock inputs for the I/O registers only. These clock inputs are connected to one of the clock inputs of all I/O registers in the device.
GND	Ground (GND)
GOE	Global Output Enable inputs.
SET/RESET	Dedicated reset/preset pin connected to ALL registers in the device, GLB registers and I/O registers. Each register can independently choose to be reset or preset when this signal goes active. The active polarity is user-selectable.
IOCLKEN	Dedicated clock enable input for the I/O registers only. This input is available as a clock enable input for all I/O registers in the device. Use of the clock enable input eliminates the need for the user to tie the clock to the I/O register.
I/O	Input/Output – These are the general purpose I/O used by the logic array.
BSCAN/$\overline{\text{ispEN}}$	Input – Dedicated in-system programming enable input. When this is high, the BSCAN TAP controller signals TMS, TDI, TDO and TCK are enabled. When this is brought low, the ISP State Machine control signals MODE, SDI, SDO and SLCK are enabled. High-to-low transition will put the device in the Lattice ISP programming mode and put all I/O in the high-Z state.
TMS/MODE	Input – This signal performs two functions. It is the Test Mode Select input signal when $\overline{\text{ispEN}}$ is logic high. When $\overline{\text{ispEN}}$ is logic low, it controls the operation of the ISP State Machine.
NC[1]	No connect.
QIOCLK0 QIOCLK1 QIOCLK2 QIOCLK3	Dedicated clock inputs for the I/O registers only. These clock inputs are connected to the I/O registers on the same side of the device only, they are not connected to all of the I/O registers. Use of these quadrant I/O clocks gives the fastest tco from the device.
TCK/SCLK	Input – This signal performs two functions. It is the Test Clock input signal when $\overline{\text{ispEN}}$ is logic high. When $\overline{\text{ispEN}}$ is logic low, it functions as a clock signal for the Serial Shift Register.
TDI/SDI	Input – This signal performs two functions. It is the Test Data input signal when $\overline{\text{ispEN}}$ is logic high. When $\overline{\text{ispEN}}$ is logic low, it functions as an input to load programming data into the device. SDI is also used as one of the two control signals for the ISP State Machine.
TDO/SDO	Output – This signal performs two functions. When $\overline{\text{ispEN}}$ is logic low, it reads the ISP data. When $\overline{\text{ispEN}}$ is high, it functions as Test Data Out.
TOE	Test Output Enable pin – This pin tristates all I/O pins when a logic low is driven.
VCC	Vcc
VCCIO	Power supply for the output drivers. The internal logic of the device is connected to VCC which is always 5V. The output drivers are connected to VCCIO which can be equal to VCC or 3.3V. This allows the output drivers to be powered from 3.3V, for example, to interface directly with another 3.3V device.

1. NC pins are not to be connected to any active signals, VCC or GND.

Signal Locations (432-Ball BGA Package)

Signal	432-Ball BGA
CLK0, CLK1, CLK2	A18, P29, AL19
CLKEN	C18
GIOCLK0, GIOCLK1	A19, AJ18
GND	A1, A2, A16, A30, A31, B1, B5, B9, B13, B19, B23, B27, B31, E2, E30, J2, J30, N2, N30, T1, T31, W2, W30, AC2, AC30, AG2, AG30, AK1, AK5, AK9, AK13, AK19, AK23, AK27, AK31, AL1, AL2, AL16, AL30, AL31
GOE0, GOE1 GOE2, GOE3	D18, T29, AH18, T2
SET/RESET	P1
IOCLKEN	AL20
BSCAN/$\overline{\text{ispEN}}$	AG28
TMS/MODE	E4
NC[1]	A4, B30, D1, D31, AH1, AH31, AK2, AK30, AL4, AL28
QIOCLK0, QIOCLK1, QIOCLK2, QIOCKK3	D17, R31, AL18, T3
TCK/SCLK	AH2
TDI/SDI	E3
TDO/SDO	AH3
TOE	V3
VCC	A3, A10, A22, A29, B14, B18, C1, C31, K1, K31, P2, P30, V2, V30, AB1, AB31, AJ1, AJ31, AK14, AK18, AL3, AL10, AL22, AL29
VCCIO	D5, D9, D12, D15, D20, D23, D27, H4, H28, M4, M28, T4, T28, Y4, Y28, AE4, AE28, AH5, AH9, AH12, AH15, AH20, AH23, AH27

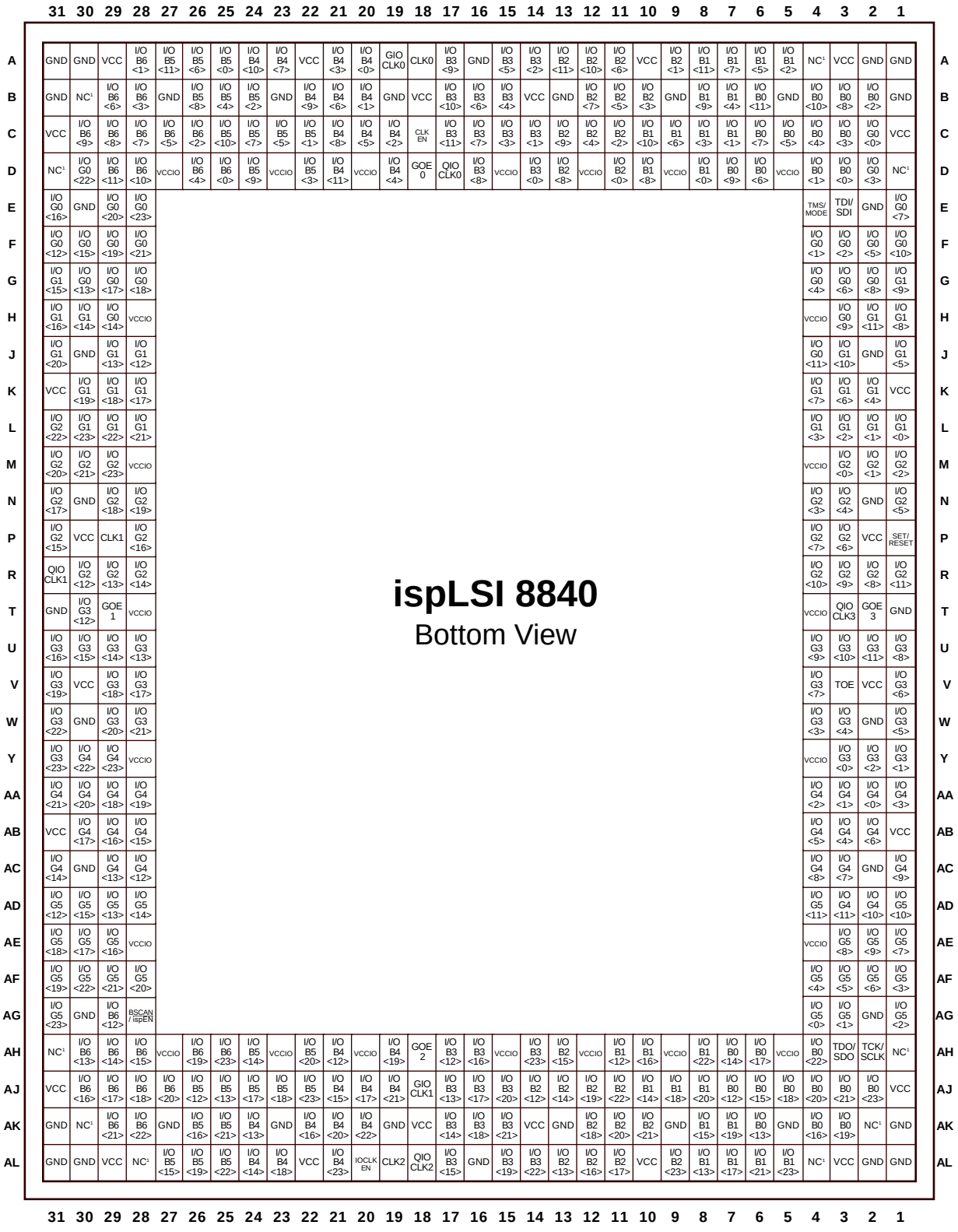
1. NC pins are not to be connected to any active signals, VCC or GND.

I/O Pin Locations (432-Ball BGA Package)

Signal	BGA	Signal	BGA	Signal	BGA	Signal	BGA	Signal	BGA
I/O G0 <0>	C2	I/O G2 <15>	P31	I/O G5 <6>	AF2	I/O B1 <21>	AL6	I/O B4 <12>	AH21
I/O G0 <1>	F4	I/O G2 <16>	P28	I/O G5 <7>	AE1	I/O B1 <22>	AH8	I/O B4 <13>	AK24
I/O G0 <2>	F3	I/O G2 <17>	N31	I/O G5 <8>	AE3	I/O B1 <23>	AL5	I/O B4 <14>	AL24
I/O G0 <3>	D2	I/O G2 <18>	N29	I/O G5 <9>	AE2	I/O B2 <0>	D11	I/O B4 <15>	AJ21
I/O G0 <4>	G4	I/O G2 <19>	N28	I/O G5 <10>	AD1	I/O B2 <1>	A9	I/O B4 <16>	AK22
I/O G0 <5>	F2	I/O G2 <20>	M31	I/O G5 <11>	AD4	I/O B2 <2>	C11	I/O B4 <17>	AJ20
I/O G0 <6>	G3	I/O G2 <21>	M30	I/O G5 <12>	AD31	I/O B2 <3>	B10	I/O B4 <18>	AL23
I/O G0 <7>	E1	I/O G2 <22>	L31	I/O G5 <13>	AD29	I/O B2 <4>	C12	I/O B4 <19>	AH19
I/O G0 <8>	G2	I/O G2 <23>	M29	I/O G5 <14>	AD28	I/O B2 <5>	B11	I/O B4 <20>	AK21
I/O G0 <9>	H3	I/O G3 <0>	Y3	I/O G5 <15>	AD30	I/O B2 <6>	A11	I/O B4 <21>	AJ19
I/O G0 <10>	F1	I/O G3 <1>	Y1	I/O G5 <16>	AE29	I/O B2 <7>	B12	I/O B4 <22>	AK20
I/O G0 <11>	J4	I/O G3 <2>	Y2	I/O G5 <17>	AE30	I/O B2 <8>	D13	I/O B4 <23>	AL21
I/O G0 <12>	F31	I/O G3 <3>	W4	I/O G5 <18>	AE31	I/O B2 <9>	C13	I/O B5 <0>	A25
I/O G0 <13>	G30	I/O G3 <4>	W3	I/O G5 <19>	AF31	I/O B2 <10>	A12	I/O B5 <1>	C22
I/O G0 <14>	H29	I/O G3 <5>	W1	I/O G5 <20>	AF28	I/O B2 <11>	A13	I/O B5 <2>	B24
I/O G0 <15>	F30	I/O G3 <6>	V1	I/O G5 <21>	AF29	I/O B2 <12>	AJ14	I/O B5 <3>	D22
I/O G0 <16>	E31	I/O G3 <7>	V4	I/O G5 <22>	AF30	I/O B2 <13>	AL13	I/O B5 <4>	B25
I/O G0 <17>	G29	I/O G3 <8>	U1	I/O G5 <23>	AG31	I/O B2 <14>	AJ13	I/O B5 <5>	C23
I/O G0 <18>	G28	I/O G3 <9>	U4	I/O B0 <0>	D3	I/O B2 <15>	AH13	I/O B5 <6>	A26
I/O G0 <19>	F29	I/O G3 <10>	U3	I/O B0 <1>	D4	I/O B2 <16>	AL12	I/O B5 <7>	C24
I/O G0 <20>	E29	I/O G3 <11>	U2	I/O B0 <2>	B2	I/O B2 <17>	AL11	I/O B5 <8>	B26
I/O G0 <21>	F28	I/O G3 <12>	T30	I/O B0 <3>	C3	I/O B2 <18>	AK12	I/O B5 <9>	D24
I/O G0 <22>	D30	I/O G3 <13>	U28	I/O B0 <4>	C4	I/O B2 <19>	AJ12	I/O B5 <10>	C25
I/O G0 <23>	E28	I/O G3 <14>	U29	I/O B0 <5>	C5	I/O B2 <20>	AK11	I/O B5 <11>	A27
I/O G1 <0>	L1	I/O G3 <15>	U30	I/O B0 <6>	D6	I/O B2 <21>	AK10	I/O B5 <12>	AJ26
I/O G1 <1>	L2	I/O G3 <16>	U31	I/O B0 <7>	C6	I/O B2 <22>	AJ11	IO B5 <13>	AJ25
I/O G1 <2>	L3	I/O G3 <17>	V28	I/O B0 <8>	B3	I/O B2 <23>	AL9	I/O B5 <14>	AH24
I/O G1 <3>	L4	I/O G3 <18>	V29	I/O B0 <9>	D7	I/O B3 <0>	D14	I/O B5 <15>	AL27
I/O G1 <4>	K2	I/O G3 <19>	V31	I/O B0 <10>	B4	I/O B3 <1>	C14	I/O B5 <16>	AK26
I/O G1 <5>	J1	I/O G3 <20>	W29	I/O B0 <11>	B6	I/O B3 <2>	A14	I/O B5 <17>	AJ24
I/O G1 <6>	K3	I/O G3 <21>	W28	I/O B0 <12>	AJ7	I/O B3 <3>	C15	I/O B5 <18>	AJ23
I/O G1 <7>	K4	I/O G3 <22>	W31	I/O B0 <13>	AK6	I/O B3 <4>	B15	I/O B5 <19>	AL26
I/O G1 <8>	H1	I/O G3 <23>	Y31	I/O B0 <14>	AH7	I/O B3 <5>	A15	I/O B5 <20>	AH22
I/O G1 <9>	G1	I/O G4 <0>	AA2	I/O B0 <15>	AJ6	I/O B3 <6>	B16	I/O B5 <21>	AK25
I/O G1 <10>	J3	I/O G4 <1>	AA3	I/O B0 <16>	AK4	I/O B3 <7>	C16	I/O B5 <22>	AL25
I/O G1 <11>	H2	I/O G4 <2>	AA4	I/O B0 <17>	AH6	I/O B3 <8>	D16	I/O B5 <23>	AJ22
I/O G1 <12>	J28	I/O G4 <3>	AA1	I/O B0 <18>	AJ5	I/O B3 <9>	A17	I/O B6 <0>	D25
I/O G1 <13>	J29	I/O G4 <4>	AB3	I/O B0 <19>	AK3	I/O B3 <10>	B17	I/O B6 <1>	A28
I/O G1 <14>	H30	I/O G4 <5>	AB4	I/O B0 <20>	AJ4	I/O B3 <11>	C17	I/O B6 <2>	C26
I/O G1 <15>	G31	I/O G4 <6>	AB2	I/O B0 <21>	AJ3	I/O B3 <12>	AH17	I/O B6 <3>	B28
I/O G1 <16>	H31	I/O G4 <7>	AC3	I/O B0 <22>	AH4	I/O B3 <13>	AJ17	I/O B6 <4>	D26
I/O G1 <17>	K28	I/O G4 <8>	AC4	I/O B0 <23>	AJ2	I/O B3 <14>	AK17	I/O B6 <5>	C27
I/O G1 <18>	K29	I/O G4 <9>	AC1	I/O B1 <0>	D8	I/O B3 <15>	AL17	I/O B6 <6>	B29
I/O G1 <19>	K30	I/O G4 <10>	AD2	I/O B1 <1>	C7	I/O B3 <16>	AH16	I/O B6 <7>	C28
I/O G1 <20>	J31	I/O G4 <11>	AD3	I/O B1 <2>	A5	I/O B3 <17>	AJ16	I/O B6 <8>	C29
I/O G1 <21>	L28	I/O G4 <12>	AC28	I/O B1 <3>	C8	I/O B3 <18>	AK16	I/O B6 <9>	C30
I/O G1 <22>	L29	I/O G4 <13>	AC29	I/O B1 <4>	B7	I/O B3 <19>	AL15	I/O B6 <10>	D28
I/O G1 <23>	L30	I/O G4 <14>	AC31	I/O B1 <5>	A6	I/O B3 <20>	AJ15	I/O B6 <11>	D29
I/O G2 <0>	M3	I/O G4 <15>	AB28	I/O B1 <6>	C9	I/O B3 <21>	AK15	I/O B6 <12>	AG29
I/O G2 <1>	M2	I/O G4 <16>	AB29	I/O B1 <7>	A7	I/O B3 <22>	AL14	I/O B6 <13>	AH30
I/O G2 <2>	M1	I/O G4 <17>	AB30	I/O B1 <8>	D10	I/O B3 <23>	AH14	I/O B6 <14>	AH29
I/O G2 <3>	N4	I/O G4 <18>	AA29	I/O B1 <9>	B8	I/O B4 <0>	A20	I/O B6 <15>	AH28
I/O G2 <4>	N3	I/O G4 <19>	AA28	I/O B1 <10>	C10	I/O B4 <1>	B20	I/O B6 <16>	AJ30
I/O G2 <5>	N1	I/O G4 <20>	AA30	I/O B1 <11>	A8	I/O B4 <2>	C19	I/O B6 <17>	AJ29
I/O G2 <6>	P3	I/O G4 <21>	AA31	I/O B1 <12>	AH11	I/O B4 <3>	A21	I/O B6 <18>	AJ28
I/O G2 <7>	P4	I/O G4 <22>	Y30	I/O B1 <13>	AL8	I/O B4 <4>	D19	I/O B6 <19>	AH26
I/O G2 <8>	R2	I/O G4 <23>	Y29	I/O B1 <14>	AJ10	I/O B4 <5>	C20	I/O B6 <20>	AJ27
I/O G2 <9>	R3	I/O G5 <0>	AG4	I/O B1 <15>	AK8	I/O B4 <6>	B21	I/O B6 <21>	AK29
I/O G2 <10>	R4	I/O G5 <1>	AG3	I/O B1 <16>	AH10	I/O B4 <7>	A23	I/O B6 <22>	AK28
I/O G2 <11>	R1	I/O G5 <2>	AG1	I/O B1 <17>	AL7	I/O B4 <8>	C21	I/O B6 <23>	AH25
I/O G2 <12>	R30	I/O G5 <3>	AF1	I/O B1 <18>	AJ9	I/O B4 <9>	B22		
I/O G2 <13>	R29	I/O G5 <4>	AF4	I/O B1 <19>	AK7	I/O B4 <10>	A24		
I/O G2 <14>	R28	I/O G5 <5>	AF3	I/O B1 <20>	AJ8	I/O B4 <11>	D21		

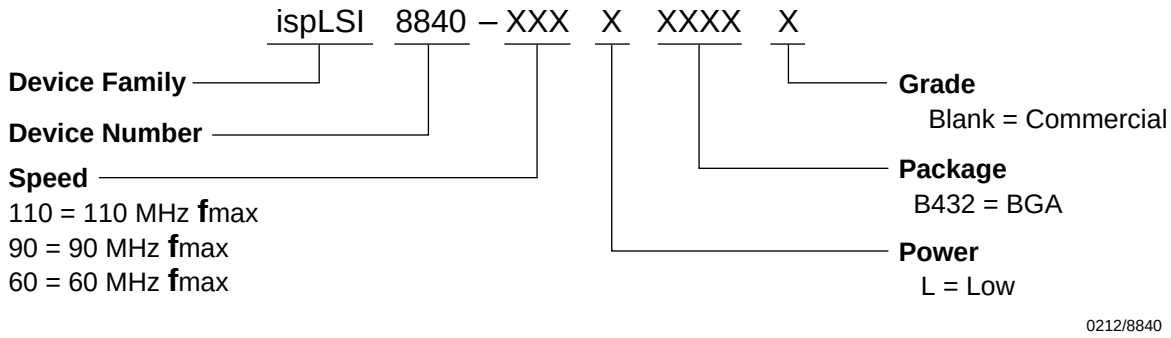
Signal Configuration

ispLSI 8840 432-Ball BGA Signal Diagram



1. NC pins are not to be connected to any active signals, VCC or GND.

Part Number Description



0212/8840

Ordering Information

COMMERCIAL

FAMILY	fmax (MHz)	tpd (ns)	ORDERING NUMBER	PACKAGE
ispLSI	110	8.5	ispLSI 8840-110LB432	432-Ball BGA
	90	10	ispLSI 8840-90LB432	432-Ball BGA
	60	15	ispLSI 8840-60LB432	432-Ball BGA

Table 2-0041/8840

Mouser Electronics

Authorized Distributor

Click to View Pricing, Inventory, Delivery & Lifecycle Information:

Lattice:

ISPLSI8840-90LB432 ISPLSI8840-110LB432 ISPLSI8840-60LB432