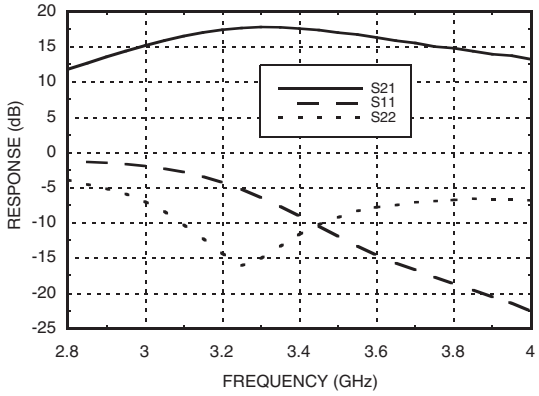
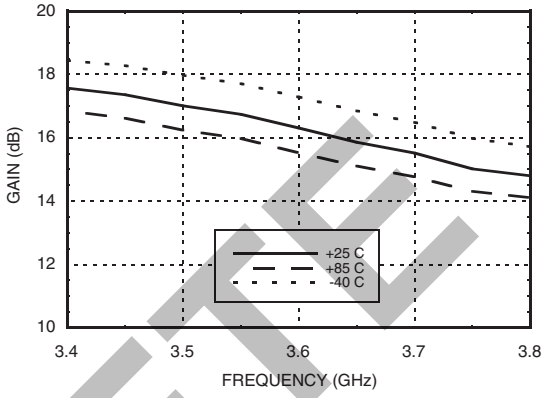
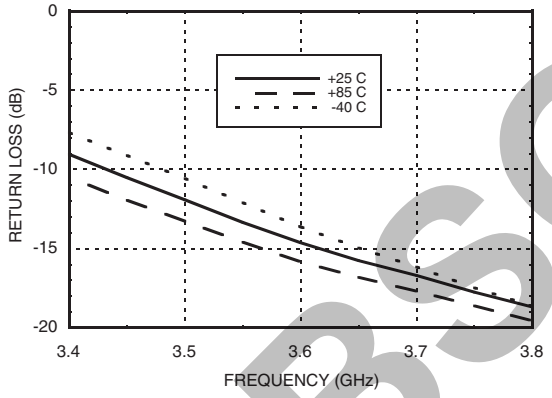
### LNA Mode
### Broadband Gain & Return Loss



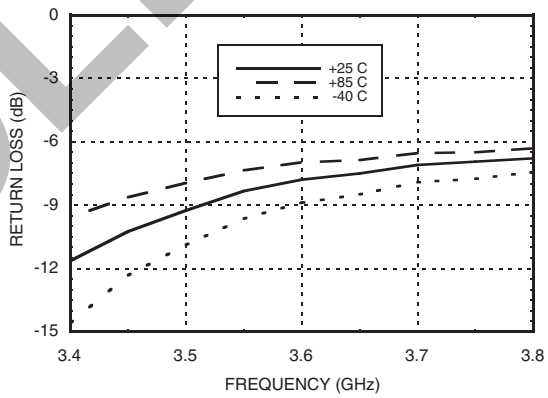

### LNA Mode
### Gain vs. Temperature



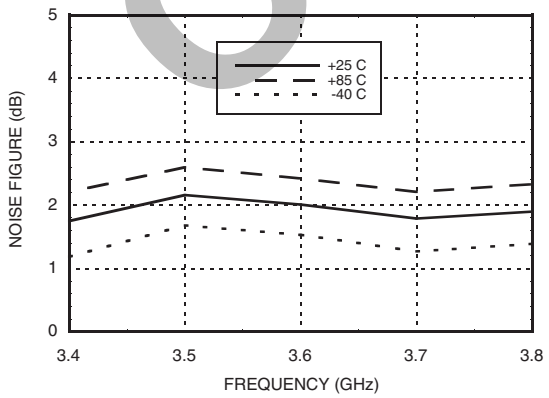

### LNA Mode
### Input Return Loss vs. Temperature



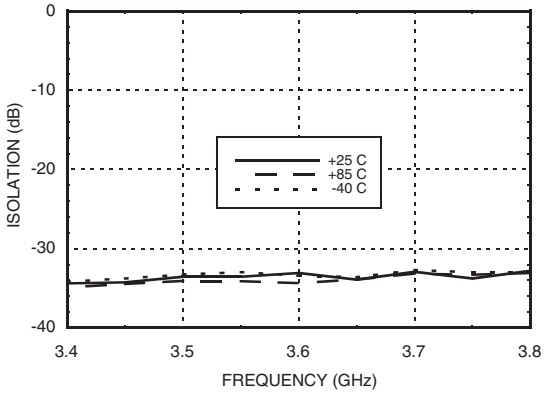

### LNA Mode
### Output Return Loss vs. Temperature




### LNA Mode
### Noise Figure vs. Temperature




### LNA Mode
### Reverse Isolation vs. Temperature



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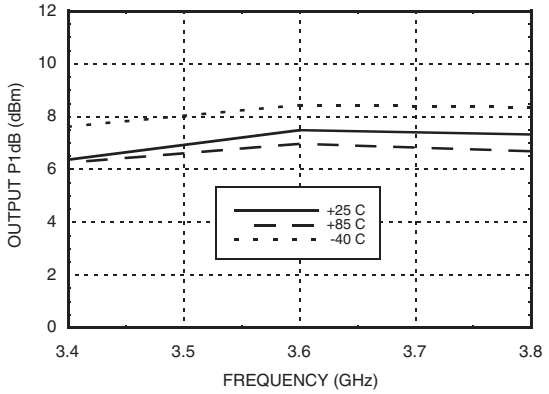
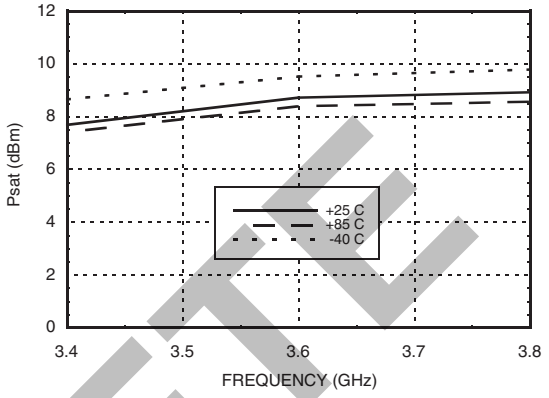
## GaAs MMIC LOW NOISE AMPLIFIER w/ BYPASS MODE, 3.4 - 3.8 GHz

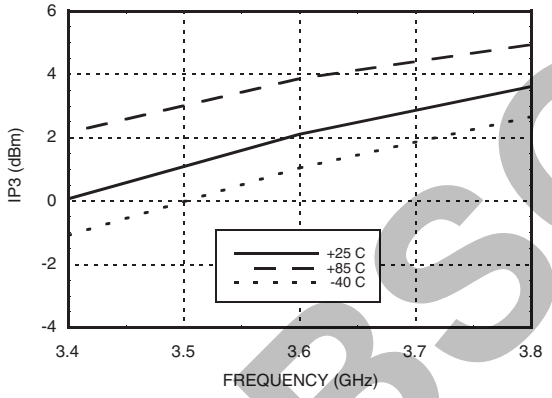
### LNA Mode
### Output P1dB vs. Temperature



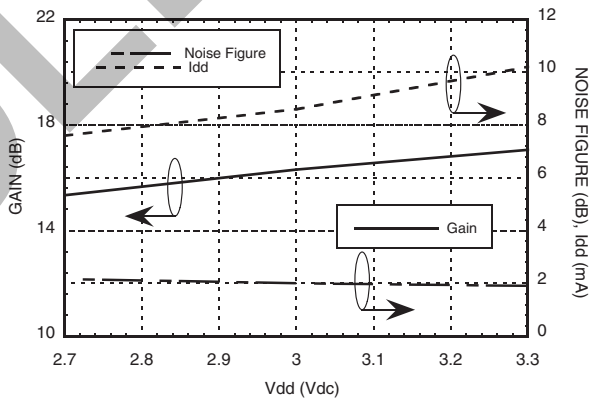

### LNA Mode
### Psat vs. Temperature



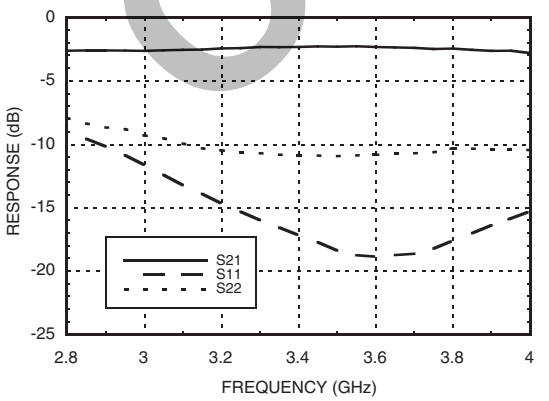

### LNA Mode
### Input IP3 vs. Temperature



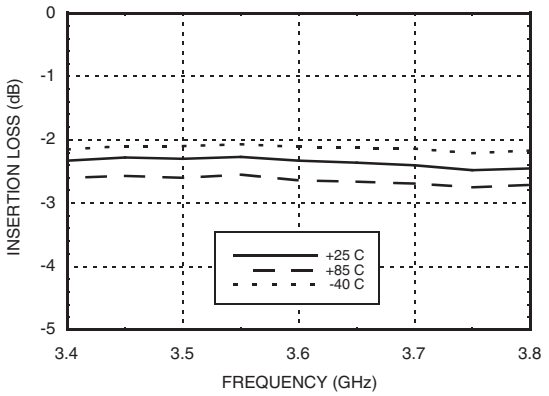

### LNA Mode Gain, Noise Figure & Supply Current vs. Supply Voltage @ 3.6 GHz




### Bypass Mode
### Broadband Insertion Loss & Return Loss




### Bypass Mode
### Insertion Loss vs. Temperature





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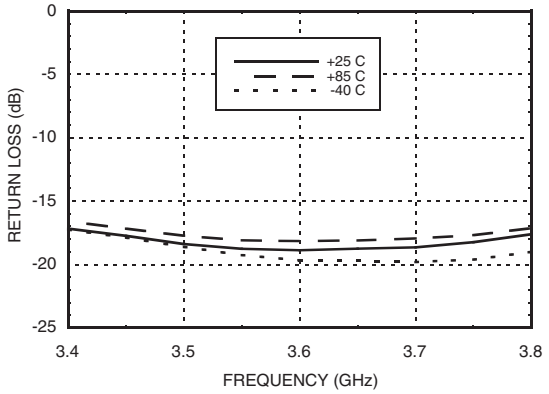
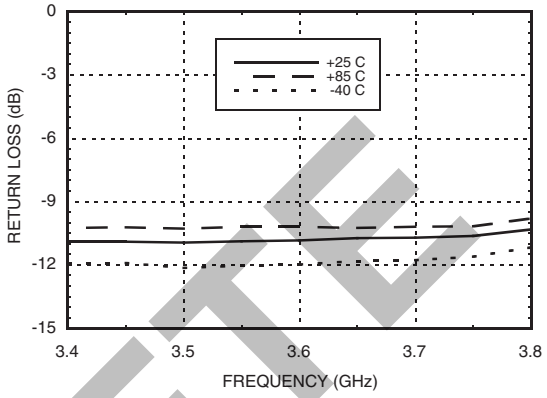
# GaAs MMIC LOW NOISE AMPLIFIER w/ BYPASS MODE, 3.4 - 3.8 GHz



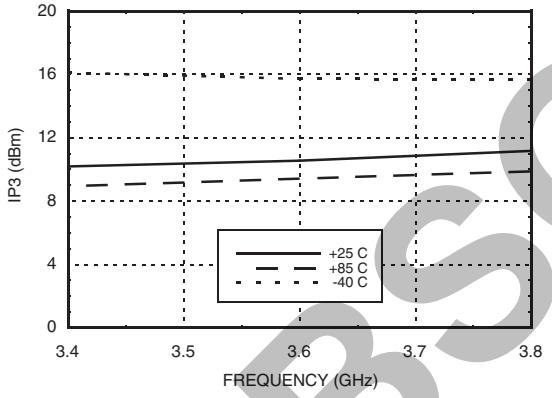
### Bypass Mode
### Input Return Loss vs. Temperature



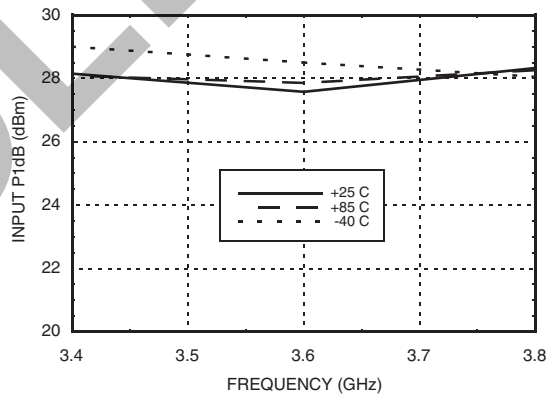

### Bypass Mode
### Output Return Loss vs. Temperature




### Bypass Mode
### Input IP3 vs. Temperature




### Bypass Mode
### Input P1dB vs. Temperature






## Absolute Maximum Ratings

| | |
|---|---|
| Drain Bias Voltage (Vdd) | +7.0 Vdc |
| RF Input Power (RFIN) LNA Mode<br>(Vdd = +3.0 Vdc) Bypass Mode | 0 dBm<br>+30 dBm |
| Channel Temperature | 150 °C |
| Continuous Pdiss (T = 85 °C)<br>(derate 1.8 mW/°C above 85 °C) | 0.117 W |
| Thermal Resistance<br>(channel to ground paddle) | 556 °C/W |
| Storage Temperature | -65 to +150 °C |
| Operating Temperature | -40 to +85 °C |

ELECTROSTATIC SENSITIVE DEVICE
OBSERVE HANDLING PRECAUTIONS

## Typical Supply Current vs. Vdd

| Vdd (Vdc) | Idd (mA) |
|---|---|
| +2.7 | 7.6 |
| +3.0 | 9.0 |
| +3.3 | 10.2 |

## Truth Table

| | |
|---|---|
| LNA Mode | Vctl= Vdd @ 1.6 mA |
| Bypass Mode | Vctl= 0Vdc @ -13 µA |
| Vdd= +3V ±10% | |



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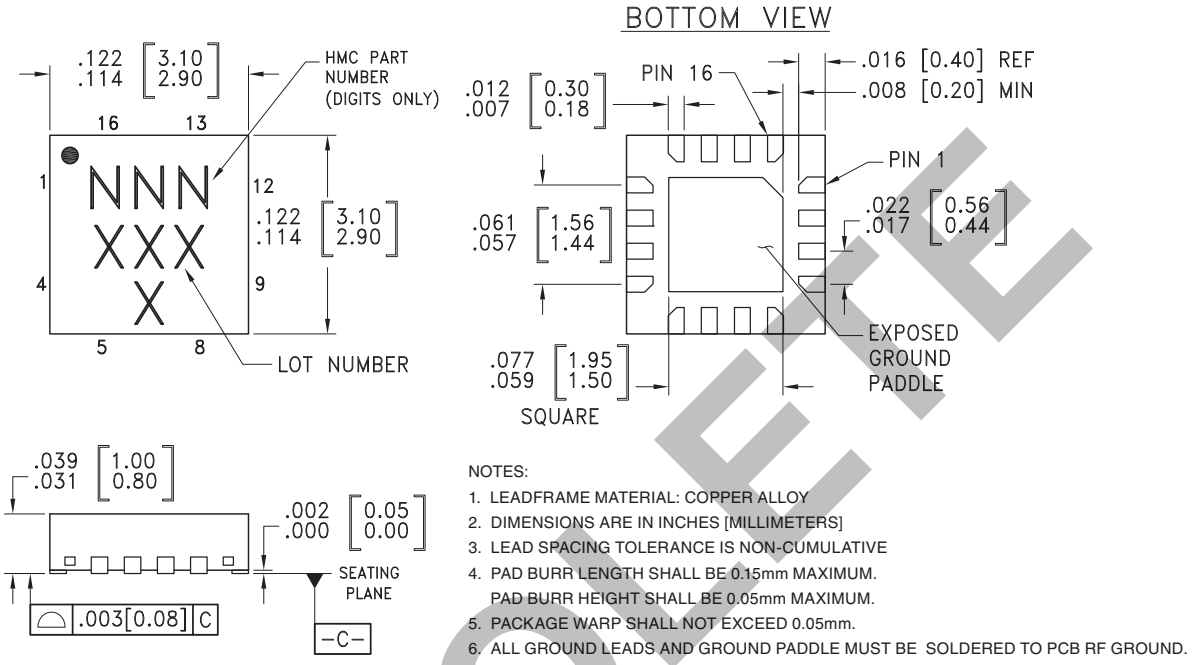
# HMC491LP3 / 491LP3E

v03.1206

## GaAs MMIC LOW NOISE AMPLIFIER w/ BYPASS MODE, 3.4 - 3.8 GHz

### Outline Drawing




NOTES:

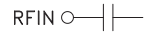
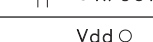
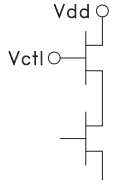
1. LEADFRAME MATERIAL: COPPER ALLOY
2. DIMENSIONS ARE IN INCHES [MILLIMETERS]
3. LEAD SPACING TOLERANCE IS NON-CUMULATIVE
4. PAD BURR LENGTH SHALL BE 0.15mm MAXIMUM. PAD BURR HEIGHT SHALL BE 0.05mm MAXIMUM.
5. PACKAGE WARP SHALL NOT EXCEED 0.05mm.
6. ALL GROUND LEADS AND GROUND PADDLE MUST BE SOLDERED TO PCB RF GROUND.
7. REFER TO HITTITE APPLICATION NOTE FOR SUGGESTED LAND PATTERN.

### Package Information

| Part Number | Package Body Material | Lead Finish | MSL Rating | Package Marking [3] |
|---|---|---|---|---|
| HMC491LP3 | Low Stress Injection Molded Plastic | Sn/Pb Solder | MSL1 [1] | 491<br>XXXX |
| HMC491LP3E | RoHS-compliant Low Stress Injection Molded Plastic | 100% matte Sn | MSL1 [2] | 491<br>XXXX |

[1] Max peak reflow temperature of 235 °C
[2] Max peak reflow temperature of 260 °C
[3] 4-Digit lot number XXXX

### Pin Descriptions

| Pin Number | Function | Description | Interface Schematic |
|---|---|---|---|
| 1, 5 - 8, 12, 13 | N/C | No connection necessary.<br>These pins may be connected to RF/DC ground. | |
| 2, 4, 9, 11, 15 | GND | These pins must be connected to RF/DC ground. |   |
| 3 | RF IN | This pin is AC coupled and matched to 50 Ohms. |   |
| 10 | RF OUT | This pin is AC coupled and matched to 50 Ohms. |   |
| 14 | Vdd | Power supply voltage. |   |
| 16 | Vctl | Control voltage. Vctl= Vdd for LNA mode.<br>Vctl= 0V for bypass mode. | |





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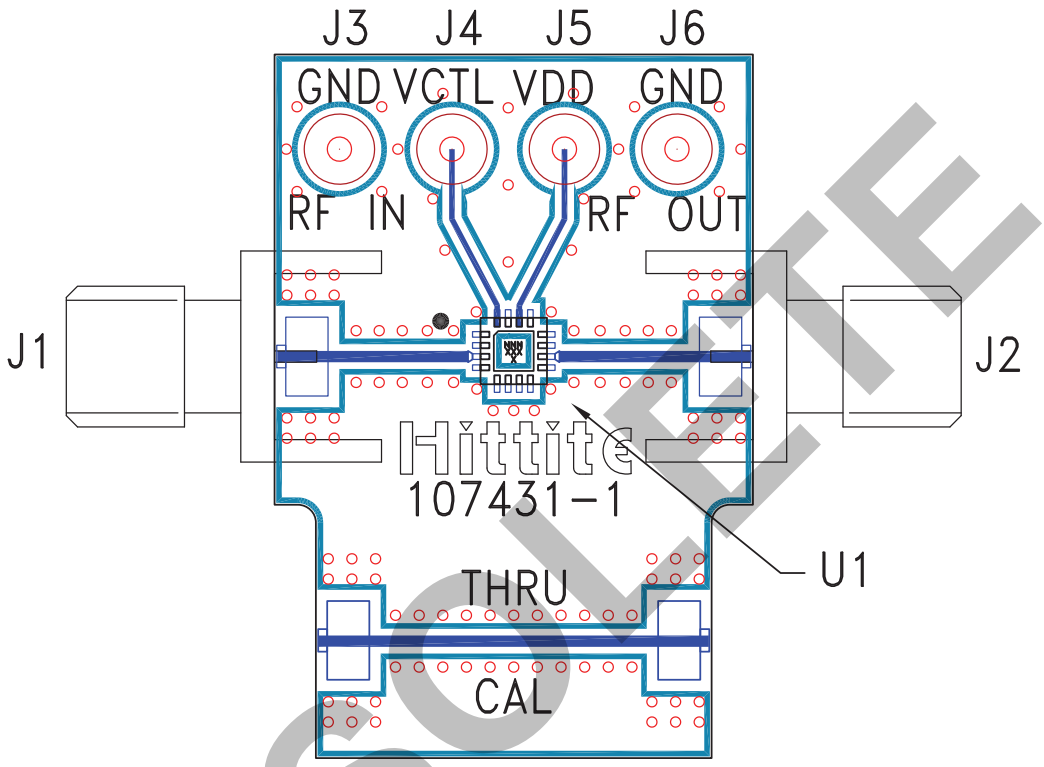
## Evaluation PCB






## List of Materials for Evaluation PCB 107174 [1]

| Item | Description |
|---|---|
| J1 - J2 | PCB Mount SMA RF Connector |
| J3 - J6 | DC Pin |
| U1 | HMC491LP3 / HMC491LP3E Amplifier |
| PCB [2] | 107431 Evaluation PCB |

[1] Reference this number when ordering complete evaluation PCB

[2] Circuit Board Material: Rogers 4350

The circuit board used in the final application should use RF circuit design techniques. Signal lines should have 50 ohm impedance while the package ground leads and exposed paddle should be connected directly to the ground plane similar to that shown. A sufficient number of via holes should be used to connect the top and bottom ground planes. The evaluation circuit board shown is available from Hittite upon request.



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