

2.4GHz to 2.5GHz 802.11g/b RF Transceivers with Integrated PA

ABSOLUTE MAXIMUM RATINGS

V_{CCTXPA}, V_{CCPA} and TXRF₋ to GND-0.3V to +4.5V
 V_{CC}LN_A, V_{CC}TXMX, V_{CC}PLL, V_{CC}CP, V_{CC}X_{TAL}, V_{CC}V_{CO},
 V_{CC}R_{XVGA}, V_{CC}R_{XFL}, and V_{CC}R_{XM}₋ to GND.....-0.3V to +3.9V
 B6, B7, B3, B2, SHDN, B5, CS, SCLK, DIN, B1, TUNE, B4,
 TXBBI₋, TXBBQ₋, RXHP, RXTX, RXBBI₋, RXBBQ₋, RSSI,
 BYPASS, CPOUT, LD, CLOCKOUT, XTAL, CTUNE, RXRF₋ to
 GND-0.3V to (Operating V_{CC} + 0.3V)
 RXBBI₋, RXBBQ₋, RSSI, BYPASS, CPOUT, LD, CLOCKOUT
 Short-Circuit Duration 10s

RF Input Power+10dBm
 Continuous Power Dissipation (T_A = +70°C)
 48-Pin TQFN (derates 27.8mW/°C above +70°C)2.22W
 Operating Temperature Range-40°C to +85°C
 Junction Temperature+150°C
 Storage Temperature Range-65°C to +160°C
 Lead Temperature (soldering, 10s)+300°C
 Soldering Temperature (reflow)+260°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.



CAUTION! ESD SENSITIVE DEVICE

DC ELECTRICAL CHARACTERISTICS

(MAX2831 EV kit: V_{CC}₋ = 2.7V to 3.6V, V_{CCPA} = V_{CCTXPA} = 2.7V to 4.2V, T_A = -40°C to +85°C, Rx set to the maximum gain. CS = high, RXHP = SCLK = DIN = low, RSSI and clock output buffer are off, no signal at RF inputs, all RF inputs and outputs terminated into 50Ω, receiver baseband outputs are open. 100mV_{RMS} differential I and Q signals (54Mbps IEEE 802.11g OFDM) applied to I/Q baseband inputs of transmitter in transmit mode, f_{REF} = 40MHz, and registers set to recommended settings and corresponding test mode, unless otherwise noted. Typical values are at V_{CC} = 2.8V, V_{CCPA} = 3.3V, and T_A = +25°C, LO frequency = 2.437GHz, unless otherwise noted. RF inputs/outputs specifications are referenced to device pins and do not include 1dB loss from EV kit PCB, balun, and SMA connectors.) (Note 1)

PARAMETERS	CONDITIONS		MIN	TYP	MAX	UNITS
Supply Voltage	V _{CC} ₋		2.7		3.6	V
	V _{CCPA} , V _{CCTXPA}		2.7		4.2	
Supply Current	Shutdown mode, B7: B1 = 0000000, reference oscillator not applied	T _A = +25°C		20		μA
	Standby mode	T _A = +25°C		28	35	mA
		T _A = -40°C to +85°C			35	
	Rx mode	T _A = +25°C		62	78	
		T _A = -40°C to +85°C			82	
	Tx mode, T _A = +25°C, V _{CC} = 2.8V, V _{CCPA} = 3.3V, (Note 2)	MAX2831, transmit section		82	104	
		MAX2831, PA, P _{OUT} = +18.2dBm		209	258	
	MAX2832		86			
Rx calibration mode	T _A = +25°C		101			
Tx calibration mode	T _A = +25°C		78			
Rx I/Q Output Common-Mode Voltage	T _A = +25°C at default common-mode setting		0.98	1.2	1.33	V
Rx I/Q Output Common-Mode Voltage Variation	T _A = -40°C (relative to T _A = +25°C)			-17		mV
	T _A = +85°C (relative to T _A = +25°C)			15		
Tx Baseband Input Common- Mode Voltage Operating Range	DC-coupled		0.9		1.3	V
Tx Baseband Input Bias Current	Source current				22	μA

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DC ELECTRICAL CHARACTERISTICS (continued)

(MAX2831 EV kit: $V_{CC_} = 2.7V$ to $3.6V$, $V_{CCPA} = V_{CCTXPA} = 2.7V$ to $4.2V$, $T_A = -40^{\circ}C$ to $+85^{\circ}C$, Rx set to the maximum gain, $\overline{CS} =$ high, $RXHP = SCLK = DIN =$ low, RSSI and clock output buffer are off, no signal at RF inputs, all RF inputs and outputs terminated into 50Ω , receiver baseband outputs are open. $100mV_{RMS}$ differential I and Q signals (54Mbps IEEE 802.11g OFDM) applied to I/Q baseband inputs of transmitter in transmit mode, $f_{REF} = 40MHz$, and registers set to recommended settings and corresponding test mode, unless otherwise noted. Typical values are at $V_{CC} = 2.8V$, $V_{CCPA} = 3.3V$, and $T_A = +25^{\circ}C$, LO frequency = $2.437GHz$, unless otherwise noted. RF inputs/outputs specifications are referenced to device pins and do not include 1dB loss from EV kit PCB, balun, and SMA connectors.) (Note 1)

PARAMETERS	CONDITIONS	MIN	TYP	MAX	UNITS
LOGIC INPUTS: \overline{SHDN}, $RXTX$, $SCLK$, DIN, \overline{CS}, B7:B1, $RXHP$					
Digital Input-Voltage High, V_{IH}		$V_{CC} - 0.4$			V
Digital Input-Voltage Low, V_{IL}				0.4	V
Digital Input-Current High, I_{IH}		-1		+1	μA
Digital Input-Current Low, I_{IL}		-1		+1	μA
LOGIC OUTPUTS: LD, CLOCKOUT					
Digital Output-Voltage High, V_{OH}	Sourcing $100\mu A$	$V_{CC} - 0.4$			V
Digital Output-Voltage Low, V_{OL}	Sinking $100\mu A$			0.4	V

AC ELECTRICAL CHARACTERISTICS—Rx Mode

(MAX2831 EV kit: $V_{CC_} = 2.8V$, $V_{CCPA} = V_{CCTXPA} = 3.3V$, $T_A = +25^{\circ}C$, $f_{RF} = 2.439GHz$, $f_{LO} = 2.437GHz$; receiver baseband I/Q outputs at $112mV_{RMS}$ ($-19dBV$), $f_{REF} = 40MHz$, $\overline{SHDN} = \overline{CS} =$ high, $RXTX = SCLK = DIN =$ low, with power matching for the differential RF pins using the typical applications and registers set to default settings and corresponding test mode, unless otherwise noted. Unmodulated single-tone RF input signal is used with specifications which normally apply over the entire operating conditions, unless otherwise indicated. RF inputs/outputs specifications are referenced to device pins and do not include 1dB loss from EV kit PCB, balun, and SMA connectors.) (Note 1)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
RECEIVER SECTION: LNA RF INPUT-TO-BASEBAND I/Q OUTPUTS					
RF Input Frequency Range		2.4		2.5	GHz
RF Input Return Loss	High RF gain		18		dB
	Mid RF gain		11		
	Low RF gain		14		
Total Voltage Gain	Maximum gain, B7:B1 = 1111111	$T_A = +25^{\circ}C$	86	98	dB
		$T_A = -40^{\circ}C$ to $+85^{\circ}C$	83		
	Minimum gain, B7:B1 = 0000000	$T_A = +25^{\circ}C$	3	8	
RF Gain Steps (Note 3)	From high-gain mode (B7:B6 = 11) to medium-gain mode (B7:B6 = 10)		-16		dB
	From high-gain mode (B7:B6 = 11) to low-gain mode (B7:B6 = 0X)		-33		
RF Gain-Change Settling Time	Gain change from high gain to medium gain, high gain to low, or medium gain to low gain; gain settling to within $\pm 2dB$ of steady state; $RXHP = 1$		0.2		μs

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AC ELECTRICAL CHARACTERISTICS—Rx Mode (continued)

(MAX2831 EV kit: $V_{CC-} = 2.8V$, $V_{CCPA} = V_{CCTXPA} = 3.3V$, $T_A = +25^{\circ}C$, $f_{RF} = 2.439GHz$, $f_{LO} = 2.437GHz$; receiver baseband I/Q outputs at 112 mV_{RMS} (-19dBV), $f_{REF} = 40MHz$, $\overline{SHDN} = \overline{CS} = high$, $RXTX = SCLK = DIN = low$, with power matching for the differential RF pins using the typical applications and registers set to default settings and corresponding test mode, unless otherwise noted. Unmodulated single-tone RF input signal is used with specifications which normally apply over the entire operating conditions, unless otherwise indicated. RF inputs/outputs specifications are referenced to device pins and do not include 1dB loss from EV kit PCB, balun, and SMA connectors.) (Note 1)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Baseband Gain Range	From maximum baseband gain (B5:B1 = 11111) to minimum baseband gain (B5:B1 = 00000)	55	62	67	dB
DSB Noise Figure	Voltage gain = maximum with B7:B6 = 11		2.6		dB
	Voltage gain = 50dB with B7:B6 = 11		3.2		
	Voltage gain = 45dB with B7:B6 = 10		16		
	Voltage gain = 15dB with B7:B6 = 0X		34		
In-Band Compression Point Based on EVM	-19dBV _{RMS} baseband output EVM degrades to 9%	B7:B6 = 11		-41	dBm
		B7:B6 = 10		-24	
		B7:B6 = 0X		-6	
In-Band Output P-1dB	Voltage gain = 90dB, with B7:B6 = 11		2.5		V _{P-P}
Out-of-Band Input IP3 (Note 4)	B7:B6 = 11		-12		dBm
	B7:B6 = 10		-4		
	B7:B6 = 0X		24		
I/Q Phase Error	1 σ variation (without calibration)		± 0.35		Degrees
I/Q Gain Imbalance	1 σ variation (without calibration)		± 0.1		dB
RX I/Q Output Load Impedance (R C)	Minimum differential resistance		10		k Ω
	Maximum differential capacitance		10		pF
Tx-to-Rx Conversion Gain for Rx I/Q Calibration	For receiver gain, B7:B1 = 1101111 (Note 5)		0.5		dB
Baseband VGA Settling Time	Gain change from B5:B1 = 10111 to B5:B1 = 00111; gain settling to within $\pm 2dB$ of steady state		0.1		μs
I/Q Output DC Step when RXHP Transitions from 1 to 0 in Presence of 802.11g Short Sequence	After switching RXHP to logic 0 from initial logic 1, during ideal short sequence data at -55dBm input in AWGN channel, for -19dBV output; normalized to RMS signal on I and Q outputs; transition point varied from 0 to 0.8 μs in steps of 0.1 μs		-5		dBc
I/Q Output DC Droop	After switching RXHP to 0, D13:D12, Register 7 (A3:A0 = 0111)		± 1		V/s
I/Q Static DC Offset	RXHP = 1, B7:B1 = 1101110, 1 σ variation		± 1		mV
Spurious Signal Emissions from LNA input	RF = 1GHz to 26.5GHz		-51		dBm
RECEIVER BASEBAND FILTERS					
Gain Ripple in Passband	10kHz to 8.5MHz at baseband		± 1.3		DB _{P-P}
Group-Delay Ripple in Passband	10kHz to 8.5MHz at baseband		± 45		nsp-p

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AC ELECTRICAL CHARACTERISTICS—Rx Mode (continued)

(MAX2831 EV kit: $V_{CC-} = 2.8V$, $V_{CCPA} = V_{CCTXPA} = 3.3V$, $T_A = +25^{\circ}C$, $f_{RF} = 2.439GHz$, $f_{LO} = 2.437GHz$; receiver baseband I/Q outputs at 112 mV_{RMS} (-19dBV), $f_{REF} = 40MHz$, $\overline{SHDN} = \overline{CS} = high$, $RXTX = SCLK = DIN = low$, with power matching for the differential RF pins using the typical applications and registers set to default settings and corresponding test mode, unless otherwise noted. Unmodulated single-tone RF input signal is used with specifications which normally apply over the entire operating conditions, unless otherwise indicated. RF inputs/outputs specifications are referenced to device pins and do not include 1dB loss from EV kit PCB, balun, and SMA connectors.) (Note 1)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Baseband Filter Rejection (Nominal Mode)	At 8.5MHz		3.2		dB
	At 15MHz		27		
	At 20MHz		50		
	At > 40MHz		80		
RSSI					
RSSI Minimum Output Voltage	$R_{LOAD} \geq 10k\Omega \parallel 5pF$		0.4		V
RSSI Maximum Output Voltage	$R_{LOAD} \geq 10k\Omega \parallel 5pF$		2.4		V
RSSI Slope			30		mV/dB
RSSI Output Settling Time	To within 3dB of steady state	+32dB signal step	200		ns
		-32dB signal step	600		

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AC ELECTRICAL CHARACTERISTICS—Tx Mode

(MAX2831 EV kit: $V_{CC_} = 2.8V$, $V_{CCPA} = V_{CCTXPA} = 3.3V$, $T_A = +25^\circ C$, $f_{RF} = 2.439GHz$, $f_{LO} = 2.437GHz$, $f_{REF} = 40MHz$, $\overline{SHDN} = RXTX = \overline{CS} = high$, and $SCLK = DIN = low$, with power matching for the differential RF pins using the typical applications circuit. 100mV_{RMS} sine and cosine signal (or 100mV_{RMS} 54Mbps IEEE 802.11g I/Q signals wherever OFDM is mentioned) applied to base-band I/Q inputs of transmitter (differential DC-coupled). Registers set to recommend settings and corresponding test mode, unless otherwise noted. RF inputs/outputs specifications are referenced to device pins and do not include 1dB loss from EV kit PCB, balun, and SMA connectors.) (Note 1)

PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
TRANSMIT SECTION: Tx BASEBAND I/Q INPUTS TO RF OUTPUTS						
RF Output Frequency Range			2.4		2.5	GHz
Output Power	MAX2831	54Mbps 802.11g OFDM signal	Output power adjusted to meet 5.6% EVM, and spectral mask		18.5	dBm
			B6:B1 = 000000		-7.5	
		802.11b signal, 141mV _{RMS} , IEEE802.11b I/Q signals	Output power adjusted to meet spectral mask		21	
	MAX2832	-3dB VGA back off			-5.3	
		B6:B1 = 000000			-31.5	
Unwanted Sideband Suppression	Without I/Q calibration, B6:B1 = 100001				-42	dBc
Carrier Leakage at Center Frequency of Channel	Without DC offset correction				-30	dBc
Transmitter Spurious Signal Emissions (MAX2831)	B6:B1 = 111000, OFDM signal	$1/3 \times f_{LO}$			-67	dBm/MHz
		< 1GHz			-36	
		> 1GHz			-47	
		$2/3 \times f_{LO}$			-64	
		$4/3 \times f_{LO}$			-42	
		$5/3 \times f_{LO}$			-65	
		$8/3 \times f_{LO}$			-51	
		$2 \times f_{LO}$			-33	
		$3 \times f_{LO}$			-54	
Transmitter Spurious Signal Emissions (MAX2832)	B6:B1 = 111111, OFDM signal	$1/3 \times f_{LO}$			-78	dBm/MHz
		< 1GHz			-65	
		> 1GHz			-72	
		$2/3 \times f_{LO}$			-78	
		$4/3 \times f_{LO}$			-46	
		$5/3 \times f_{LO}$			-72	
		$8/3 \times f_{LO}$			-46	
		$2 \times f_{LO}$			-60	
		$3 \times f_{LO}$			-75	

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AC ELECTRICAL CHARACTERISTICS—Tx Mode (continued)

(MAX2831 EV kit: $V_{CC_} = 2.8V$, $V_{CCPA} = V_{CCTXPA} = 3.3V$, $T_A = +25^\circ C$, $f_{RF} = 2.439GHz$, $f_{LO} = 2.437GHz$, $f_{REF} = 40MHz$, $\overline{SHDN} = RXTX = \overline{CS} = \text{high}$, and $SCLK = \overline{DIN} = \text{low}$, with power matching for the differential RF pins using the typical applications circuit. 100mV_{RMS} sine and cosine signal (or 100mV_{RMS} 54Mbps IEEE 802.11g I/Q signals wherever OFDM is mentioned) applied to baseband I/Q inputs of transmitter (differential DC-coupled). Registers set to recommend settings and corresponding test mode, unless otherwise noted. RF inputs/outputs specifications are referenced to device pins and do not include 1dB loss from EV kit PCB, balun, and SMA connectors.) (Note 1)

PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
RF Output Return Loss	Off-chip balun + match, single-ended	MAX2831		-20		dB
		MAX2832		-10		
Tx I/Q Input Load Impedance (R C)	Minimum differential resistance			20		k Ω
	Maximum differential capacitance			0.7		pF
Baseband -3dB Corner Frequency	D1:D0 = 01, Register 8 (A3:A0 = 1000)	Nominal mode		11		MHz
Baseband Filter Rejection	At 30MHz, in nominal mode			62		dB
Minimum Power Detector Output Voltage	Short sequence transmitter power = +9dBm			0.3		V
Maximum Power Detector Output Voltage	Short sequence transmitter power = +19dBm			1.2		V
RF Power Detector Response Time				0.3		μs
TRANSMITTER LO LEAKAGE AND I/Q CALIBRATION USING LO LEAKAGE AND SIDEBAND DETECTOR (see the Tx/Rx Calibration Mode section)						
Tx BASEBAND I/Q INPUTS TO RECEIVER OUTPUTS						
LO Leakage and Sideband Detector Output	Calibration register, D12:D11 = 00, A3:A0 = 0110	Output at 1 x f_{TONE} (for LO leakage = -29dBc), $f_{TONE} = 2MHz$, 100mV _{RMS}		-34		dBV _{RMS}
		Output at 2 x f_{TONE} (for LO leakage = -240dBc), $f_{TONE} = 2MHz$, 100mV _{RMS}		-44		
Amplifier Gain Range	D12:D11 = 00 to D12:D11 = 11, A3:A0 = 0110			30		dB
Lower -3dB Corner Frequency				1		MHz

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AC ELECTRICAL CHARACTERISTICS—Frequency Synthesis

(MAX2831 EV kit: $V_{CC-} = 2.7V$, $V_{CCPA} = V_{CCTXPA} = 3.3V$, $T_A = +25^\circ C$, $f_{LO} = 2.437GHz$, $f_{REF} = 40MHz$, $\overline{SHDN} = \overline{CS} = \text{high}$, $SCLK = DIN = \text{low}$, PLL loop bandwidth = 150kHz, and $T_A = +25^\circ C$, unless otherwise noted.) (Note 1)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
FREQUENCY SYNTHESIZER					
RF Channel Center Frequency		2.4		2.5	GHz
Channel Center Frequency Programming Minimum Step Size			20		Hz
Charge-Pump Comparison Frequency			20		MHz
Reference Frequency Range		20		44	MHz
Reference Frequency Input Levels	AC-coupled to XTAL pin	800			mV _{p-p}
Reference Frequency Input Impedance (R C)	Resistance (XTAL)		5		k Ω
	Capacitance (XTAL)		4		pF
Closed-Loop Phase Noise	$f_{\text{OFFSET}} = 1kHz$		-86		dBc/Hz
	$f_{\text{OFFSET}} = 10kHz$		-94		
	$f_{\text{OFFSET}} = 100kHz$		-94		
	$f_{\text{OFFSET}} = 1MHz$		-110		
	$f_{\text{OFFSET}} = 10MHz$		-120		
Closed-Loop Integrated Phase Noise	RMS phase jitter; integrate from 10kHz to 10MHz offset		0.9		Degrees
Charge-Pump Output Current			1		mA
Reference Spurs	20MHz offset		-55		dBc
VCO Frequency Error	Measured from Tx-Rx or Rx-Tx transition	$3\mu s$ to $9\mu s$	50		kHz
		$> 9\mu s$	1		
VOLTAGE-CONTROLLED OSCILLATOR					
Pushing	Referred to 2400MHz LO, V_{CC} varies by 0.3V		210		kHz
VCO Tuning Voltage Range		0.5		2.2	V
LO Tuning Gain	$V_{TUNE} = 0.5V$		103		MHz/V
	$V_{TUNE} = 2.2V$		86		

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AC ELECTRICAL CHARACTERISTICS—Miscellaneous Blocks

(MAX2831 EV kit: $V_{CC_} = 2.8V$, $V_{CCPA} = V_{CCTXPA} = 3.3V$, $f_{LO} = 2.437GHz$, $f_{REF} = 40MHz$, $\overline{SHDN} = \overline{CS} = high$, $SCLK = DIN = low$, and $T_A = +25^\circ C$, unless otherwise noted.) (Note 1)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
CRYSTAL OSCILLATOR					
On-Chip Tuning Capacitance Range	Maximum capacitance, A3:A0 = 1110, D6:D0 = 1111111		15.4		pF
	Minimum capacitance, A3:A0 = 1110, D6:D0 = 0000000		0.5		
On-Chip Tuning Capacitance Step Size			0.12		pF
ON-CHIP TEMPERATURE SENSOR					
Output Voltage	A3:A0 = 1000, D9:D8 = 01	$T_A = -40^\circ C$	0.35		V
		$T_A = +25^\circ C$	1		
		$T_A = +85^\circ C$	1.6		

AC ELECTRICAL CHARACTERISTICS—Timing

(MAX2831 EV kit: $V_{CC_} = 2.8V$, $V_{CCPA} = V_{CCTXPA} = 3.3V$, $T_A = +25^\circ C$, $f_{LO} = 2.437GHz$, $f_{REF} = 40MHz$, $\overline{SHDN} = \overline{CS} = high$, $SCLK = DIN = low$, PLL loop bandwidth = 150kHz, and $T_A = +25^\circ C$, unless otherwise noted.) (Note 1)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
SYSTEM TIMING (See Figure 3)					
Turn-On Time	From \overline{SHDN} rising edge to LO settled within 1kHz using external reference frequency input		60		μs
Crystal Oscillator Turn-On Time	90% of final output amplitude level		1		ms
Channel Switching Time	Loop BW = 150kHz, $f_{RF} = 2.5GHz$ to 2.4GHz		25		μs
Rx/Tx Turnaround Time	Measured from Tx or Rx enable rising edge; signal settling to within $\pm 2dB$ of steady state	Rx to Tx	2		μs
		Tx to Rx, RXHP = 1	2		
Tx Turn-On Time (from Standby Mode)	From Tx-enable active rising edge; signal settling to within $\pm 2dB$ of steady state		1.5		μs
Tx Turn-Off Time (from Standby Mode)	From Tx-enable inactive rising edge		1		μs
Rx Turn-On Time (from Standby Mode)	From Rx-enable active rising edge; signal settling to within $\pm 2dB$ of steady state		1.9		μs
Rx Turn-Off Time (from Standby Mode)	From Rx-enable inactive rising edge		0.1		μs

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AC ELECTRICAL CHARACTERISTICS—Timing (continued)

(MAX2831 EV kit: $V_{CC_} = 2.8V$, $V_{CCPA} = V_{CCTXPA} = 3.3V$, $T_A = +25^\circ C$, $f_{LO} = 2.437GHz$, $f_{REF} = 40MHz$, $\overline{SHDN} = \overline{CS} = \text{high}$, $SCLK = DIN = \text{low}$, PLL loop bandwidth = 150kHz, and $T_A = +25^\circ C$, unless otherwise noted.) (Note 1)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
3-WIRE SERIAL-INTERFACE TIMING (See Figure 2)					
SCLK Rising Edge to \overline{CS} Falling Edge Wait Time, t_{CSO}			6		ns
Falling Edge of \overline{CS} to Rising Edge of First SCLK Time, t_{CSS}			6		ns
DIN to SCLK Setup Time, t_{DS}			6		ns
DIN to SCLK Hold Time, t_{DH}			6		ns
SCLK Pulse-Width High, t_{CH}			6		ns
SCLK Pulse-Width Low, t_{CL}			6		ns
Last Rising Edge of SCLK to Rising Edge of \overline{CS} or Clock to Load Enable Setup Time, t_{CSH}			6		ns
\overline{CS} High Pulse Width, t_{CSW}			20		ns
Time Between the Rising Edge of \overline{CS} and the Next Rising Edge of SCLK, t_{CS1}			6		ns
Clock Frequency, f_{CLK}			20		MHz
Rise Time, t_R			2		ns
Fall Time, t_F			2		ns

Note 1: Min and max limits are guaranteed by test at $T_A = +25^\circ C$ and $+85^\circ C$ and guaranteed by design and characterization at $T_A = -40^\circ C$. The power-on register settings are not production tested. Recommended register setting must be loaded after V_{CC} is supplied.

Note 2: Guaranteed by design and characterization.

Note 3: The nominal part-to-part variation of the RF gain step is $\pm 1dB$.

Note 4: Two tones at +25MHz and +48MHz offset with -35dBm/tone. Measure IM3 at 2MHz.

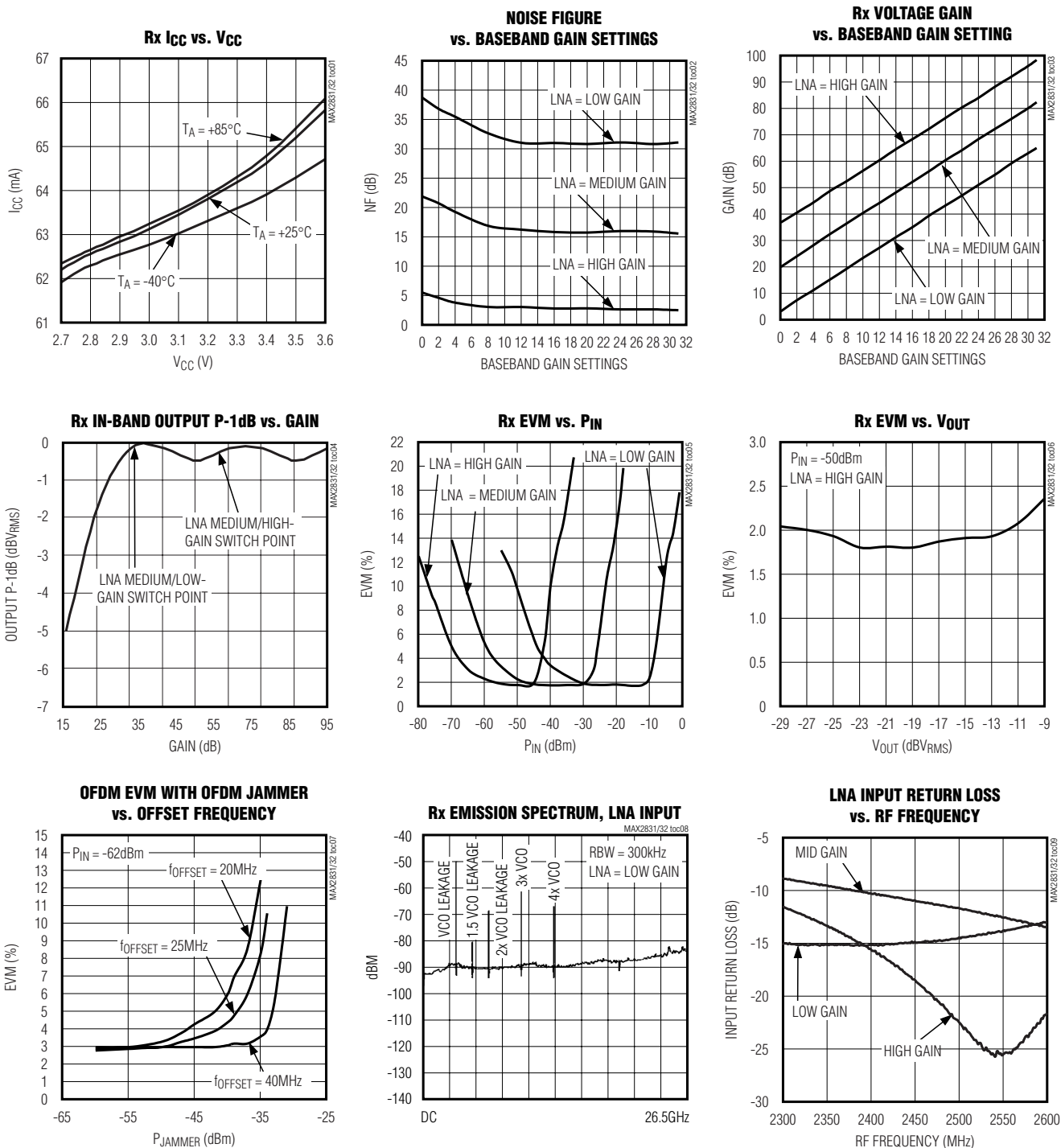
Note 5: Tx I/Q inputs = 100mVRMS.

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Typical Operating Characteristics

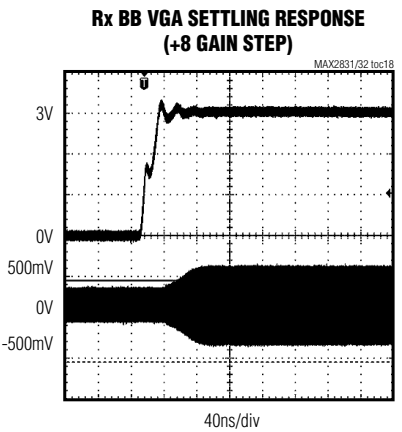
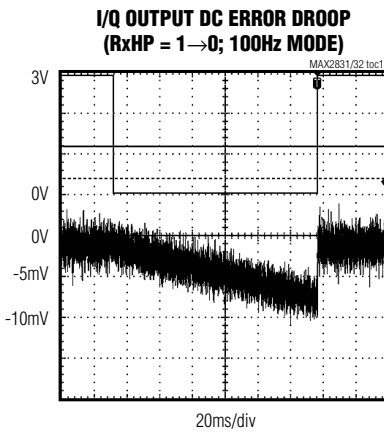
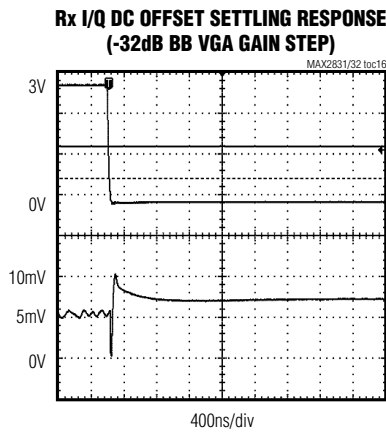
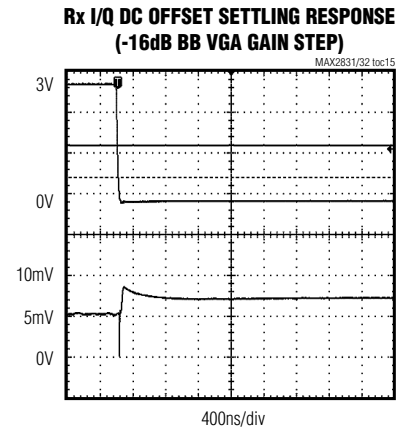
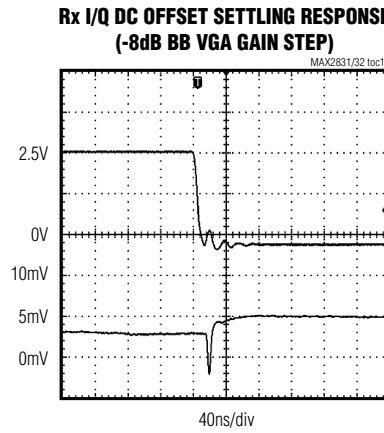
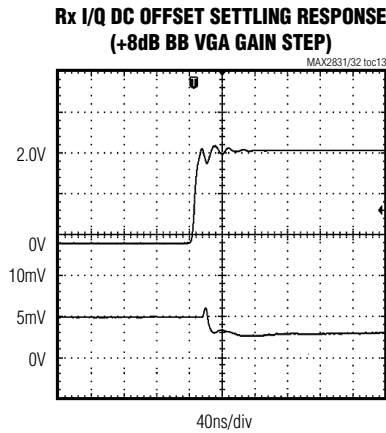
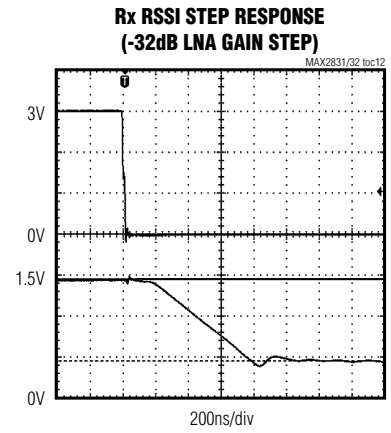
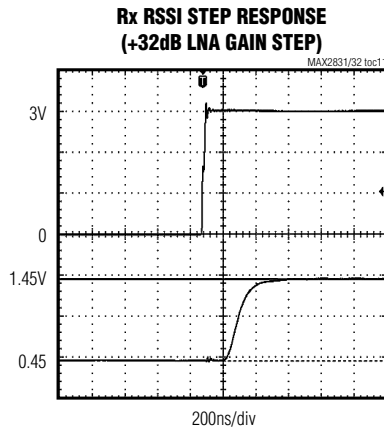
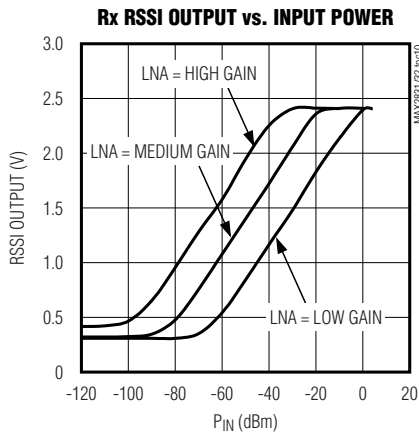
(MAX2831 EV kit, $V_{CC-} = 2.8V$, $V_{CCPA} = V_{CCTXPA} = 3.3V$, $T_A = +25^{\circ}C$, $f_{LO} = 2.437GHz$, $f_{REF} = 40MHz$, $\overline{SHDN} = \overline{CS} = high$, $RXHP = SCLK = DIN = low$.)



2.4GHz to 2.5GHz 802.11g/b RF Transceivers with Integrated PA

Typical Operating Characteristics (continued)

(MAX2831 EV kit, $V_{CC_} = 2.8V$, $V_{CCPA} = V_{CCTXPA} = 3.3V$, $T_A = +25^\circ C$, $f_{LO} = 2.437GHz$, $f_{REF} = 40MHz$, $\overline{SHDN} = \overline{CS} = high$, $RXHP = SCLK = DIN = low$.)



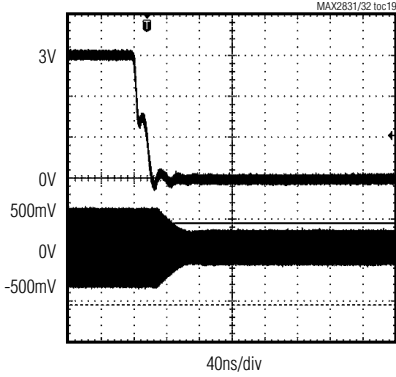
2.4GHz to 2.5GHz 802.11g/b RF Transceivers with Integrated PA

MAX2831/MAX2832

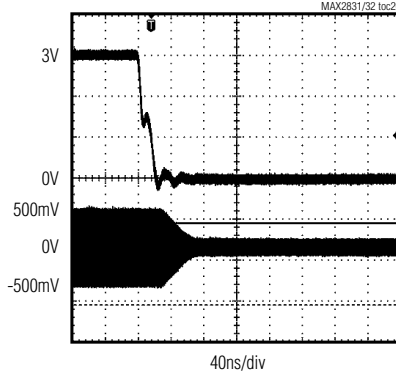
Typical Operating Characteristics (continued)

(MAX2831 EV kit, $V_{CC_} = 2.8V$, $V_{CCPA} = V_{CCXPA} = 3.3V$, $T_A = +25^\circ C$, $f_{LO} = 2.437GHz$, $f_{REF} = 40MHz$, $\overline{SHDN} = \overline{CS} = high$, $RXHP = SCLK = DIN = low$.)

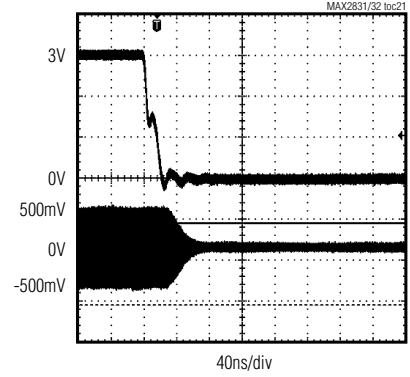
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(-8 GAIN STEP)**



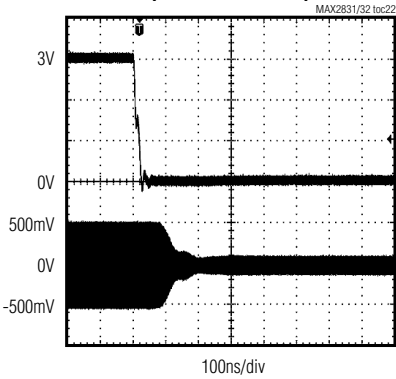
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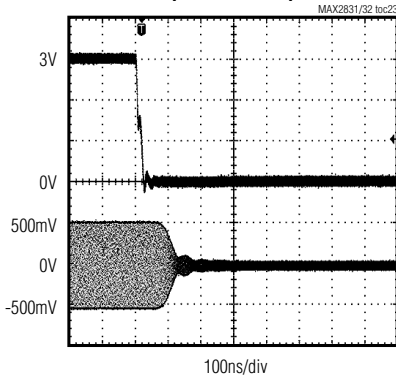
**Rx BB VGA SETTLING RESPONSE
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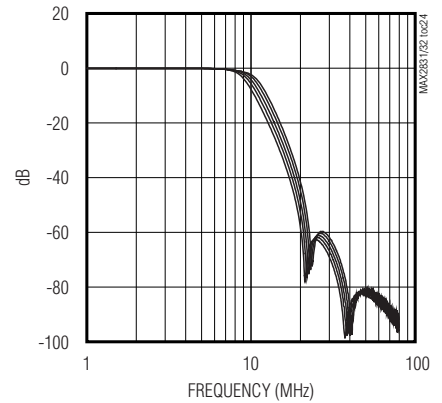
**RF LNA SETTLING RESPONSE
(HIGH TO MEDIUM)**



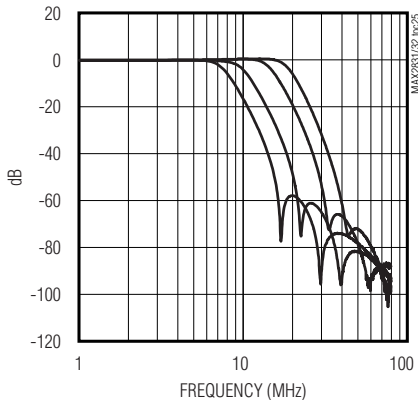
**RF LNA SETTLING RESPONSE
(HIGH TO LOW)**



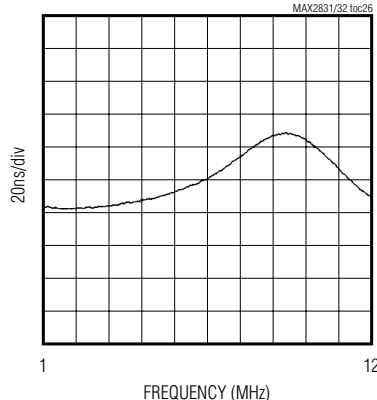
**Rx BB FREQUENCY RESPONSE vs.
FINE SETTING (COARSE SETTING = 8.5MHz)**



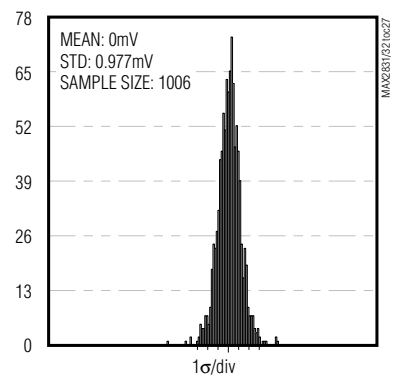
**Rx BB FREQUENCY RESPONSE vs.
COARSE SETTING (FINE SETTING = 010)**



**RX BASEBAND FILTER
GROUP DELAY**



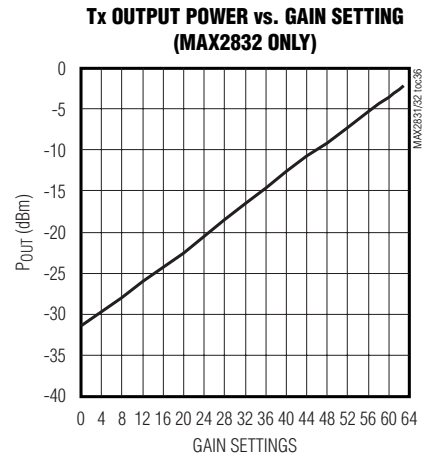
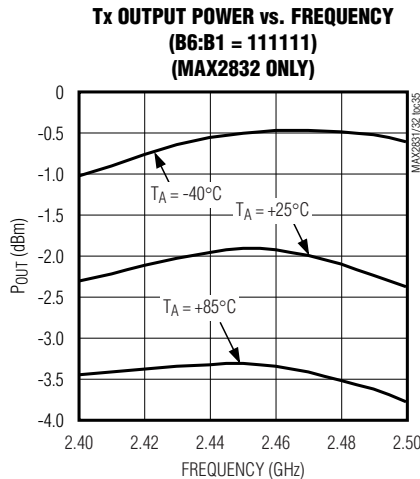
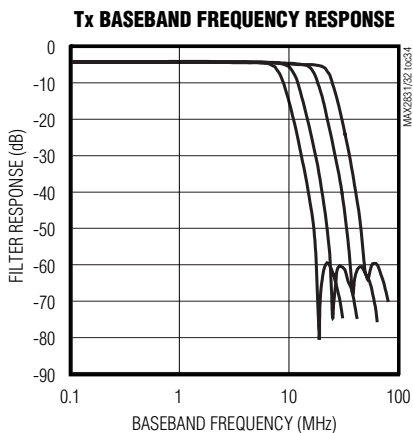
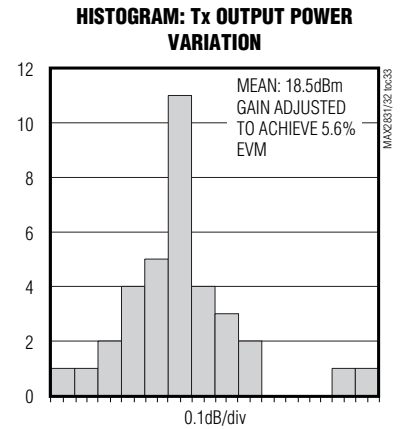
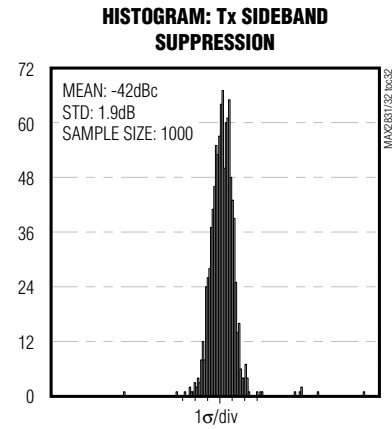
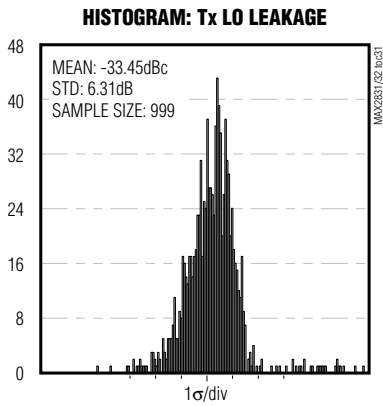
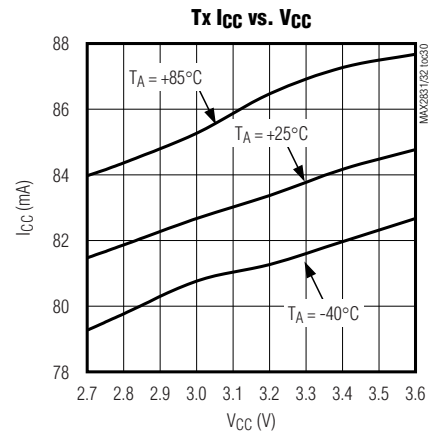
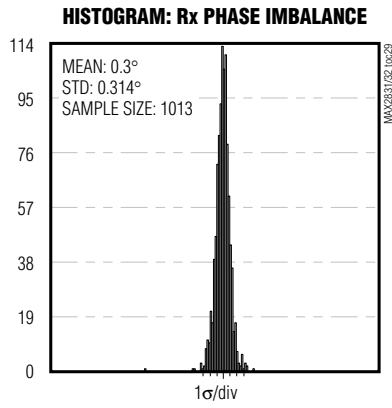
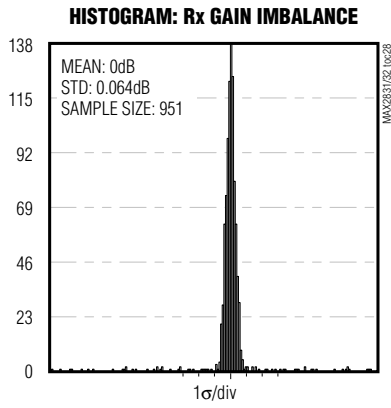
HISTOGRAM: Rx STATIC DC OFFSET



2.4GHz to 2.5GHz 802.11g/b RF Transceivers with Integrated PA

Typical Operating Characteristics (continued)

(MAX2831 EV kit, $V_{CC_} = 2.8V$, $V_{CCPA} = V_{CCTXPA} = 3.3V$, $T_A = +25^\circ C$, $f_{LO} = 2.437GHz$, $f_{REF} = 40MHz$, $\overline{SHDN} = \overline{CS} = high$, $RXHP = SCLK = DIN = low$.)

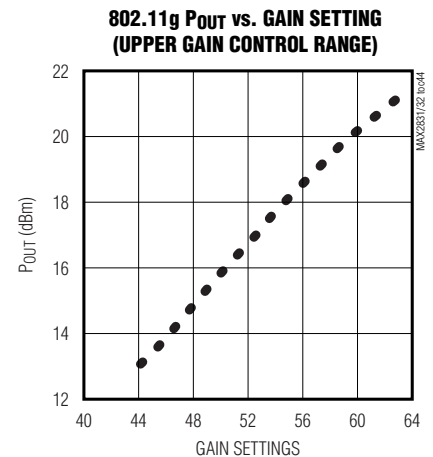
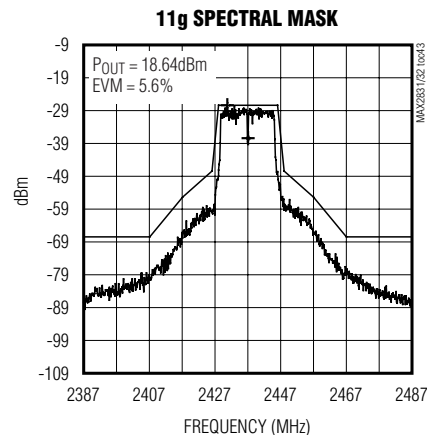
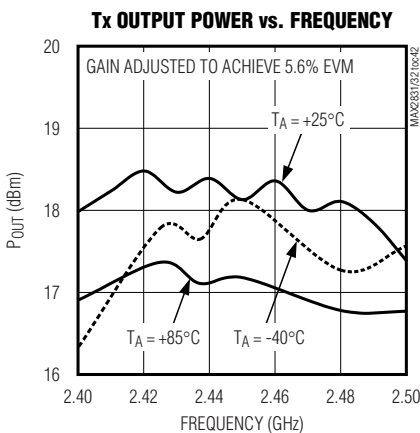
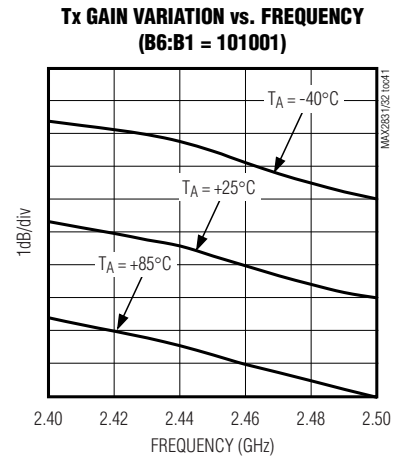
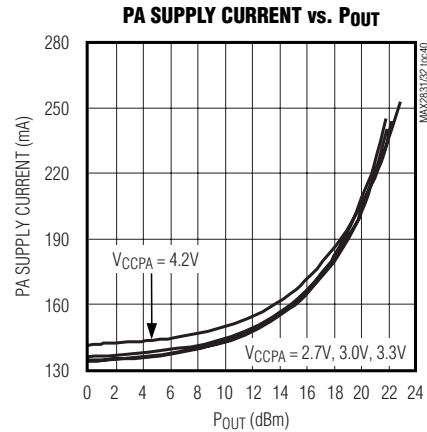
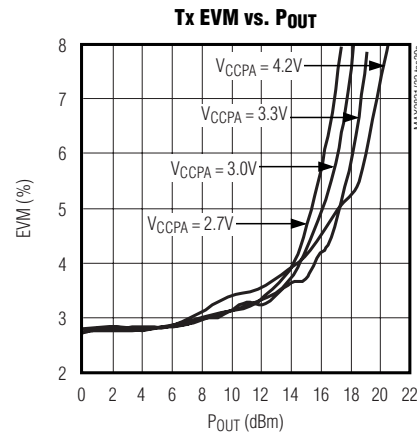
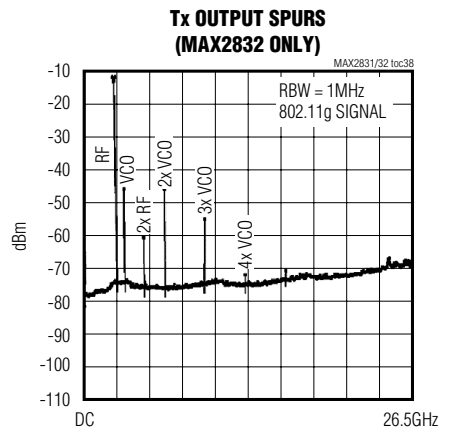
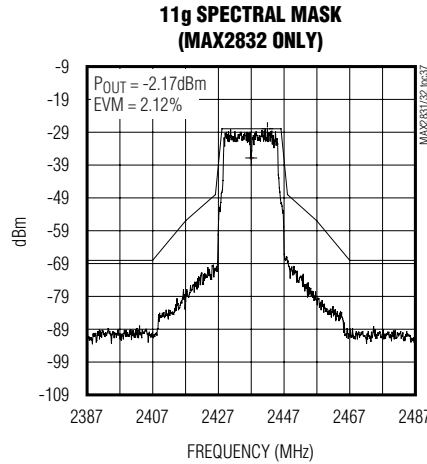
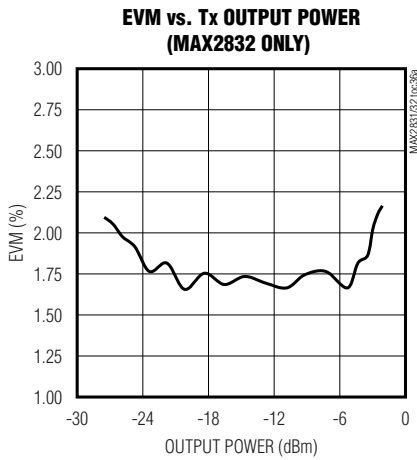


2.4GHz to 2.5GHz 802.11g/b RF Transceivers with Integrated PA

MAX2831/MAX2832

Typical Operating Characteristics (continued)

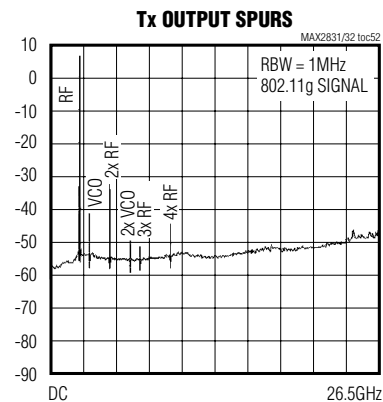
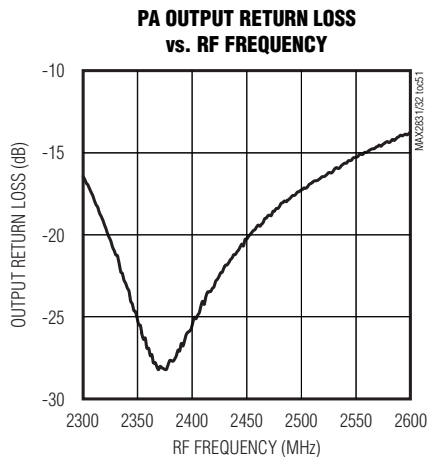
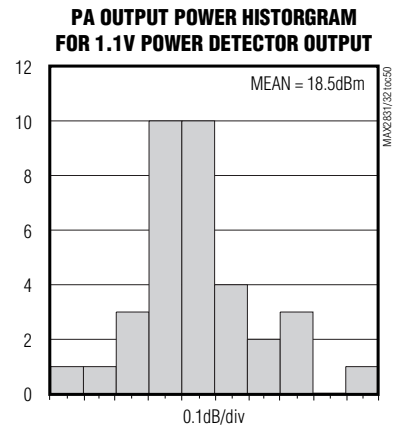
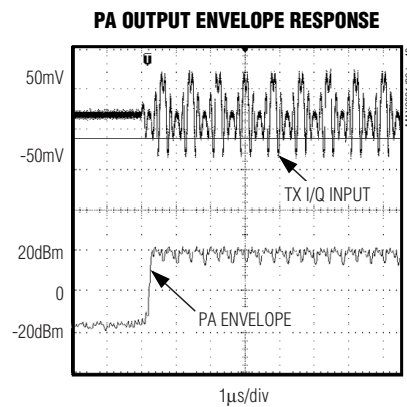
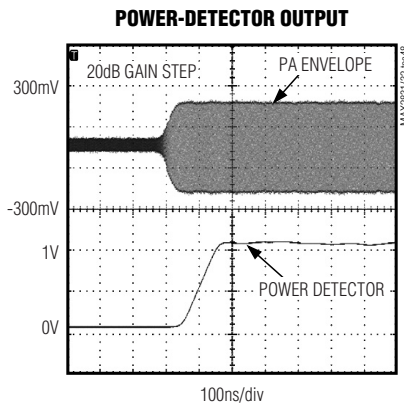
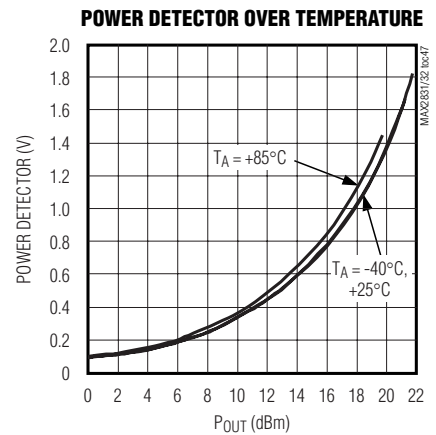
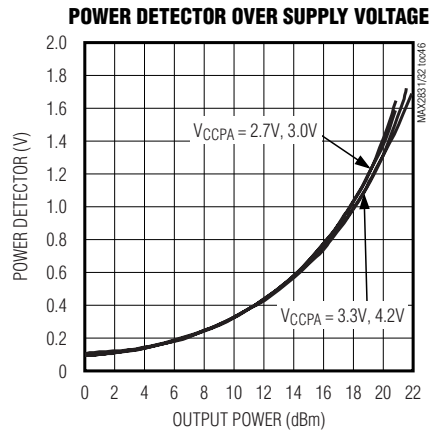
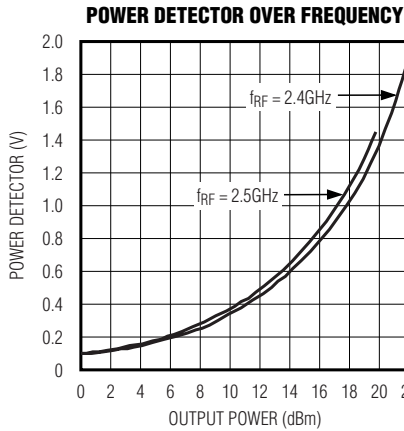
(MAX2831 EV kit, $V_{CC-} = 2.8V$, $V_{CCPA} = V_{CCTXPA} = 3.3V$, $T_A = +25^\circ C$, $f_{LO} = 2.437GHz$, $f_{REF} = 40MHz$, $\overline{SHDN} = \overline{CS} = high$, $RXHP = SCLK = DIN = low$.)



2.4GHz to 2.5GHz 802.11g/b RF Transceivers with Integrated PA

Typical Operating Characteristics (continued)

(MAX2831 EV kit, $V_{CC_} = 2.8V$, $V_{CCPA} = V_{CCTXPA} = 3.3V$, $T_A = +25^\circ C$, $f_{LO} = 2.437GHz$, $f_{REF} = 40MHz$, $\overline{SHDN} = \overline{CS} = high$, $RXHP = SCLK = DIN = low$.)

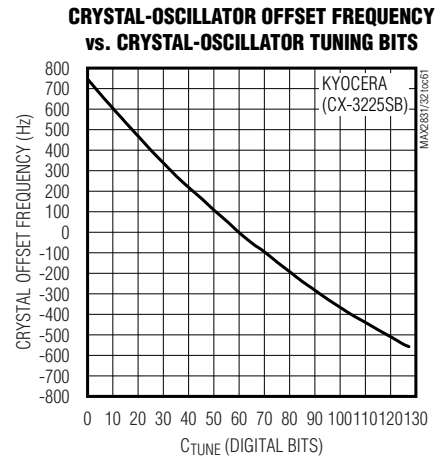
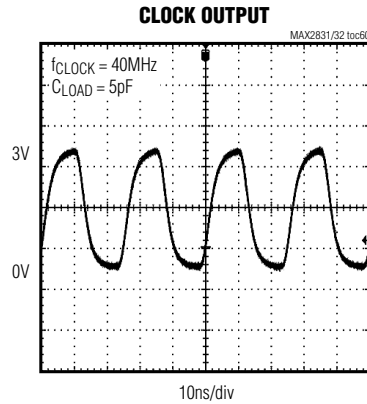
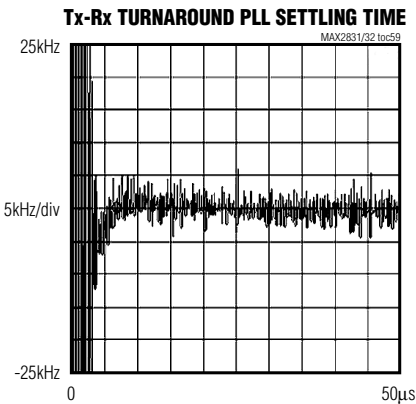
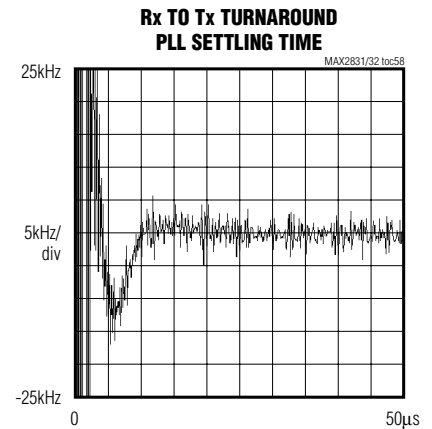
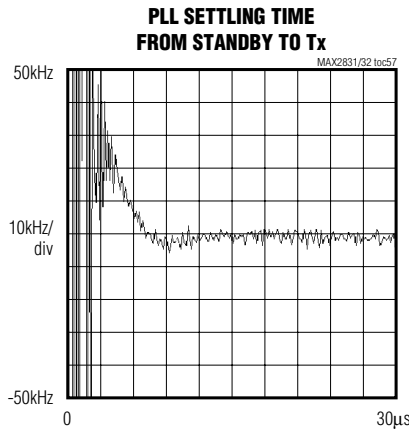
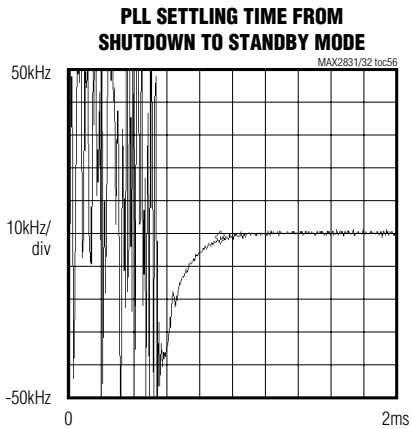
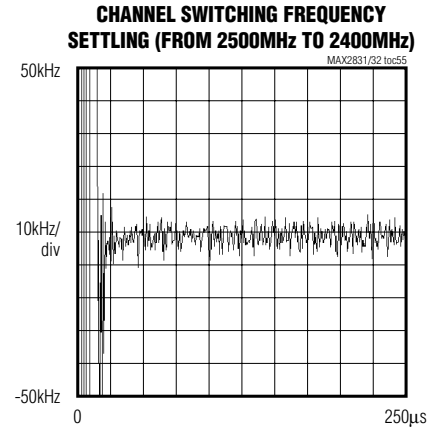
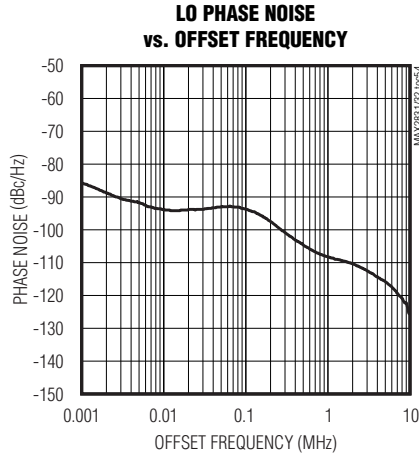
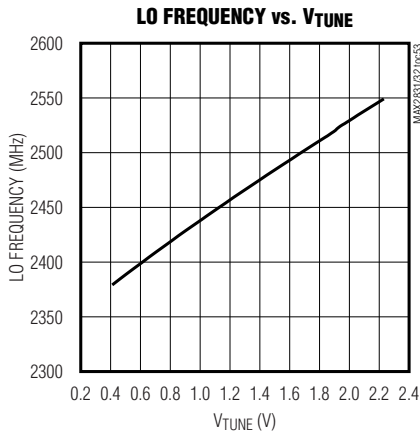


2.4GHz to 2.5GHz 802.11g/b RF Transceivers with Integrated PA

Typical Operating Characteristics (continued)

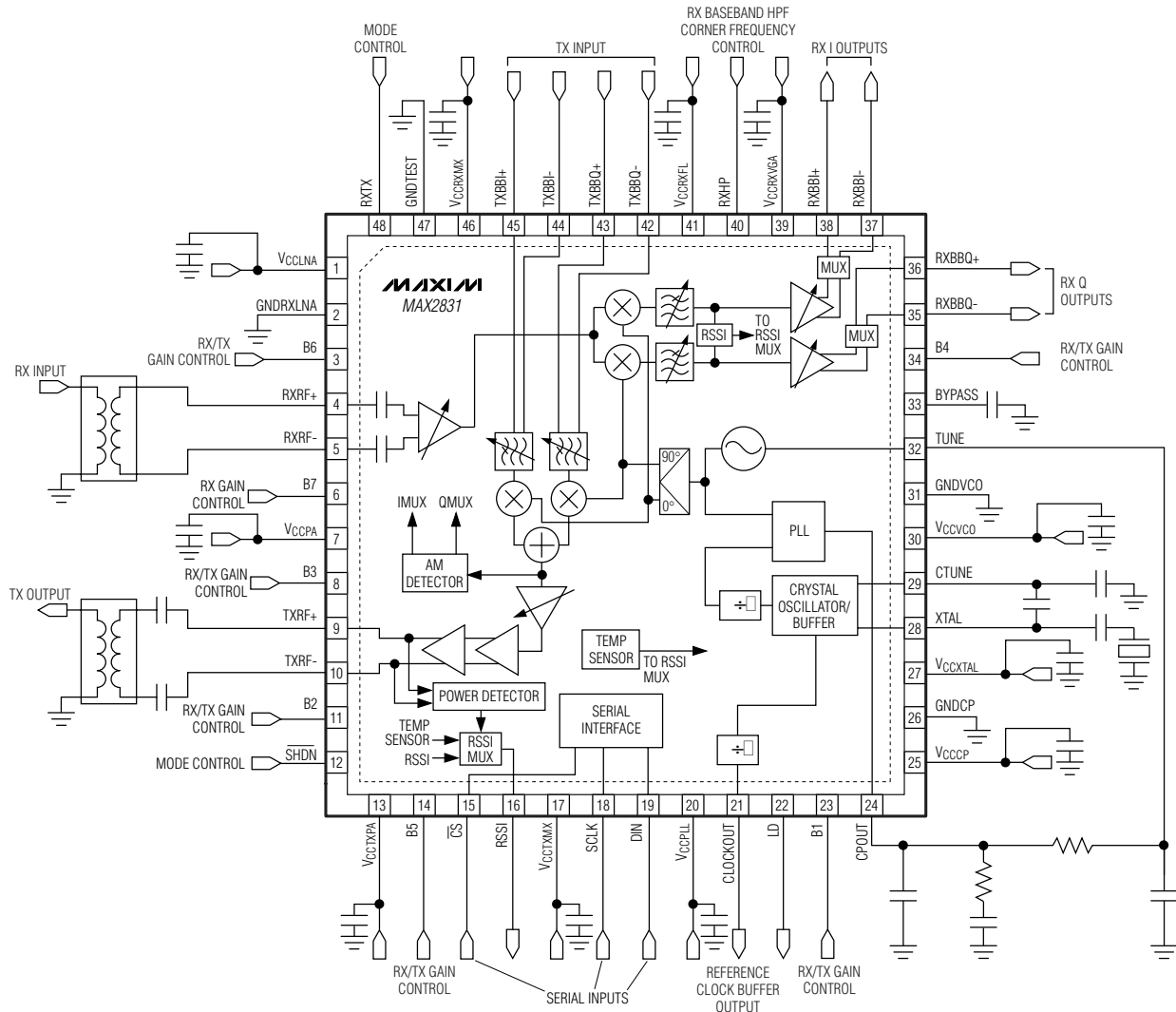
(MAX2831 EV kit, $V_{CC-} = 2.8V$, $V_{CCPA} = V_{CCTXPA} = 3.3V$, $T_A = +25^\circ C$, $f_{LO} = 2.437GHz$, $f_{REF} = 40MHz$, $\overline{SHDN} = \overline{CS} = high$, $RXHP = SCLK = DIN = low$.)

MAX2831/MAX2832



2.4GHz to 2.5GHz 802.11g/b RF Transceivers with Integrated PA

Block Diagrams/Typical Operating Circuits

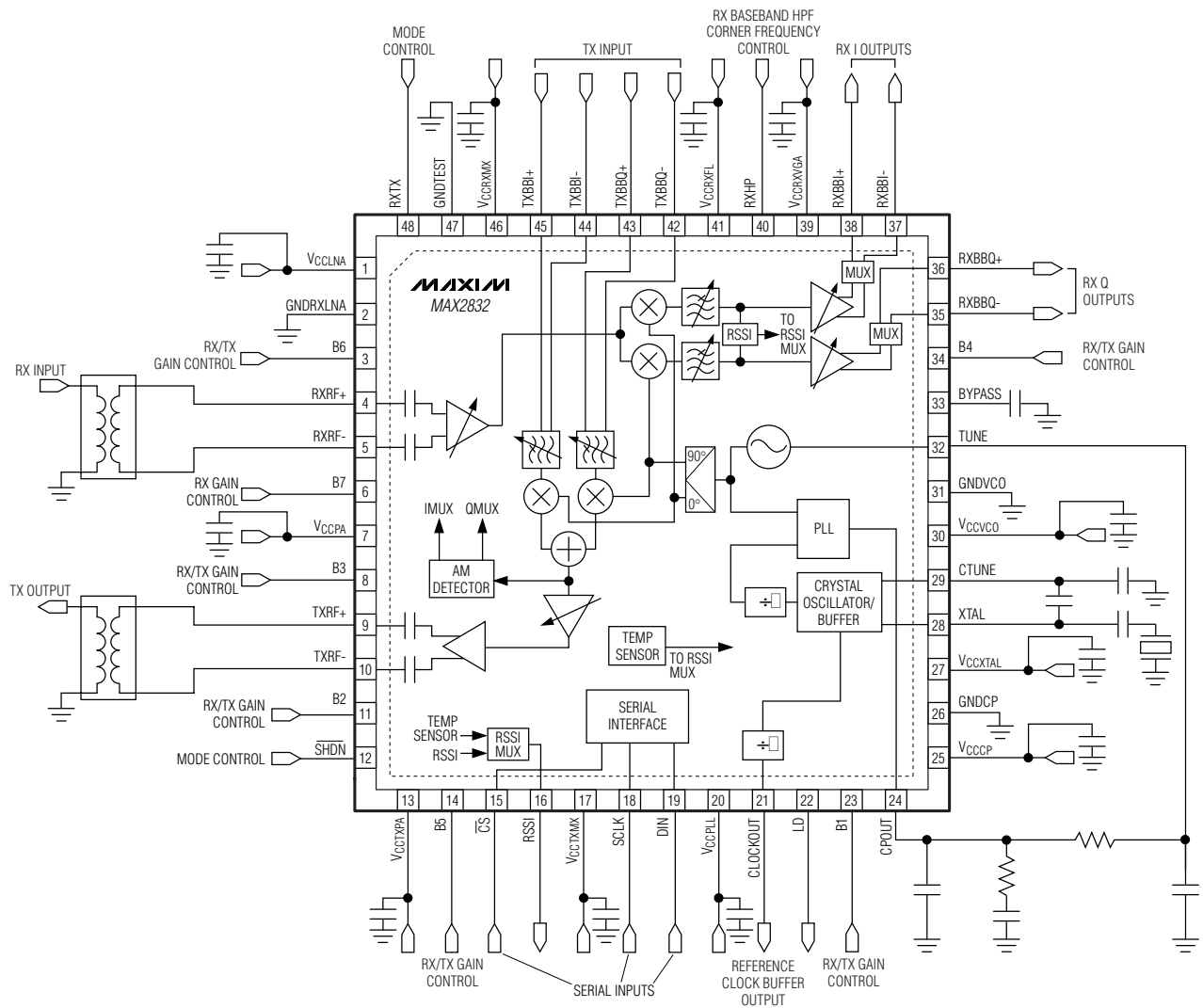


NOTE: ALL GROUND (PINS 2, 26, AND 31) AND BYPASS CAPACITORS' GROUND REQUIRE THEIR OWN VIAS TO GROUND. DO NOT CONNECT THEM TO THE EXPOSED PADDLE GROUND.

2.4GHz to 2.5GHz 802.11g/b RF Transceivers with Integrated PA

Block Diagrams/Typical Operating Circuits (continued)

MAX2831/MAX2832



NOTE: ALL GROUND (PINS 2, 26, AND 31) AND BYPASS CAPACITORS' GROUND REQUIRE THEIR OWN VIAS TO GROUND. DO NOT CONNECT THEM TO THE EXPOSED PADDLE GROUND.

2.4GHz to 2.5GHz 802.11g/b RF Transceivers with Integrated PA

Pin Description

PIN	NAME	FUNCTION
1	V _{CCLNA}	LNA Supply Voltage
2	G _{NDRXLNA}	LNA Ground
3	B6	Receiver and Transmitter Gain-Control Logic-Input Bit 6
4	R _{XRF+}	LNA Differential Input. Input is internally AC-coupled and matched to 100Ω differential. Connect directly to a 2:1 balun.
5	R _{XRF-}	
6	B7	Receiver Gain-Control Logic-Input Bit 7
7	V _{CCPA}	Supply Voltage for Second Stage of Power Amplifier
8	B3	Receiver and Transmitter Gain-Control Logic-Input Bit 3
9	T _{XRF+}	Power-Amplifier Differential Output for the MAX2831. PA output must be AC-coupled. PA driver internally AC-coupled differential outputs and matched to 100Ω differential for the MAX2832. Connect directly to a 2:1 balun.
10	T _{XRF-}	
11	B2	Receiver and Transmitter Gain-Control Logic-Input Bit 2
12	$\overline{\text{SHDN}}$	Active-Low Shutdown and Standby Logic Input. See Table 31 for operating modes.
13	V _{CCTXPA}	Supply Voltage for First-Stage of PA and PA Driver
14	B5	Receiver and Transmitter Gain-Control Logic-Input Bit 5
15	$\overline{\text{CS}}$	Active-Low Chip-Select Logic Input of 3-Wire Serial Interface (See Figure 2)
16	R _{SSI}	RSSI, PA Power Detector (MAX2831 Only) or Temperature-Sensor Multiplexed Analog Output
17	V _{CCTXMX}	Transmitter Upconverter Supply Voltage
18	S _{CLK}	Serial-Clock Logic Input of 3-Wire Serial Interface (See Figure 2)
19	D _{IN}	Data Logic Input of 3-Wire Serial Interface (See Figure 2)
20	V _{CCPLL}	PLL and Registers Supply Voltage. Connect to the supply voltage to retain the register settings.
21	C _{LOCKOUT}	Reference Clock Buffer Output
22	LD	Lock-Detect Logic Output of Frequency Synthesizer. Output high indicates that the frequency synthesizer is locked. Output programmable as CMOS or open-drain output. (See Tables 16 and 20.)
23	B1	Receiver and Transmitter Gain-Control Logic-Input Bit 1
24	C _{POUT}	Charge-Pump Output. Connect the frequency synthesizer's loop filter between C _{POUT} and TUNE (see the <i>Block Diagrams/Typical Operating Circuits</i>).
25	V _{CCCP}	PLL Charge-Pump Supply Voltage
26	G _{NDCP}	Charge-Pump Circuit Ground
27	V _{CCXTAL}	Crystal Oscillator Supply Voltage
28	X _{TAL}	Crystal or Reference Clock Input. AC-couple a crystal or a reference clock to this analog input.
29	C _{TUNE}	Connection for Crystal Oscillator Off-Chip Capacitors. When using an external reference clock input, leave C _{TUNE} unconnected.
30	V _{CCVCO}	VCO Supply Voltage
31	G _{NDVCO}	VCO Ground
32	T _{UNE}	VCO TUNE Input (see the <i>Block Diagrams/Typical Operating Circuits</i>)
33	B _{YPASS}	On-Chip VCO Regulator Output Bypass. Bypass with a 0.1μF to 1μF capacitor to GND. Do not connect other circuitry to this point.
34	B4	Receiver and Transmitter Gain-Control Logic-Input Bit 4

2.4GHz to 2.5GHz 802.11g/b RF Transceivers with Integrated PA

MAX2831/MAX2832

Pin Description (continued)

PIN	NAME	FUNCTION
35	RXBBQ-	Receiver Baseband Q-Channel Differential Outputs. In TX calibration mode, these pins are the LO leakage and sideband detector outputs.
36	RXBBQ+	
37	RXBBI-	Receiver Baseband I-Channel Differential Outputs. In TX calibration mode, these pins are the LO leakage and sideband detector outputs.
38	RXBBI+	
39	VCCR XVGA	Receiver VGA Supply Voltage
40	RXHP	Receiver Baseband AC-Coupling High-Pass Corner Frequency Control Logic Input
41	VCCR XFL	Receiver Baseband Filter Supply Voltage
42	TXBBQ-	Transmitter Baseband I-Channel Differential Inputs
43	TXBBQ+	
44	TXBBI-	Transmitter Baseband Q-Channel Differential Inputs
45	TXBBI+	
46	VCCR XMX	Receiver Downconverters Supply Voltage
47	GNDTEST	Connect to Ground
48	RXTX	RX/TX Mode Control Logic Input. See Table 31 for operating modes.
—	EP	Exposed Paddle. Connect to the ground plane with multiple vias for proper operation and heat dissipation. Do not share with any other pin grounds and bypass capacitors' ground.

Detailed Description

The MAX2831/MAX2832 single-chip, low-power, direct conversion, zero-IF transceivers are designed to support 802.11g/b applications operating in the 2.4GHz to 2.5GHz band. The fully integrated transceivers include a receive path, transmit path, voltage-controlled oscillator (VCO), sigma-delta fractional-N synthesizer, crystal oscillator, RSSI, PA power detector (MAX2831), temperature sensor, Rx and Tx I/Q error-detection circuitry, baseband-control interface and linear power amplifier (MAX2831). The only additional components required to implement a complete radio front-end solution are a crystal, a pair of baluns, a BPF, a switch, and a small number of passive components (RCs, no inductors required).

Receiver

The fully integrated receiver achieves a noise figure of 2.6dB in high-gain mode, and an input compression point of -6dBm in low-gain mode, while consuming only 62mA of supply current. The receiver integrates an LNA and VGA with a 95dB digitally programmable gain control range, direct-conversion downconverters, I/Q baseband lowpass filters with programmable LPF corner frequencies, analog RSSI and integrated DC-offset correction circuitry. A logic-low on the RXTX input (pin 48) and a logic-high on the SHDN input (pin 12) enable the receiver.

LNA Input Matching

The LNA features a differential input that is internally AC-coupled and internally matched to 100Ω. Connect a 2:1 balun transformer directly to the RXRF+ (pin 4) and RXRF- (pin 5) ports to convert the differential 100Ω input impedance to a single-ended 50Ω input. Provide electrically symmetrical input traces from the LNA input to the balun to maintain IP2 performance and RF common-mode noise rejection.

LNA Gain Control

The LNA has three gain modes: max gain, max gain - 16dB, and max gain - 33dB. The three LNA gain modes can be serially programmed through the SPI™ interface by programming bits D6:D5 in Register 11 (A3:A0 = 1011) or programmed in parallel through the digital logic gain-control pins, B7 (pin 6) and B6 (pin 3). Set bit D12 = 1 in Register 8 (A3:A0 = 1000) to enable programming through the SPI interface, or set bit D12 = 0 to enable parallel programming. See Table 1 for LNA gain-control settings.

Table 1. LNA Gain-Control Settings (Pins B7:B6 or Register A3:A0 = 1011, D6:D5)

B7 OR D6	B6 OR D5	NAME	DESCRIPTION
1	1	High	Max gain
1	0	Medium	Max gain - 16dB (typ)
0	X	Low	Max gain - 33dB (typ)

SPI is a trademark of Motorola, Inc.

2.4GHz to 2.5GHz 802.11g/b RF Transceivers with Integrated PA

Baseband Variable-Gain Amplifier

The receiver baseband variable-gain amplifiers provide 62dB of gain control range programmable in 2dB steps. The VGA gain can be serially programmed through the SPI interface by setting bits D4:D0 in Register 11 (A3:A0 = 1011) or programmed in parallel through the digital logic gain-control pins, B5 (pin 14), B4 (pin 34), B3 (pin 8), B2 (pin 11), and B1 (pin 23). Set bit D12 = 1 in Register 8 (A3:A0 = 1000) to enable serial programming through the serial interface or set bit D12 = 0 to enable parallel programming through the external logic pins. See Table 2 for the gain-step value and Table 3 for baseband VGA gain-control settings.

Receiver Baseband Lowpass Filter

The receiver integrates lowpass filters that provide an upper -3dB corner frequency of 8.5MHz (nominal mode) with 50dB of attenuation at 20MHz, and 45ns of group delay ripple in the passband (10kHz to 8.5MHz). The upper -3dB corner frequency is tightly controlled on-chip and does not require user adjustment. However, provisions are made to allow fine tuning of the upper -3dB corner frequency. In addition, coarse frequency tuning allows the -3dB corner frequency to be set to 7.5MHz (11b mode), 8.5MHz (11g mode), 15MHz (turbo 1 mode), and 18MHz (turbo 2 mode) by programming bits D1:D0 in Register 8 (A3:A0 = 1000). See Table 4. The coarse corner frequency can be fine-tuned approximately $\pm 10\%$ in 5% steps by programming bits D2:D0 in Register 7 (A3:A0 = 0111). See Table 5 for receiver LPF fine -3dB corner frequency adjustment.

Table 2. Receiver Baseband VGA Gain-Step Value (Pins B5:B1 or Register D4:D0, A3:A0 = 1011)

PIN/BIT	GAIN STEP (dB)
B1/D0	2
B2/D1	4
B3/D2	8
B4/D3	16
B5/D4	32

Table 3. Baseband VGA Gain-Control Settings in Receiver Gain-Control Register (Pin B5:B1 or Register D4:D0, A3:A0 = 1011)

B5:B1 OR D4:D0	GAIN
11111	Max
11110	Max - 2dB
11101	Max - 4dB
:	:
00000	Min

Baseband Highpass Filter and DC Offset Correction

The receiver implements programmable AC and near-DC coupling of I/Q baseband signals. Temporary AC-coupling is used to quickly remove LO leakage and other DC offsets that could saturate the receiver outputs. When DC offsets have settled, near DC-coupling is enabled to avoid attenuation of the received signal. AC-coupling is set (-3dB highpass corner frequency of 600kHz) when a logic-high is applied to RXHP (pin 40). Near DC-coupling is set (-3dB highpass corner frequency of 100Hz nominal) when a logic-low is applied to RXHP. Bits D13:D12 in Register 7 (A3:A0 = 0111) allow the near DC-coupling -3B highpass corner frequency to be set to 100Hz (D13:D12 = 00), 4kHz (D13:D12 = X1), or 30kHz (D13:D12 = 10). See Table 6.

Table 4. Receiver LPF Coarse -3dB Corner Frequency Settings in Register (A3:A0 = 1000)

BITS (D1:D0)	-3dB CORNER FREQUENCY (MHz)	MODE
00	7.5	11b
01	8.5	11g
10	15	Turbo 1
11	18	Turbo 2

Table 5. Receiver LPF Fine -3dB Corner Frequency Adjustment in Register (A3:A0 = 0111)

BITS (D2:D0)	% ADJUSTMENT RELATIVE TO COARSE SETTING
000	90
001	95
010	100
011	105
100	110

Table 6. Receiver Highpass Filter -3dB Corner Frequency Programming

RXHP	A3:A0 = 0111, D13:D12	-3dB HIGHPASS CORNER FREQUENCY (Hz)
1	XX	600k
0	00	100 (recommended)
0	X1	4k
0	10	30k

X = Don't care.

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Receiver I/Q Baseband Outputs

The differential outputs (RXBBI+, RXBBI-, RXBBQ+, RXBBQ-) of the baseband amplifiers have a differential output impedance of $\sim 300\Omega$, and are capable of driving differential loads up to $10k\Omega \parallel 10pF$. The outputs are internally biased to a common-mode voltage of 1.1V and are intended to be DC-coupled to the in-phase (I) and quadrature (Q) analog-to-digital data converter inputs of the accompanying baseband IC. Additionally, the common-mode output voltage can be adjusted from 1.1V to 1.4V through programming bits D11:D10 in Register 15 (A3:A0 = 1111).

Received Signal-Strength Indicator (RSSI)

The RSSI output (pin 16) can be programmed to multiplex an analog output voltage proportional to the received signal strength, the PA output power (MAX2831), or the die temperature. Set bits D9:D8 = 00 in Register 8 (A3:A0 = 1000) to enable the RSSI output in receive mode (off in transmit mode). Set bit D10 = 1 to enable the RSSI output when RXHP = 1, and disable the RSSI output when RXHP = 0. Set bit D10 = 0 to enable the RSSI output independent of RXHP. See Table 7 for a summary of the RSSI output versus register programming and RXHP.

The received signal strength indicator provides an analog voltage proportional to the log of the sum of the squares of the I and Q channels, measured after the receive baseband filters and before the variable-gain amplifiers. The RSSI analog output voltage is proportional to the RF input signal level and LNA gain state over a 60dB range, and is not dependent upon VGA gain. See the graph RX RSSI Output vs. Input Power in the *Typical Operating Characteristics* for further details.

Transmitter

The transmitter integrates baseband lowpass filters, direct-upconversion mixers, a VGA, a PA driver, and a linear RF PA with a power detector (MAX2831). A logic-high on the RXTX input (pin 48) and a logic-high on the SHDN input (pin 12) enable the transmitter.

Transmitter I/Q Baseband Inputs

The differential analog inputs of the transmitter baseband amplifier I/Q inputs (TXBBI+, TXBBI-, TXBBQ+, TXBBQ-) have a differential impedance of $20k\Omega \parallel 1pF$. The inputs require an input common-mode voltage of 0.9V to 1.3V, which is provided by the DC-coupled I and Q DAC outputs of the accompanying baseband IC.

Transmitter Baseband Lowpass Filtering

The transmitter integrates lowpass filters that can be tuned to -3dB corner frequencies of 8MHz (11b), 11MHz (11g), 16.5MHz (turbo 1 mode), and 22.5MHz (turbo 2 mode) through programming bits D1:D0 in

Register 8 (A3:A0 = 1000) and bit D5:D3 in Register 7 (A3:A0 = 0111). The -3dB corner-frequency is tightly controlled on-chip and does not require user adjustment. Additionally, provisions are made to fine tune the -3dB corner frequency through bits D5:D3 in the Filter Programming register (A3:A0 = 0111). See Tables 8 and 9.

Table 7. RSSI Pin Truth Table

INPUT CONDITIONS			RSSI OUTPUT
A3:A0 = 1000, D9:D8	A3:A0 = 1000, D10	RXHP	
X	0	0	No signal
00	0	1	RSSI
01	0	1	Temperature sensor
10	0	1	Power detector (MAX2831)
00	1	X	RSSI
01	1	X	Temperature sensor
10	1	X	Power detector (MAX2831)

X = Don't care.

Table 8. Transmitter LPF Coarse -3dB Corner Frequency Settings in Register (A3:A0 = 1000)

BITS (D1:D0)	-3dB CORNER FREQUENCY (MHz)	MODE
00	8	11b
01	11	11g
10	16.5	Turbo 1
11	22.5	Turbo 2

Table 9. Transmitter LPF Fine -3dB Corner Frequency Adjustment in Register (A3:A0 = 0111)

BITS (D5:D3)	% ADJUSTMENT RELATIVE TO COARSE SETTING
000	90
001	95
010	100
011	105
100	110 (11g)
101	115
101-111	Not used

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Transmitter Variable-Gain Amplifier

The variable-gain amplifier of the transmitter provides 31dB of gain control range programmable in 0.5dB steps over the top 8dB of the gain control range and in 1dB steps below that. The transmitter gain can be programmed serially through the SPI interface by setting bits D5:D0 in Register 12 (A3:A0 = 1100) or in parallel through the digital logic gain-control pins B6:B1 (pins 3, 6, 8, 11, 14, 23, and 34, respectively). Set bit D10 = 0 in Register 9 (A3:A0 = 1001) to enable parallel programming, and set bit D10 = 1 to enable programming through the 3-wire serial interface. See Table 10 for the transmitter VGA gain-control settings.

Table 10. Transmitter VGA Gain-Control Settings

NUMBER	D5:D0 Or B6:B1	OUTPUT SIGNAL POWER
63	111111	Max
62	111110	Max - 0.5dB
61	111101	Max - 1.0dB
:	:	:
49	110001	Max - 7dB
48	110000	Max - 7.5dB
47	101111	Max - 8dB
46	101110	Max - 8dB
45	101101	Max - 9dB
44	101100	Max - 9dB
:	:	:
5	000101	Max - 29dB
4	000100	Max - 29dB
3	000011	Max - 30dB
2	000010	Max - 30dB
1	000001	Max - 31dB
0	000000	Max - 31dB

Power-Amplifier Driver Output Matching (MAX2832)

The PA driver of the MAX2832 has a 100Ω differential output with on-chip AC-coupling capacitors. Provide electrically symmetrical traces to present a balanced load to the PA driver output to help maintain driver linearity and RF common-mode rejection.

Power-Amplifier Bias, Enable Delay and Output Matching (MAX2831)

The MAX2831 integrates a 2-stage PA, providing +18.5dBm of output power at 5.6% EVM (54Mbps OFDM signal) in 802.11g mode while exceeding the 802.11g spectral mask requirements. The first and second stage PA bias currents are set through programming bits D2:D0 and bits D6:D3 in Register 10 (A3:A0 = 1010), respectively. An adjustable PA enable delay, relative to the transmitter enable (RXTX low-to-high transition), can be set from 200ns to 7μs through programming bits D13:D10 in Register 10 (A3:A0 = 1010).

The PA of the MAX2831 has a 100Ω differential output that is internally matched. The output has to be AC-coupled using two off-chip 1.5pF capacitors to a 100Ω:50Ω balun. Provide electrically symmetrical traces from the PA output to the balun to present a balanced load and to reduce out-of-band spurs.

Power Detector (MAX2831)

The MAX2831 integrates a voltage-peak detector at the PA output and provides an analog voltage proportional to PA output power. See the Power Detector Over Frequency and Power Detector Over Supply Voltage graphs in the *Typical Operating Characteristics*. Set bits D9:D8 = 10 in Register 8 (A3:A0 = 1000) to multiplex the power-detector analog output voltage to the RSSI output (pin 16).

Synthesizer Programming

The MAX2831/MAX2832 integrate a 20-bit sigma-delta fractional-N synthesizer, allowing the device to achieve excellent phase-noise performance (0.9° RMS from 10kHz to 10MHz), fast PLL settling times, and an RF frequency step-size of 20Hz. The synthesizer includes a divide-by-1 or a divide-by-2 reference frequency divider, an 8-bit integer portion main divider with a divisor range programmable from 64 to 255, and a 20-bit fractional portion main-divider. Bit D2 in Register 5 (A3:A0 = 0101) sets the reference oscillator divider ratio to 1 or 2. Bits D7:D0 in Register 3 (A3:A0 = 0011) set the integer portion of the main divider. The 20-bit fractional portion of the main-divider is split between two registers. The 14 MSBs of the fractional portion are set in Register 4 (A3:A0 = 0100), and the 6 LSBs of the fractional portion of the main divider are set in Register 3 (A3:A0 = 0011). See Tables 11 and 12.

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Calculating Integer and Fractional Divider Ratios

The desired integer and fractional divider ratios can be calculated by dividing the RF frequency (f_{RF}) by f_{COMP} . For nominal 802.11g/b operation, a 40MHz reference oscillator is divided by 2 to generate a 20MHz comparison frequency (f_{COMP}). The following method can be used when calculating divider ratios supporting various reference and comparison frequencies:

$$\text{LO Frequency Divider} = f_{RF} / f_{COMP} = 2437\text{MHz} / 20\text{MHz} = 121.85$$

$$\text{Integer Divider} = 121 (d) = 0111\ 1001 \text{ (binary)}$$

$$\text{Fractional Divider} = 0.85 \times (2^{20} - 1) = 891289 \text{ (decimal)} \\ = 1101\ 1001\ 1001\ 1001\ 1001$$

See Table 13 for integer and fractional divider ratios for 802.11g/b systems using a 20MHz comparison frequency.

Table 11. Integer Divider Register (A3:A0 = 0011)

BIT	RECOMMENDED	DESCRIPTION
D13:D8	00000	6 LSBs of 20-Bit Fractional Portion of Main Divider
D7:D0	01111001	8-Bit Integer Portion of Main Divider. Programmable from 64 to 255.

Table 12. Fractional Divider Register (A3:A0 = 0100)

BIT	RECOMMENDED	DESCRIPTION
D13:D0	11011001100110	14 MSBs of 20-Bit Fractional Portion of Main Divider

Table 13. IEEE 802.11g/b Divider-Ratio Programming Words

f_{RF} (MHz)	(f_{RF} / f_{COMP})	INTEGER DIVIDER	FRACTIONAL DIVIDER	
		A3:A0 = 0011, D7:D0	A3:A0 = 0100, D13:D0	A3:A0 = 0011, D13:D8
2412	120.6	0111 1000b	2666h	1Ah
2417	120.85	0111 1000b	3666h	1Ah
2422	121.1	0111 1001b	0666h	1Ah
2427	121.35	0111 1001b	1666h	1Ah
2432	121.6	0111 1001b	2666h	1Ah
2437	121.85	0111 1001b	3666h	1Ah
2442	122.1	0111 1010b	0666h	1Ah
2447	122.35	0111 1010b	1666h	1Ah
2452	122.6	0111 1010b	2666h	1Ah
2457	122.85	0111 1010b	3666h	1Ah
2462	123.1	0111 1011b	0666h	1Ah
2467	123.35	0111 1011b	1666h	1Ah
2472	123.6	0111 1011b	2666h	1Ah
2484	124.2	0111 1100b	0CCCh	33h

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Crystal Oscillator

The crystal oscillator has been optimized to work with low-cost crystals (e.g., Kyocera CX-3225SB). See Figure 1. The crystal oscillator frequency can be fine tuned through bits D6:D0 in Register 14 (A3:A0 = 1110), which control the value of C_{TUNE} from 0.5pF to 15.4pF in 0.12pF steps. See the Crystal-Oscillator Offset Frequency vs. Crystal-Oscillator Tuning Bits graph in the *Typical Operating Characteristics*. The crystal oscillator can be used as a buffer for an external reference frequency source. In this case, the reference signal is AC-coupled to the XTAL pin, and capacitors C1 and C2 are not connected. When used as a buffer, the XTAL input pin has to be AC-coupled. The XTAL pin has an input impedance of $5k\Omega \parallel 4pF$, (set D6:D0 = 0000000 in Register 14 A3:A0 = 1110).

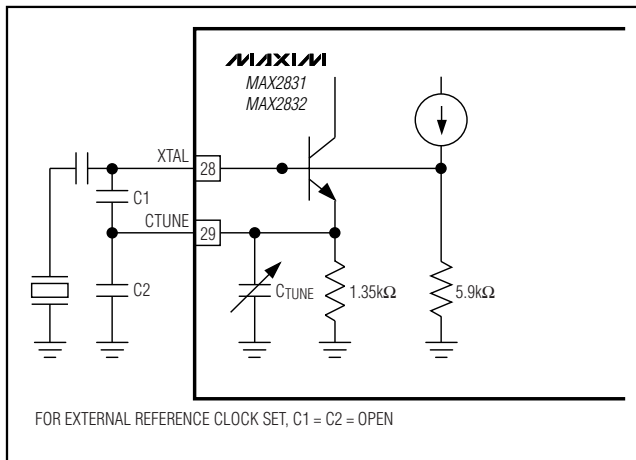


Figure 1. Crystal Oscillator Schematic

Reference Clock Output Divider/Buffer

The reference oscillator of the MAX2831/MAX2832 has a divider and a buffered output for routing the reference clock to the accompanying baseband IC. Bit D10 in Register 14 (A3:A0 = 1110) sets the buffer divider to divide by 1 or 2, independent of the divide ratio for the reference frequency provided to the PLL. Bit B9 in the same register enables or disables the reference buffer output. See the Clock Output waveform in the *Typical Operating Characteristics*.

Loop Filter

The PLL charge-pump output, CPOUT (pin 24), connects to an external third-order, lowpass RC loop-filter, which in turn connects to the voltage tuning input, TUNE (pin 32), of the VCO, completing the PLL loop. The charge-pump output sink and source current is 1mA, and the VCO tuning gain is 103MHz/V at 0.5V tune voltage and 86MHz/V at 2.2V tune voltage. The RC loop-filter values have been optimized for a loop bandwidth of 150kHz, to achieve the desired Tx/Rx turn-around settling time, while maintaining loop stability and good phase noise. Refer to the MAX2831 EV kit schematic for the recommended loop-filter component values. Keep the line from this pin to the tune input as short as possible to prevent spurious pickup.

Lock-Detector Output

The PLL features a logic lock-detect output. A logic-high indicates the PLL is locked, and a logic-low indicates the PLL is not locked. Bit D5 in Register 5 (A3:A0 = 0101) enables or disables the lock-detect output. Bit D12 in Register 1 (A3:A0 = 0001) configures the lock-detect output as a CMOS or open-drain output. In open-drain output mode, bit D9 in Register 5 (A3:A0 = 0101) enables or disables an internal 30kΩ pullup resistor from the open-drain output.

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Programmable Registers and 3-Wire SPI-Interface

The MAX2831/MAX2832 include 16 programmable, 18-bit registers. The 14 most significant bits (MSBs) are used for register data. The 4 least significant bits (LSBs) of each register contain the register address. See Table 14 for a summary of the registers and recommended register settings.

Register data is loaded through the 3-wire SPI/MICROWIRE™-compatible serial interface. Data is

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shifted in MSB first and is framed by \overline{CS} . When \overline{CS} is low, the clock is active, and data is shifted with the rising edge of the clock. When \overline{CS} transitions high, the shift register is latched into the register selected by the contents of the address bits. See Figure 2. Only the last 18 bits shifted into the device are retained in the shift register. No check is made on the number of clock pulses. For programming data words less than 14 bits long, only the required data bits and the address bits need to be shifted, resulting in faster Rx and Tx gain control where only the LSBs need to be programmed.

Table 14. Recommended Register Settings*

REGISTER	DATA														ADDRESS	TABLE
	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	(A3:A0)	
0	0	1	0	1	1	1	0	1	0	0	0	0	0	0	0000	15
1	0	1	0	0	0	1	1	0	0	1	1	0	1	0	0001	16
2	0	1	0	0	0	0	0	0	0	0	0	0	1	1	0010	17
3	0	0	0	0	0	0	0	1	1	1	1	0	0	1	0011	18
4	1	1	0	1	1	0	0	1	1	0	0	1	1	0	0100	19
5	0	0	0	0	0	0	1	0	1	0	0	1	0	0	0101	20
6	0	0	0	0	0	0	0	1	1	0	0	0	0	0	0110	21
7	0	1	0	0	0	0	0	0	1	0	0	0	1	0	0111	22
8	1	0	0	0	0	0	0	0	1	0	0	0	0	1	1000	23
9	0	0	0	0	1	1	1	0	1	1	0	1	0	1	1001	24
10	0	1	1	1	0	1	1	0	1	0	0	1	0	0	1010	25
11	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1011	26
12	0	0	0	0	0	1	0	1	0	0	0	0	0	0	1100	27
13	0	0	1	1	1	0	1	0	0	1	0	0	1	0	1101	28
14	0	0	0	0	1	1	0	0	1	1	1	0	1	1	1110	29
15	0	0	0	0	0	1	0	1	0	0	0	1	0	1	1111	30

*The power-on register settings are not production tested. Recommended register settings must be loaded after V_{CC} is supplied.

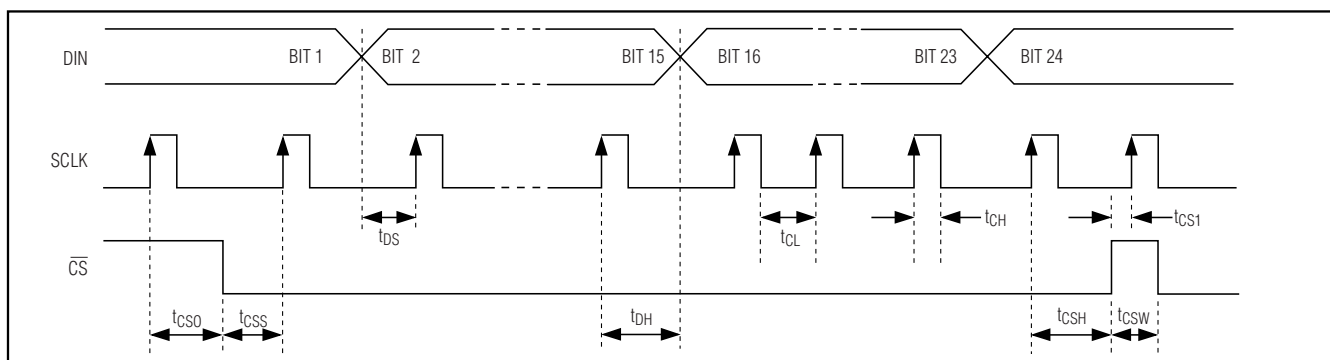


Figure 2. 3-Wire SPI Serial-Interface Timing Diagram

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Table 15. Register 0 (A3:A0 = 0000)

DATA BITS	RECOMMENDED	DESCRIPTION
D13:D11	000	Set to recommended value.
D10	1	Fractional-N PLL Mode Enable. Set 1 to enable the fractional-N PLL or set 0 to enable the integer-N PLL.
D9:D0	1101000000	Set to recommended value.

Table 16. Register 1 (A3:A0 = 0001)

DATA BITS	RECOMMENDED	DESCRIPTION
D13	0	Set to recommended value.
D12	1	Lock-Detector Output Select. Set to 1 for CMOS Output. Set to 0 for open-drain output. Bit D9 in register (A3:A0 = 0101) enables or disables an internal 30k Ω pullup resistor in open-drain output mode.
D11:D0	000110011010	Set to recommended value.

Table 17. Register 2 (A3:A0 = 0010)

DATA BITS	RECOMMENDED	DESCRIPTION
D13:D0	01000000000011	Set to recommended value.

This register contains the 8-bit integer portion and 6 LSBs of the fractional portion of the divider ratio of the synthesizer.

Table 18. Register 3 (A3:A0 = 0011)

BIT	RECOMMENDED	DESCRIPTION
D13:D8	00000	6 LSBs of 20-Bit Fractional Portion of Main Divider
D7:D0	01111001	8-Bit Integer Portion of Main Divider. Programmable from 64 to 255.

Table 19. Register 4 (A3:A0 = 0100)

BIT	RECOMMENDED	DESCRIPTION
D13:D0	11011001100110	14 MSBs of 20-Bit Fractional Portion of Main Divider

Table 20. Register 5 (A3:A0 = 0101)

BIT	RECOMMENDED	DESCRIPTION
D13:D10	0000	Set to recommended value.
D9	0	Lock-Detect Output Internal Pullup Resistor Enable. Set to 1 to enable internal 30k Ω pullup resistor or set to 0 to disable the resistor. Only available when lock-detect, open-drain output is selected (A3:A0 = 0010, D12 = 1).
D8:D6	010	Set to recommended value.
D5	1	Lock-Detect Output Enable. Set to 1 to enable the lock-detect output or set to 0 to disable the output. The output is high impedance when disabled.
D4:D3	00	Set to recommended value.
D2	1	Reference Frequency Divider Ratio to PLL. Set to 0 to divide by 1. Set to 1 to divide by 2.
D1:D0	00	Set to recommended value.

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Table 21. Register 6 (A3:A0 = 0110)

DATA BIT	RECOMMENDED	DESCRIPTION
D13	0	Set to recommended value.
D12:D11	00	Tx I/Q Calibration LO Leakage and Sideband Detector Gain-Control Bits. D12:D11 = 00: 9dB; 01 19dB; 10: 29dB; 11: 39dB.
D10:D7	0000	Set to recommended value.
D6	1	Power-Detector Enable in Tx Mode. Set to 1 to enable the power detector or set to 0 to disable the detector.
D5:D2	1000	Set to recommended value.
D1	0	Tx Calibration Mode. Set to 1 to place the device in Tx calibration mode or 0 to place the device in normal Tx mode when RXTX is set to 1 (see Table 31).
D0	0	Rx Calibration Mode. Set to 1 to place the device in Rx calibration mode or 0 to place the device in normal Rx mode when RXTX is set to 0 (see Table 31).

Table 22. Register 7 (A3:A0 = 0111)

BIT	RECOMMENDED	DESCRIPTION
D13:D12	01	Receiver Highpass Corner Frequency Setting for RXHP = 0. Set to 00 for 100Hz, X1 for 4kHz, and 10 for 30kHz.
D11:D6	000000	Set to recommended value.
D5:D3	100	Transmitter Lowpass Filter Corner Frequency Fine Adjustment (Relative to Coarse Setting). See Table 8. Bits D1:D0 in A3:A0 = 1000 provide the lowpass filter corner coarse adjustment.
D2:D0	010	Receiver Lowpass Filter Corner Frequency Fine Adjustment (Relative to Coarse Setting). See Table 5. Bits D1:D0 in A3:A0 = 1000 provide the lowpass filter corner coarse adjustment.

Table 23. Register 8 (A3:A0 = 1000)

BIT	RECOMMENDED	DESCRIPTION
D13	1	Set to recommended value.
D12	0	Enable Receiver Gain Programming Through the Serial Interface. Set to 1 to enable programming through the 3-wire serial interface (D6:D0 in Register A3:A0 = 1011). Set to 0 to enable programming in parallel through external digital pins (B7:B1).
D11	0	Set to recommended value.
D10	0	RSSI Operating Mode. Set to 1 to enable RSSI output independent of RXHP. Set to 0 to disable RSSI output if RXHP = 0, and enable the RSSI output if RXHP = 1.
D9:D8	00	RSSI, Power Detector or Temperature Sensor Output Select. Set to 00 to enable the RSSI output in receive mode. Set to 01 to enable the temperature sensor output in receive and transmit modes. Set to 10 to enable the power-detector output in transmit mode. See Table 7.
D7:D2	001000	Set to recommended value.
D1:D0	01	Receiver and Transmitter Lowpass Filter Corner Frequency Coarse Adjustment. See Tables 4 and 7.

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Table 24. Register 9 (A3:A0 = 1001)

BIT	RECOMMENDED	DESCRIPTION
D13:D11	000	Set to recommended value.
D10	0	Enable Transmitter Gain Programming Through the Serial or Parallel Interface. Set to 1 to enable programming through the 3-wire serial interface (D5:D0 in Register A3:A0 = 1011). Set to 0 to enable programming in parallel through external digital pins (B6:B1).
D9:D0	1110110101	Set to recommended value.

Table 25. Register 10 (A3:A0 = 1010)

BIT	RECOMMENDED	DESCRIPTION
D13:D10	0111	Power-Amplifier Enable Delay. Sets a delay between RXTX low-to-high transition and internal PA enable. Programmable in 0.5 μ s steps. D13:D10 = 0001 (0.2 μ s) and D13:D10 = 1111 (7 μ s).
D9:D7	011	Set to recommended value.
D6:D3	0100	Second-Stage Power-Amplifier Bias Current Adjustment. Set to XXXX for 802.11g/b.
D2:D0	100	First-Stage Power-Amplifier Bias Current Adjustment. Set to XXX for 802.11g/b.

Table 26. Register 11 (A3:A0 = 1011)

BIT	RECOMMENDED	DESCRIPTION
D13:D7	0000000	Set to recommended value.
D6:D5	11	LNA Gain Control. Set to 11 for high-gain mode. Set to 10 for medium-gain mode, reducing LNA gain by 16dB. Set to 0X for low-gain mode, reducing LNA gain by 33dB.
D4:D0	11111	Receiver VGA Control. Set D4:D0 = 00000 for minimum gain and D4:D0 = 11111 for maximum gain.

Table 27. Register 12 (A3:A0 = 1100)

BIT	RECOMMENDED	DESCRIPTION
D13:D6	00000101	Set to recommended value.
D5:D0	000000	Transmitter VGA Gain Control. Set D5:D0 = 000000 for minimum gain, and set D5:D0 = 111111 for maximum gain.

Table 28. Register 13 (A3:A0 = 1101)

BIT	RECOMMENDED	DESCRIPTION
D13:D10	0011	Set to recommended value.
D9:D6	1010	Set to recommended value.
D5:D0	010010	Set to recommended value.

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Table 29. Register 14 (A3:A0 = 1110)

BIT	RECOMMENDED	DESCRIPTION
D13:D11	000	Set to recommended value.
D10	0	Reference Clock Output Divider Ratio. Set 1 to divide by 2 or set 0 to divide by 1.
D9	1	Reference Clock Output Enable. Set 1 to enable the reference clock output or set 0 to disable.
D8:D7	10	Set to recommended value.
D6:D0	XXXXXX	Crystal-Oscillator Fine Tune. Tunes crystal oscillator over ± 20 ppm to within ± 1 ppm.

X = Don't care.

Table 30. Register 15 (A3:A0 = 1111)

BIT	RECOMMENDED	DESCRIPTION
D13:D12	00	Set to recommended value.
D11:D10	00	Receiver I/Q Output Common-Mode Voltage Adjustment. Set D11:D10 = 00: 1.1V, 01: 1.2V, 10: 1.3V, 11: 1.45V.
D9:D0	0101000101	Set to recommended value.

Table 31. Operating Mode Table

MODE	LOGIC PINS		REGISTER SETTINGS	CIRCUIT BLOCK STATES			
	$\overline{\text{SHDN}}$	RXTX	D1:D0 (A3:A0 = 0110)	Rx PATH	Tx PATH	PLL, VCO, LO GEN, AUTO-TUNER	CALIBRATION SECTIONS ON
Shutdown	0	0	00	Off	Off	Off	None
Standby	0	1	00	Off	Off	On	None
Rx	1	0	X0	On	Off	On	None
Tx	1	1	0X	Off	On	On	None
Rx Calibration	1	0	X1	On (except LNA)	Upconverters	On	Cal tone, RF phase shift, Tx filter
Tx Calibration	1	1	1X	Off	On (except PA driver and PA)	On	AM detector, Rx I/Q buffers

X = Don't care.

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Modes of Operation

The modes of operation for the MAX2831/MAX2832 are shutdown, standby, transmit, receive, transmitter calibration, and receiver calibration. See Table 31 for a summary of the modes of operation. The logic-input pins, SHDN (pin 12) and RXTX (pin 48), control the various modes.

Shutdown Mode

The MAX2831/MAX2832 feature a low-power shutdown mode that disables all circuit blocks, except the serial-interface and internal registers, allowing the registers to be loaded and values maintained, as long as V_{CC} is applied. Set SHDN and RXTX logic-low to place the device in shutdown mode.

After supply voltage ramp up, supply current in shutdown mode could be high. Program the default value to SPI register 0 to eliminate high shutdown current.

Standby Mode

The standby mode is used to enable the frequency synthesizer block while the rest of the device is powered down. In this mode, the PLL, VCO, and LO generators are on, so that Tx or Rx modes can be quickly enabled from this mode. Set SHDN to a logic-low and RXTX to a logic-high to place the device in standby mode.

Receive (Rx) Mode

The complete receive signal path is enabled in this mode. Set SHDN to logic-high and RXTX to logic-low to place the device in Rx mode.

Transmit (Tx) Mode

The complete transmitter signal path is enabled in this mode. Set SHDN and RXTX to logic-high to place the device in Tx mode.

Tx/Rx Calibration Mode

The MAX2831/MAX2832 feature Rx/Tx calibration modes to detect I/Q imbalances and transmit LO leakage. In the Tx calibration mode, all Tx circuit blocks, except the PA driver and external PA, are powered on and active. The AM detector and receiver I and Q channel buffers are also on, along with multiplexers in the receiver side to route this AM detector's signal. In this mode, the LO leakage calibration is done only for the LO leakage signal that is present at the center frequency of the channel (i.e., in the middle of the OFDM or QPSK spectrum). The LO leakage calibration includes the effect of all DC offsets in the entire baseband paths of the I/Q modulator and direct leakage of the LO to the I/Q modulator output.

The LO leakage and sideband detector output are taken at the receiver I and Q channel outputs during this calibration phase.

During Tx LO leakage and I/Q imbalance calibration, a sine and cosine signal ($f = f_{\text{TONE}}$) is input to the baseband I/Q Tx pins from the baseband IC. At the LO leakage and sideband-detector output, the LO leakage corresponds to the signal at f_{TONE} and the sideband suppression corresponds to the signal at $2 \times f_{\text{TONE}}$. The output power of these signals vary 1dB for 1dB of variation in the LO leakage and sideband suppression. To calibrate the Tx path, first set the power-detector gain to 9dB using D12:D11 in Register 5 (see Table 21). Adjust the DC offset of the baseband inputs to minimize the signal at f_{TONE} (LO leakage). Then, adjust the baseband input relative magnitude and phase offsets to reduce the signal at $2 \times f_{\text{TONE}}$.

In Rx calibration mode, the calibrated Tx RF signal is internally routed to the Rx inputs. In this mode, the VCO/LO generator/PLL blocks are powered on and active except for the low-noise amplifier (LNA).

Applications Information

Layout Issues

The MAX2831 EV kit can be used as a starting point for layout. For best performance, take into consideration grounding and RF, baseband, and power-supply routing. Make connections from vias to the ground plane as short as possible. Do not connect the device ground pin to the exposed paddle ground. Keep the buffered clock output trace as short as possible. Do not share the trace with the RF input layer, especially on or inter-layer or back side of the board. On the high-impedance ports, keep traces short to minimize shunt capacitance. EV kit Gerber files can be requested at www.maxim-ic.com.

Power-Supply Layout

To minimize coupling between different sections of the IC, a star power-supply routing configuration with a large decoupling capacitor at a central V_{CC} node is recommended. The V_{CC} traces branch out from this node, each going to a separate V_{CC} node in the circuit. Place a bypass capacitor as close as possible to each supply pin. This arrangement provides local decoupling at each V_{CC} pin. Use at least one via per bypass capacitor for a low-inductance ground connection. Do not share the capacitor ground vias with any other branch and the exposed paddle ground.

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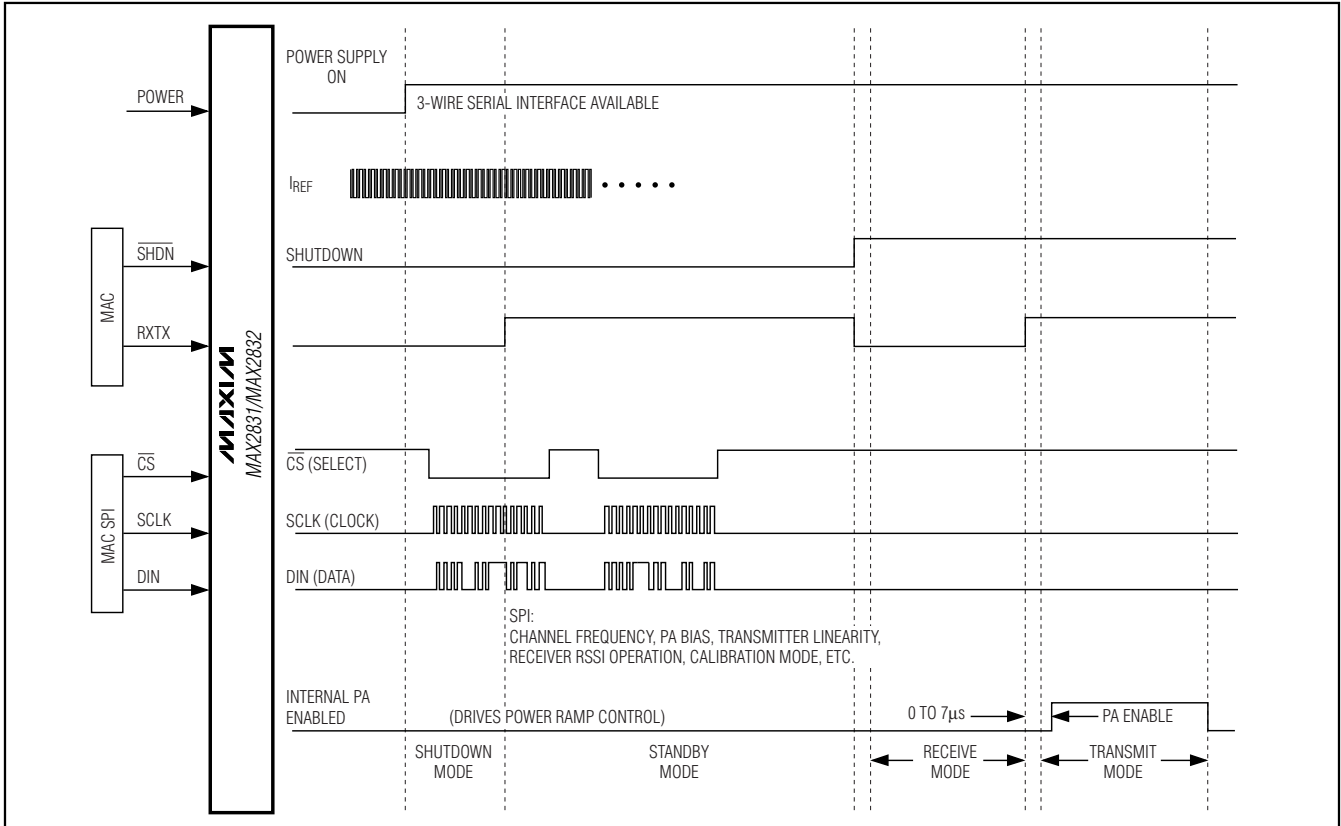
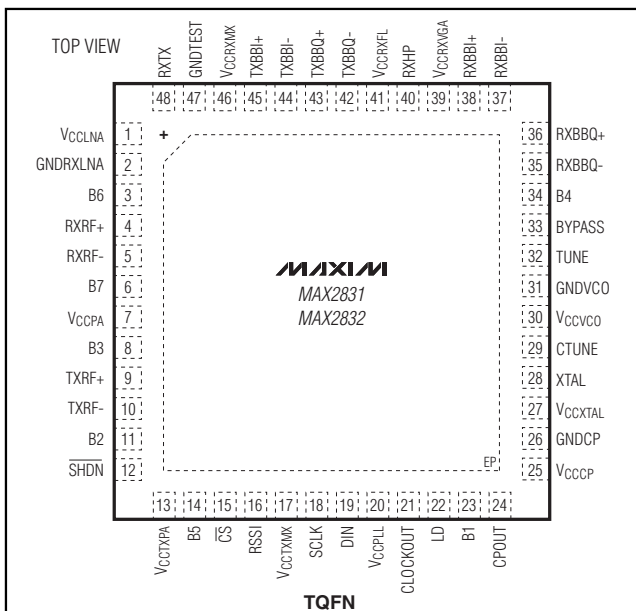


Figure 3. Timing Diagram

Pin Configuration



Chip Information

PROCESS: BiCMOS

Package Information

For the latest package outline information and land patterns (footprints), go to www.maxim-ic.com/packages. Note that a "+", "#", or "-" in the package code indicates RoHS status only. Package drawings may show a different suffix character, but the drawing pertains to the package regardless of RoHS status.

PACKAGE TYPE	PACKAGE CODE	OUTLINE NO.	LAND PATTERN NO.
48 TQFN-EP	T4877+4	21-0144	90-0130

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Revision History

REVISION NUMBER	REVISION DATE	DESCRIPTION	PAGES CHANGED
0	10/06	Initial release	—
1	3/10	Removed MAX2832 future product reference and made minor corrections	1, 2, 10, 18, 19, 20
2	3/11	Corrected conditions for Rx I/Q Output Common-Mode Voltage Variation in the <i>DC Electrical Characteristics</i> ; corrected Tables 14, 17, and 27; added text to <i>Shutdown Mode</i> section	2, 27, 28, 30, 32

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