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REVISION HISTORY

3/14—Rev. B to Rev. C

Added Exposed Pad Notation, Figure 2 and Table 3 ... 5
Updated Outline Dimensions ... 20
Changes to Ordering Guide ... 20

8/07—Rev. A to Rev B

Replaced Pin Configuration and Function Descriptions Section ... 5
Changes to Figure 30 ... 12
Changes to Figure 39 ... 18

7/07—Rev. 0 to Rev. A

Replaced Pin Configuration and Function Descriptions Section ... 5
Changes to Ordering Guide ... 20

6/04—Revision 0: Initial Version

SPECIFICATIONS

V_S = 5 V, T_A = 25°C, Z_O = 50 Ω, f = 880 MHz, single-ended, ac-coupled source drive to RFIP through 5.6 nH series inductor, RFIM ac-coupled through 5.6 nH series inductor to common, differential-to-single-ended conversion at output using 1:1 balun.

Table 1.

Parameter	Conditions	Min	Typ	Max	Unit
OVERALL FUNCTION					
Frequency Range		700		1000	MHz
Maximum Gain	Maximum gain setpoint for all phase setpoints		−2		dB
Minimum Gain	$V_{BBI} = V_{BBQ} = 0$ V		−32		dB
Gain Control Range	Relative to maximum gain		30		dB
Phase Control Range	Over 30 dB control range		360		Degrees
Gain Flatness	Over any 60 MHz bandwidth		0.25		dB
Group Delay Flatness	Over any 60 MHz bandwidth		10		ps
RF INPUT STAGE	RFIM, RFIP (Pin 21 and Pin 22)				
Input Return Loss	From RFIP to CMRF (with 5.6 nH series inductors)		20		dB
CARTESIAN CONTROL INTERFACE (I and Q)	IBBP, IBBM, QBBP, QBBM (Pin 16, Pin 15, Pin 3, Pin 4)				
Gain Scaling			2		1/V
Modulation Bandwidth	250 mV p-p sinusoidal baseband input single-ended		230		MHz
Second Harmonic Distortion	250 mV p-p, 1 MHz, sinusoidal baseband input differential		47		dBc
Third Harmonic Distortion	250 mV p-p, 1 MHz, sinusoidal baseband input differential		45		dBc
Step Response	For gain setpoint from 0.1 to 0.9 (V_{BBP} = 0.5 V, V_{BBM} = 0.55 V to 0.95 V)		45		ns
	For gain setpoint from 0.9 to 0.1 (V_{BBP} = 0.5 V, V_{BBM} = 0.95 V to 0.55 V)		47		ns
RF OUTPUT STAGE	RFOP, RFOM (Pin 9 and Pin 10)				
Output Return Loss	Measured through balun		7.5		dB
f = 880 MHz					
Gain	Maximum gain setpoint		−2		dB
Output Noise Floor	Maximum gain setpoint, no input		−149		dBm/Hz
	P_{IN} = 0 dBm, frequency offset = 20 MHz		−147		dBm/Hz
Output IP3	f1 = 880 MHz, f2 = 877.5 MHz, maximum gain setpoint		24		dBm
ACPR	IS-95, single carrier, P_{OUT} = 0 dBm, maximum gain, phase setpoint = 45°		62		dBc
Output 1 dB Compression Point	Maximum gain		11		dBm
POWER SUPPLY	VPS2 (Pin 5, Pin 6, Pin 14); RFOP, RFOM (Pin 9 and Pin 10)				
Positive Supply Voltage		4.75	5	5.25	V
Total Supply Current	Includes load current	110	130	150	mA
OUTPUT DISABLE	DSOP (Pin 13)				
Disable Threshold			2.5		V
Maximum Attenuation	DSOP = 5 V		40		dB
Enable Response Time	Delay following high-to-low transition until device meets full specifications		15		ns
Disable Response Time	Delay following low-to-high transition until device produces full attenuation		10		ns

ABSOLUTE MAXIMUM RATINGS

Table 2.

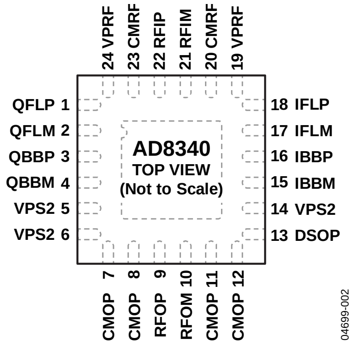
Parameter	Rating
Supply Voltage VPRF, VPS2	5.5 V
DSOP	5.5 V
IBBP, IBBM, QBBP, QBBM	2.5 V
RFOP, RFOM	5.5 V
RF Input Power at Maximum Gain (50 Ω)	13 dBm
(RFIP or RFIM, Single-Ended Drive)	
Equivalent Voltage	2.8 V p-p
Internal Power Dissipation	825 mW
θ_{JA} (with Pad Soldered to Board)	59°C/W
Maximum Junction Temperature	125°C
Operating Temperature Range	−40°C to +85°C
Storage Temperature Range	−65°C to +150°C
Lead Temperature (Soldering, 60 sec)	300°C

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS



NOTES
1. THE EXPOSED PAD MUST BE CONNECTED TO GROUND VIA A LOW IMPEDANCE PATH.

Figure 2. Pin Configuration

Table 3. Pin Function Descriptions

Pin No.	Mnemonic	Description
1; 2	QFLP; QFLM	Q Baseband Input Filter Pins. Connect optional capacitor to reduce Q baseband channel low-pass corner frequency.
3; 4	QBBP; QBBM	Q Channel Differential Baseband Inputs.
5, 6, 14; 19, 24	VPS2; VPRF	Positive Supply Voltage, 4.75 V to 5.25 V.
7, 8, 11, 12; 20, 23	CMOP; CMRF	Device Common. Connect via lowest possible impedance to external circuit common.
9; 10	RFOP; RFOM	Differential RF Outputs. Must be ac-coupled. Differential impedance 50 Ω nominal.
13	DSOP	Output Disable. Pull high to disable output stage.
15; 16	IBBM; IBBP	I Channel Differential Baseband Inputs.
17; 18	IFLM; IFLP	I Baseband Input Filter Pins. Connect optional capacitor to reduce I baseband channel low-pass corner frequency.
21; 22	RFIM; RFIP	Differential RF Inputs. Must be ac-coupled. Differential impedance 50 Ω nominal.
	EPAD	Exposed Pad. The exposed pad must be connected to ground via a low impedance path.

TYPICAL PERFORMANCE CHARACTERISTICS

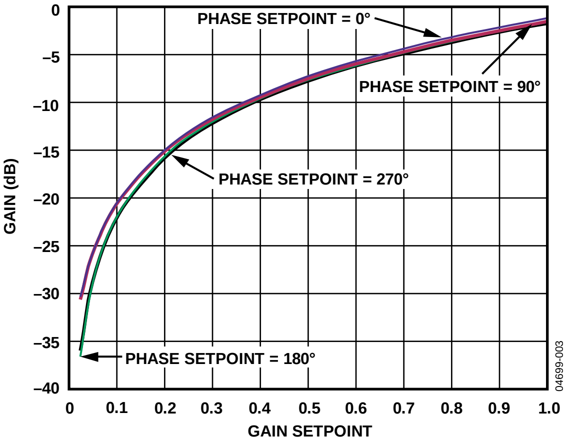


Figure 3. Gain Magnitude vs. Gain Setpoint at Different Phase Setpoints, RF Frequency = 880 MHz

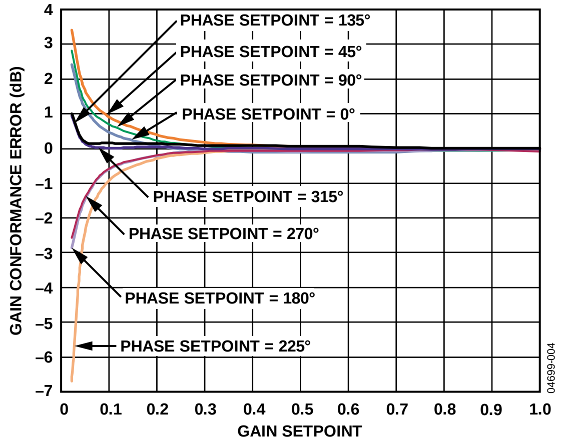


Figure 4. Gain Conformance Error vs. Gain Setpoint at Different Phase Setpoints

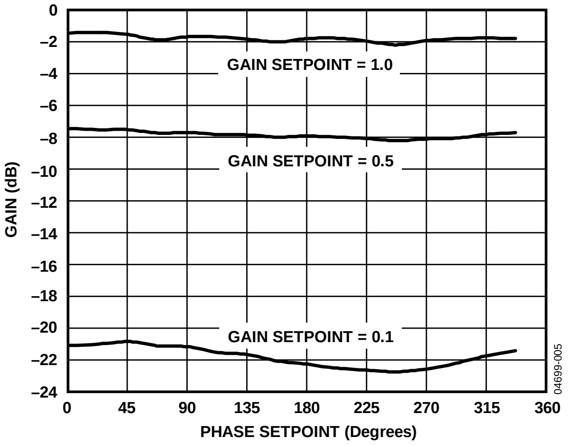


Figure 5. Gain Magnitude vs. Phase Setpoint at Different Gain Setpoints

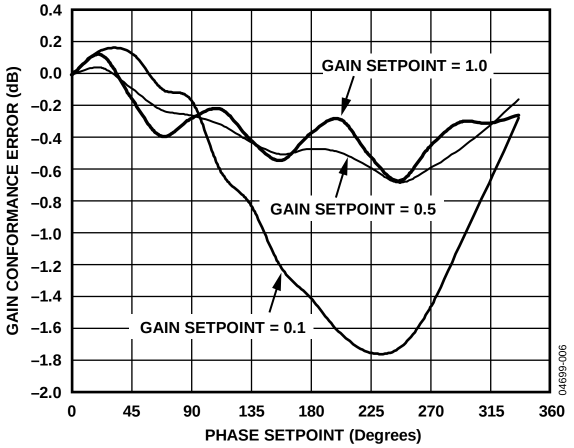


Figure 6. Gain Conformance Error vs. Phase Setpoint at Different Gain Setpoints

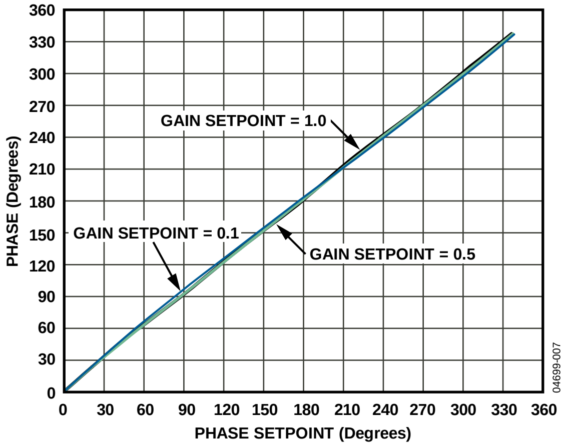


Figure 7. Phase vs. Phase Setpoint at Different Gain Setpoints

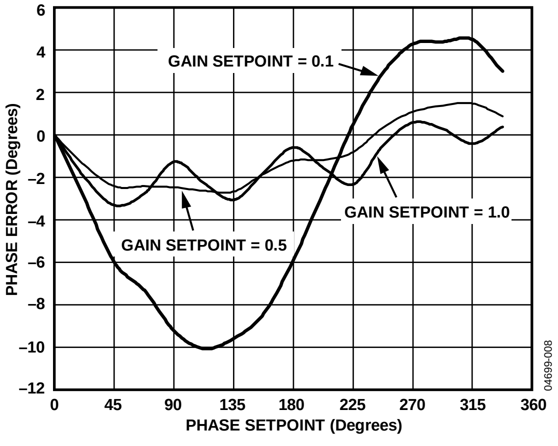


Figure 8. Phase Error vs. Phase Setpoint at Different Gain Setpoints

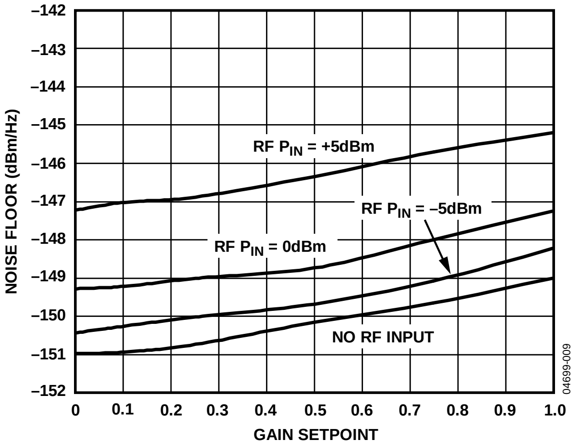


Figure 9. Output Noise Floor vs. Gain, Noise in dBm/Hz, No Carrier, With Carrier (20 MHz Offset) P_{IN} = –5 dBm, 0 dBm, and +5 dBm

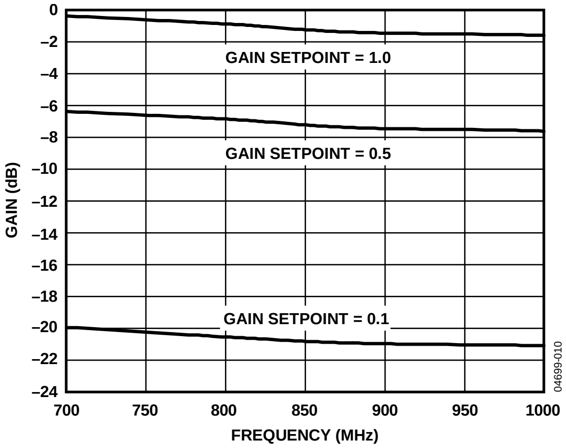


Figure 10. Gain vs. Frequency at Different Gain Setpoints (700 MHz to 1000 MHz), Phase Setpoint = 0°

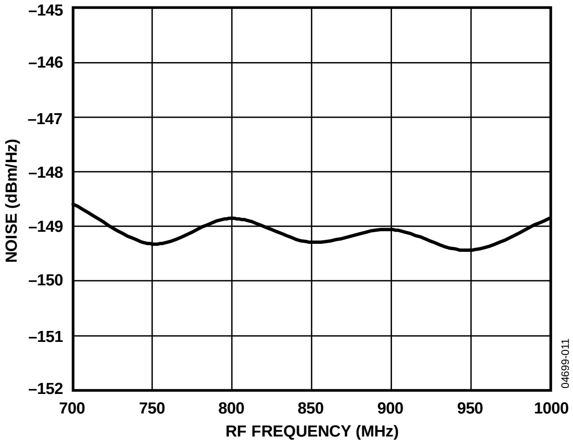


Figure 11. Output Noise Floor vs. Frequency, Maximum Gain, No RF Carrier, Phase Setpoint = 0°

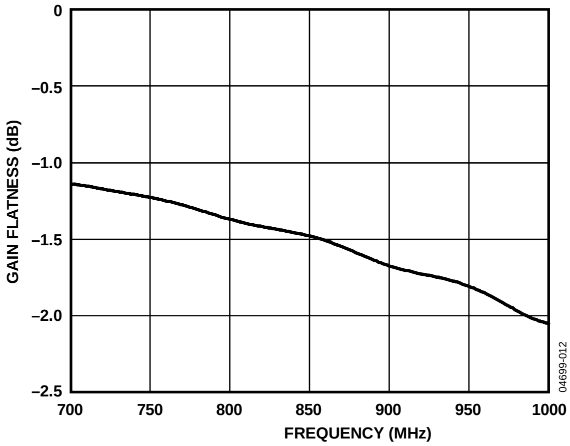


Figure 12. Gain Flatness vs. Frequency, Maximum Gain, Phase Setpoint = 0°

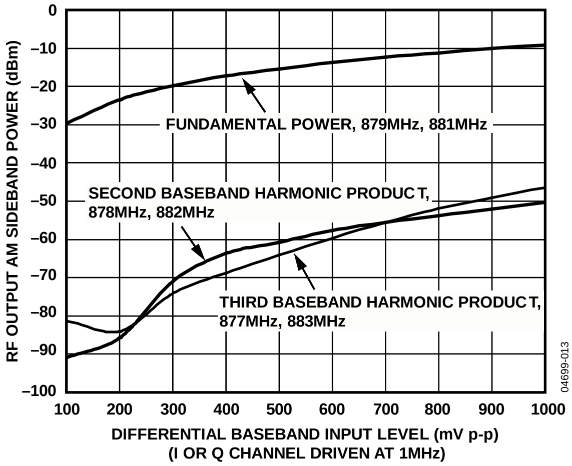


Figure 13. Baseband Harmonic Distortion (I and Q Channel, RF Input = 0 dBm, Balun and Cable Losses of Approximately 2 dB Not Accounted for in Plot)

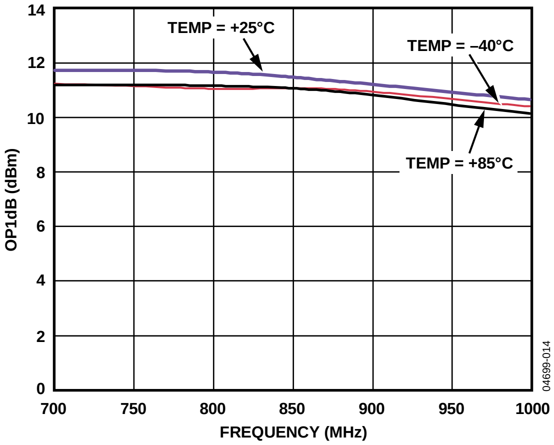


Figure 14. Output 1 dB Compression Point vs. Frequency and Temperature, Maximum Gain, Phase Setpoint = 0°

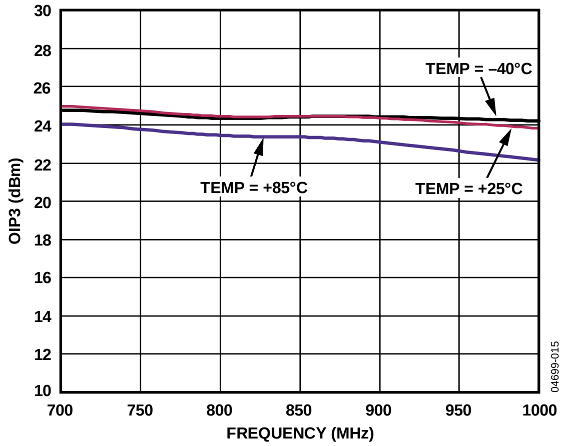


Figure 15. Output IP3 vs. Frequency and Temperature, Maximum Gain, I Only

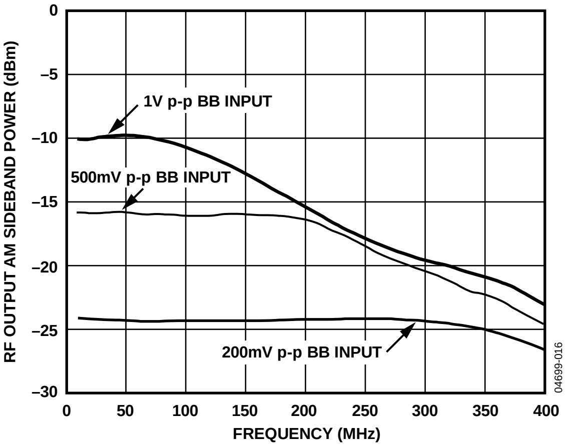


Figure 16. I/Q Modulation Bandwidth vs. Baseband Magnitude

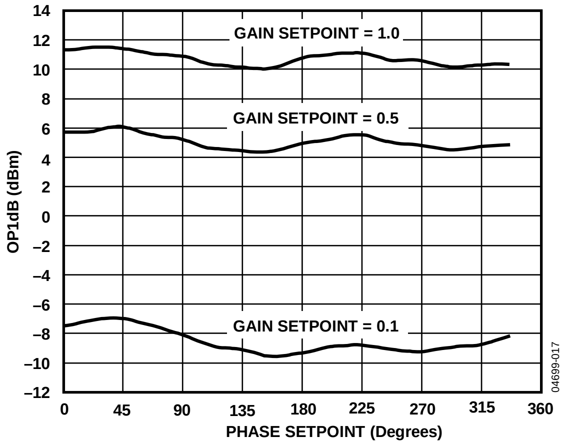


Figure 17. Output 1dB Compression Point vs. Gain and Phase Setpoints

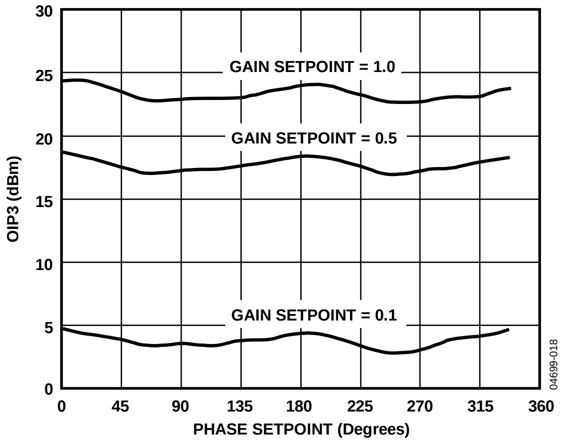


Figure 18. Output IP3 vs. Gain and Phase Setpoints, 2.5 MHz Carrier Spacing

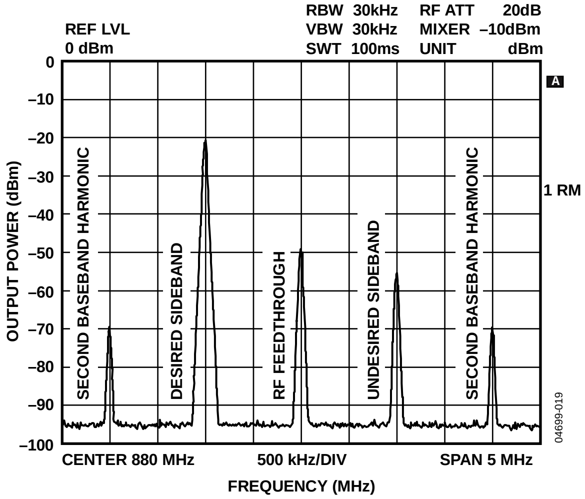


Figure 19. Single-Sideband Performance, 880 MHz, –10 dBm RF Input; 1 MHz, 500 mV p-p Differential BB Drive

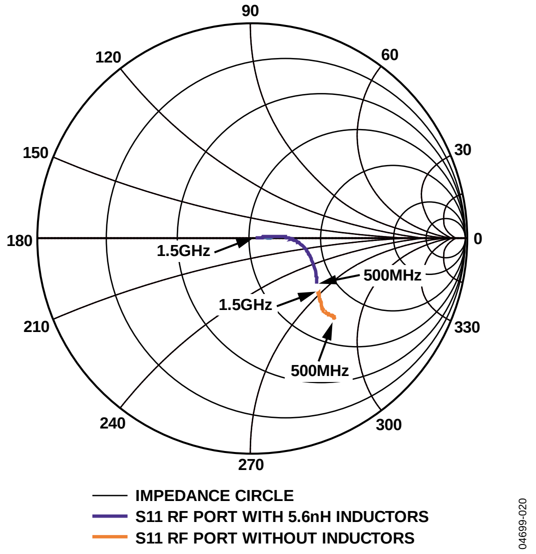


Figure 20. Input and Output Impedance Smith Chart (with Frequency Markers)

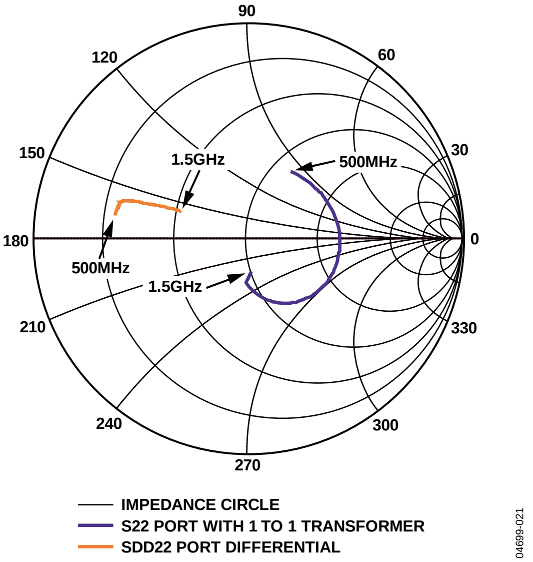


Figure 21. Output Impedance Smith Chart (with Frequency Markers)

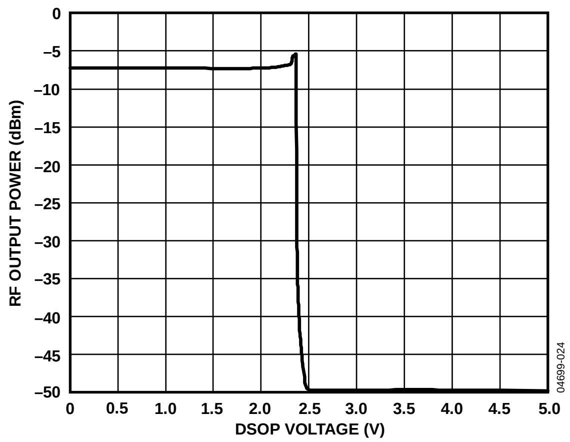


Figure 24. Power Shutdown Attenuation

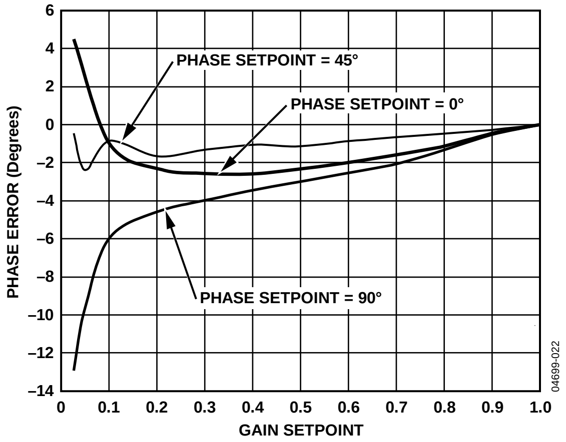


Figure 22. Phase Error vs. Gain Setpoint by Phase Setpoint, 5 V DC, 25°C, 880 MHz

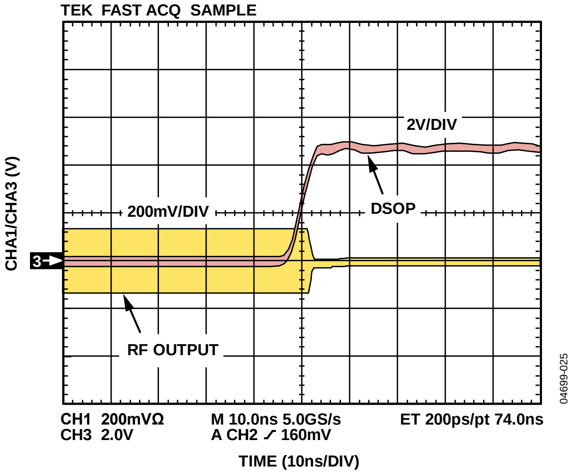


Figure 25. Power Shutdown Response Time

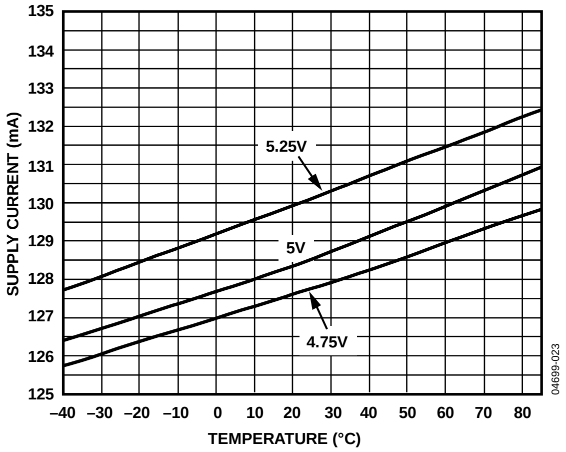


Figure 23. Supply Current vs. Temperature

THEORY OF OPERATION

The AD8340 is a linear RF vector modulator with Cartesian baseband controls. In the simplified block diagram shown in Figure 26, the RF signal propagates from the left to the right while baseband controls are placed above and below. The RF input is first split into in-phase (I) and quadrature (Q) components. The variable attenuators independently scale the I and Q components of the RF input. The attenuator outputs are then summed and buffered to the output.

By controlling the relative amounts of I and Q components that are summed, the AD8340 allows continuous magnitude and phase control of the gain. Consider the vector gain representation of the AD8340 expressed in polar form in Figure 27. The attenuation factors for the I and Q signal components are represented on the x- and y-axis, respectively, by the baseband inputs, V_{BBI} and V_{BBQ}. The resultant vector sum represents the vector gain, which can also be expressed as a magnitude and phase. By applying different combinations of baseband inputs, any vector gain within the unit circle can be programmed.

A change in sign of V_{BBI} or V_{BBQ} can be viewed as a change in sign of the gain or as a 180° phase change. The outermost circle represents the maximum gain magnitude of unity. The circle origin implies, in theory, a gain of 0. In practice, circuit mismatches and unavoidable signal feedthrough limit the minimum gain to approximately −40 dB. The phase angle between the resultant gain vector and the positive x-axis is defined as the phase shift. Note that there is a nominal, systematic insertion phase through the AD8340 to which the phase shift is added. In the following discussions, the systematic insertion phase is normalized to 0°.

The correspondence between the desired gain and phase setpoints, $Gain_{SP}$ and $Phase_{SP}$, and the Cartesian inputs, V_{BBI} and V_{BBQ}, is given by simple trigonometric identities.

$$Gain_{SP} = \sqrt{(V_{BBI}/V_O)^2 + (V_{BBQ}/V_O)^2}$$

$$Phase_{SP} = \arctan(V_{BBQ}/V_{BBI})$$

where:
V_O is the baseband scaling constant (500 mV).
V_{BBI} and V_{BBQ} are the differential I and Q baseband voltages, respectively.

Note that when evaluating the arctangent function, the proper phase quadrant must be selected. For example, if the principal value of the arctangent (known as the arctangent(x)) is used, Quadrant 2 and Quadrant 3 would be interpreted mistakenly as Quadrant 4 and Quadrant 1, respectively. In general, both V_{BBI} and V_{BBQ} are needed in concert to modulate the gain and the phase.

Pure amplitude modulation is represented by radial movement of the gain vector tip at a fixed angle, while pure phase modulation is represented by rotation of the tip around the circle at a fixed radius. Unlike traditional I-Q modulators, the AD8340 is designed to have a linear RF signal path from input to output. Traditional I-Q modulators provide a limited LO carrier path through which any amplitude information is removed.

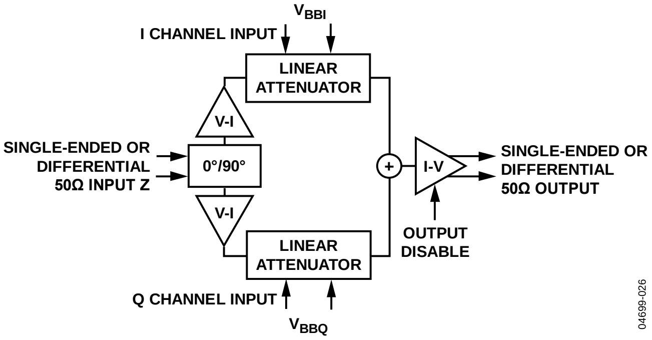


Figure 26. Simplified Architecture of the AD8340

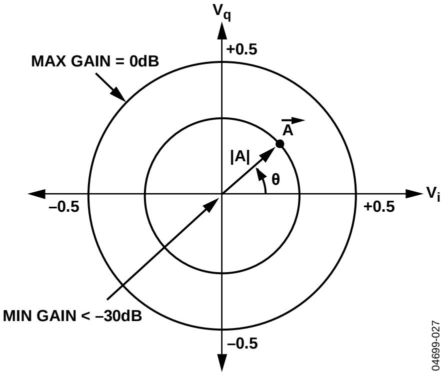


Figure 27. Vector Gain Representation

RF QUADRATURE GENERATOR

The RF input is directly coupled differentially or single-endedly to the quadrature generator, which consists of a multistage RC polyphase network tuned over the operating frequency range of 700 MHz to 1000 MHz. The recycling nature of the polyphase network generates two replicas of the input signal, which are in precise quadrature, that is, 90°, to each other. Because the passive network is perfectly linear, the amplitude and phase information contained in the RF input is transmitted faithfully to both channels. The quadrature outputs are then separately buffered to drive the respective attenuators. The characteristic impedance of the polyphase network is used to set the input impedance to the AD8340.

I-Q ATTENUATORS AND BASEBAND AMPLIFIERS

The proprietary linear-responding attenuator structure is an active solution with differential inputs and outputs that offer excellent linearity, low noise, and greater immunity from mismatches than other variable attenuator methods. The gain, in linear terms, of the I and Q channels is proportional to its control voltage with a scaling factor designed to be 2/V, that is, a full-scale gain setpoint of 1.0 (−2 dB) for $V_{BBI\,(Q)}$ of 500 mV. The control voltages can be driven differentially or single-endedly. The combination of the baseband amplifiers and attenuators allows for maximum modulation bandwidths in excess of 200 MHz.

OUTPUT AMPLIFIER

The output amplifier accepts the sum of the attenuator outputs and delivers a differential output signal into the external load. The output pins must be pulled up to an external supply, preferably through RF chokes. When the 50 Ω load is taken differentially, an OP1dB of 11 dBm and OIP3 of 24 dBm are achieved at 880 MHz. The output can be taken in single-ended fashion, albeit at lower performance levels.

NOISE AND DISTORTION

The output noise floor and distortion levels vary with the gain magnitude but do not vary significantly with the phase. At the higher gain magnitude setpoints, the OIP3 and the noise floor vary in direct proportion with the gain. At lower gain magnitude setpoints, the noise floor levels off while the OIP3 continues to vary with the gain.

GAIN AND PHASE ACCURACY

There are numerous ways to express the accuracy of the AD8340. Ideally, the gain and phase should precisely follow the setpoints. Figure 4 illustrates the gain error in decibels (dB) from a best fit line, normalized to the gain measured at the gain setpoint = 1.0, for the different phase setpoints. Figure 6 shows the gain error in a different form; the phase setpoint is swept from 0° to 360° for different gain setpoints. Figure 8 and Figure 22 show analogous errors for the phase error as a function of gain and phase setpoints. The accuracy clearly depends on the region of operation within the vector gain unit circle. Operation very close to the origin generally results in larger errors as the relative accuracy of the I and Q vectors degrades.

RF FREQUENCY RANGE

The frequency range on the RF input is limited by the internal polyphase quadrature phase-splitter. The phase-splitter splits the incoming RF input into two signals, 90° out of phase, as previously described in the RF Quadrature Generator section. This polyphase network has been designed to ensure robust quadrature accuracy over standard fabrication process parameter variations for the 700 MHz to 1 GHz specified RF frequency range. Using the AD8340 as a single-sideband modulator and measuring the resulting sideband suppression is a good gauge of how the quadrature accuracy is maintained over RF frequency. A typical plot of sideband suppression from 500 MHz to 1.5 GHz is shown in Figure 28. The level of sideband suppression degradation outside the 700 MHz to 1 GHz specified range is subject to manufacturing process variations.

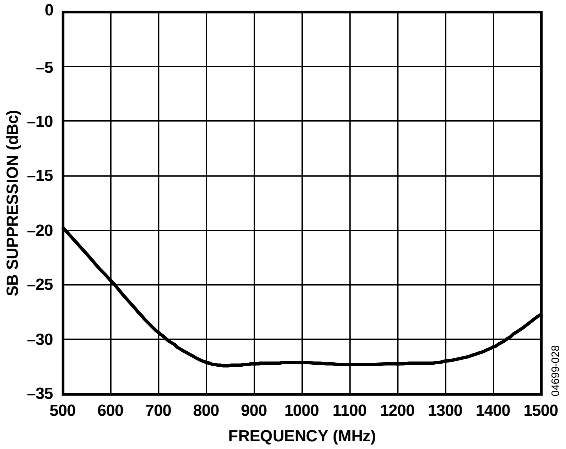


Figure 28. Sideband Suppression vs. Frequency

APPLICATIONS INFORMATION

USING THE AD8340

The AD8340 is designed to operate in a 50 Ω impedance system. Figure 30 illustrates where the RF input is driven in a single-ended fashion while the differential RF output is converted to a single-ended output with an RF balun. The baseband controls for the I and Q channels are typically driven from differential DAC outputs. The power supplies, VPRF and VPS2, should be bypassed appropriately with 0.1 µF and 100 pF capacitors. Low inductance grounding of the CMOP and CMRF common pins is essential to prevent unintentional peaking of the gain.

RF INPUT AND MATCHING

The input impedance of the AD8340 is defined by the characteristics of the polyphase network. The capacitive component of the network causes its impedance to roll off with frequency, albeit at a slower rate than 6 dB/octave. With matching inductors on the order of 5.6 nH in series with each of the RF inputs, RFIP and RFIM, a 50 Ω match is achieved with a return loss of >10 dB over the operating frequency range. Different matching inductors can improve matching over a narrower frequency range. The single-ended and differential input impedances are exactly the same.

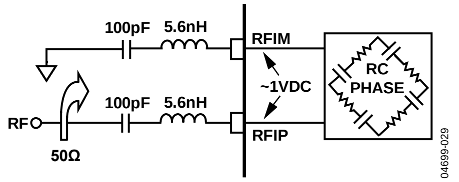


Figure 29. RF Input Interface to the AD8340 Showing Coupling Capacitors and Matching Inductors

The RFIP and RFIM should be ac-coupled through low loss series capacitors as shown in Figure 29. The internal dc levels are at approximately 1 V. For single-ended operation, one input is driven by the RF signal and the other input is ac grounded.

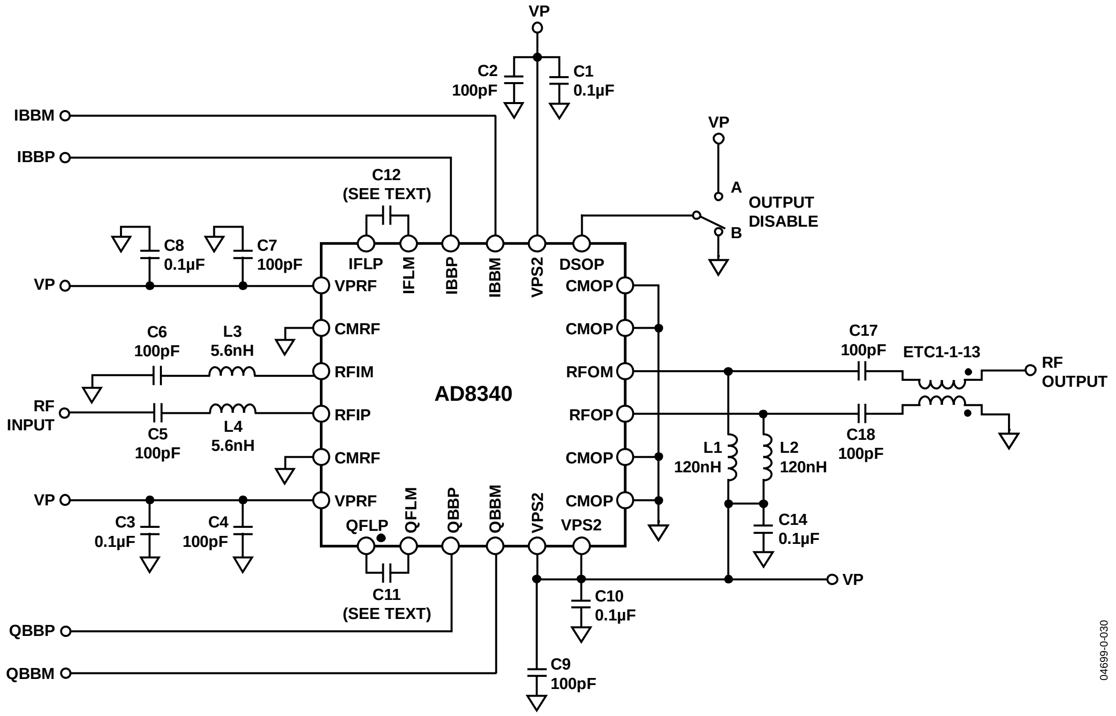


Figure 30. Basic Connections

RF OUTPUT AND MATCHING

The RF outputs of the AD8340, RFOP, and RFOM, are open collectors of a transimpedance amplifier that needs to be pulled up to the positive supply, preferably with RF chokes, as shown in Figure 31. The nominal output impedance looking into each individual output pin is 25 Ω. Consequently, the differential output impedance is 50 Ω.

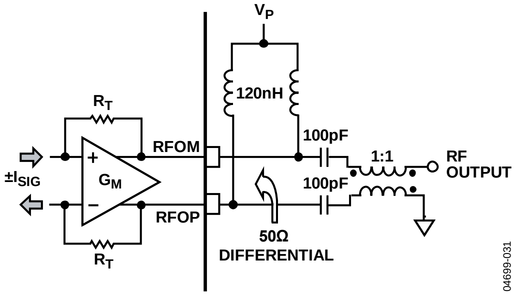


Figure 31. RF Output Interface to the AD8340 Showing Coupling Capacitors, Pull-Up RF Chokes, and Balun

Because the output dc levels are at the positive supply, ac coupling capacitors are usually needed between the AD8340 outputs and the next stage in the system.

A 1:1 RF broadband output balun, such as the ETC1-1-13 (M/A-COM), converts the differential output of the AD8340 into a single-ended signal. Note that the loss and balance of the balun directly impact the apparent output power, noise floor, and gain/phase errors of the AD8340. In critical applications, narrow-band baluns with low loss and superior balance are recommended.

If the output is taken in a single-ended fashion directly into a 50 Ω load through a coupling capacitor, there is an impedance mismatch. This can be resolved with a 1:2 balun to convert the single-ended 25 Ω output impedance to 50 Ω. If loss-of-signal swing is not critical, a 25 Ω back termination in series with the output pin can also be used. The unused output pin must still be pulled up to the positive supply. The user can load it through a coupling capacitor with a dummy load to preserve balance. The gain of the AD8340 when the output is single-ended varies slightly with the dummy load value, as shown in Figure 32.

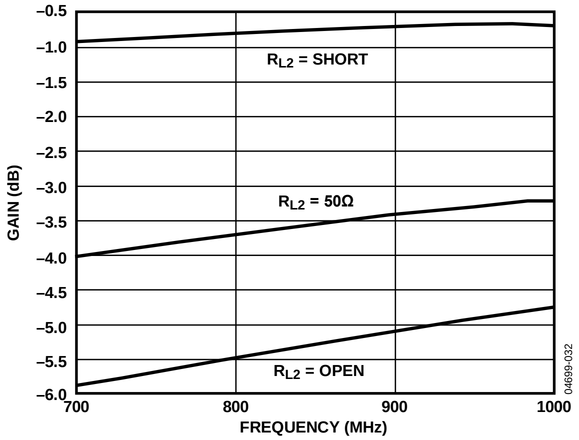


Figure 32. Gain of the AD8340 Using a Single-Ended Output with Different Dummy Loads, R_{L2} on the Unused Output

The RF output signal can be disabled by raising the DSOP pin to the positive supply. The shutdown function provides >40 dB attenuation of the input signal even at full gain. The interface to DSOP is high impedance, and the shutdown and turn-on response times are <100 ns. If the disable function is not needed, the DSOP should be tied to ground.

DRIVING THE I-Q BASEBAND CONTROLS

The I and Q inputs to the AD8340 set the gain and phase between input and output. These inputs are differential and should normally have a common-mode level of 0.5 V. However, when differentially driven, the common mode can vary from 250 mV to 750 mV while still allowing full gain control. Each input pair has a nominal input swing of ±0.5 V differential around the common-mode level. The maximum gain of unity is achieved if the differential voltage is equal to +500 mV or −500 mV. Therefore, with a common-mode level of 500 mV, IBBP and IBBM each swings between 250 mV and 750 mV.

The I and Q inputs can also be driven with a single-ended signal. In this case, one side of each input should be tied to a low noise 0.5 V voltage source (a 0.1 μF decoupling capacitor located close to the pin is recommended), while the other input swings from 0 V to 1 V. Differential drive generally offers superior even-order distortion and lower noise than single-ended drive.

The bandwidth of the baseband controls exceeds 200 MHz even at full-scale baseband drive. This allows for very fast gain and phase modulation of the RF input signal. In cases where lower modulation bandwidths are acceptable or desired, external filter capacitors can be connected across Pin IFLP to Pin IFLM, and across Pin QFLP to Pin QFLM, to reduce the ingress of baseband noise and spurious signal into the control path.

The 3 dB bandwidth is set by choosing C_{FLT} according to the following equation:

$$f_{3\,\text{dB}} \approx \frac{45\ \text{kHz} \times 10\ \text{nF}}{C_{EXTERNAL} + 0.5\ \text{pF}}$$

This equation has been verified for values of C_{FLT} from 10 pF to 0.1 μF (bandwidth settings of approximately 4.5 kHz to 43 MHz).

INTERFACING TO HIGH SPEED DACs

The AD977x family of dual DACs is well suited for driving the I and Q vector controls of the AD8340. While these inputs can in general be driven by any DAC, the differential outputs and bias level of the Analog Devices TxDAC® family allow for a direct connection between DAC and modulator.

The AD977x family of dual DACs has differential current outputs. The full-scale current is user programmable and is usually set to 20 mA, that is, each output swings from 0 mA to 20 mA.

The basic interface between the AD9777 DAC outputs and the AD8340 I and Q inputs is shown in Figure 33. The resistors R1 and R2 set the dc bias level according to the equation:

$$Bias\ Level = Average\ Output\ Current \times R1$$

For example, if the full-scale current from each output is 20 mA, each output will have an average current of 10 mA. Therefore, to set the bias level to the recommended 0.5 V, R1 and R2 should be set to 50 Ω each. R1 and R2 should always be equal.

If R3 is omitted, this results in an available swing from the DAC of 2 V p-p differential, which is twice the maximum voltage range required by the AD8340. DAC resolution can be maximized by adding R3, which scales down this voltage according to the following equation:

$$Full-Scale\ Swing =$$

$$2 \times I_{MAX}\left(R1 \| (R2 + R3)\right) \times \left(1 - \frac{R2}{R2 + R3}\right)$$

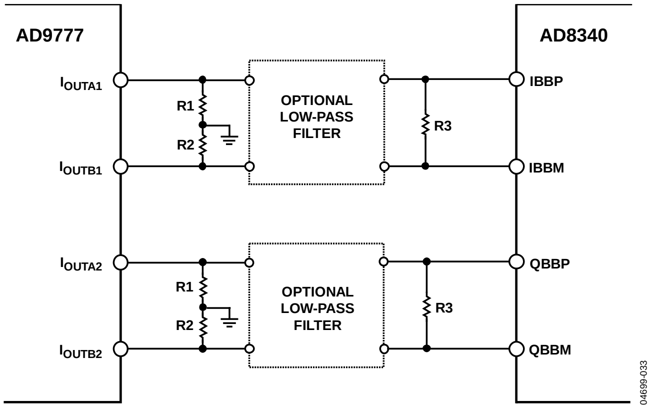


Figure 33. Basic AD9777 to AD8340 Interface

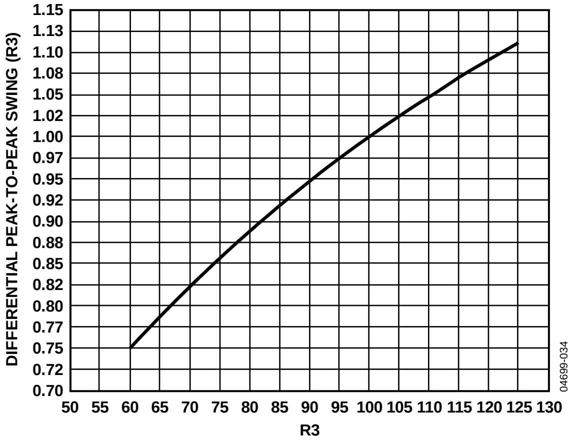


Figure 34. Peak-to-Peak DAC Output Swing vs. Swing Scaling Resistor R3 (R1 = R2 = 50 Ω)

Figure 34 shows the relationship between the value of R3 and the peak baseband voltage with R1 and R2 equal to 50 Ω. Figure 34 shows that a value of 100 Ω for R3 provides a peak-to-peak swing of 1 V p-p differential into the AD8340 I and Q inputs.

When using a DAC, low-pass image reject filters are typically used to eliminate the Nyquist images produced by the DAC. They also provide the added benefit of eliminating broadband noise that might feed into the modulator from the DAC.

CDMA2000 APPLICATION

To test the compliance to the CDMA2000 base station standard, a single-carrier CDMA2000 test model signal (forward pilot, sync, paging, and six traffic as per 3GPP2 C.S0010-B, Table 6.5.2.1) was applied to the AD8340. A cavity-tuned filter was used to reduce noise from the signal source being applied to the device. The 4.6 MHz pass band of this filter is apparent in the subsequent spectral plots (see Figure 35 to Figure 38).

Figure 35 shows a plot of the spectrum of the output signal under nominal conditions. P_{OUT} is equal to −5 dBm and $V_I = V_Q = 0.353$ V, that is, VIBBP − VIBBM = VQBBP − VQBBM = 0.353 V. Adjacent channel power is measured in 30 kHz resolution bandwidth at 750 kHz and 1.98 MHz carrier offset. Noise floor is measured at ±4 MHz carrier offset.

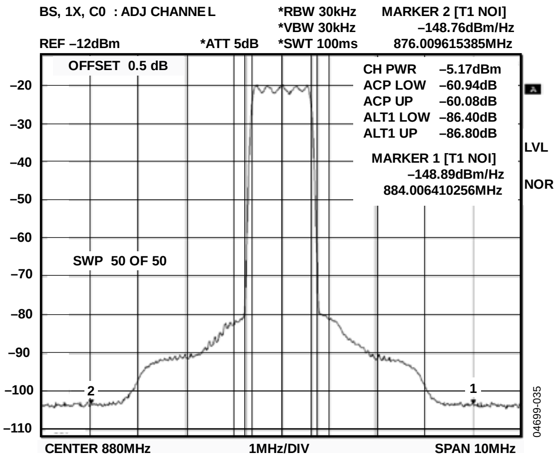


Figure 35. Output Spectrum, Single-Carrier CDMA2000 Test Model at –5 dBm $V_I = V_Q = 0.353$ V, ACP Measured at 750 kHz and 1.98 MHz Carrier Offset, Noise Measured at ±4 MHz Carrier Offset, Input Signal Filtered Using a Cavity Tuned Filter (Pass Band = 4.6 MHz)

Holding the I and Q control voltages steady at 0.353 V, input power was swept. Figure 36 shows the resulting output power, noise floor, and adjacent channel power ratio. Noise floor is presented as noise in a 1 MHz bandwidth as defined by the 3GPP2 specification.

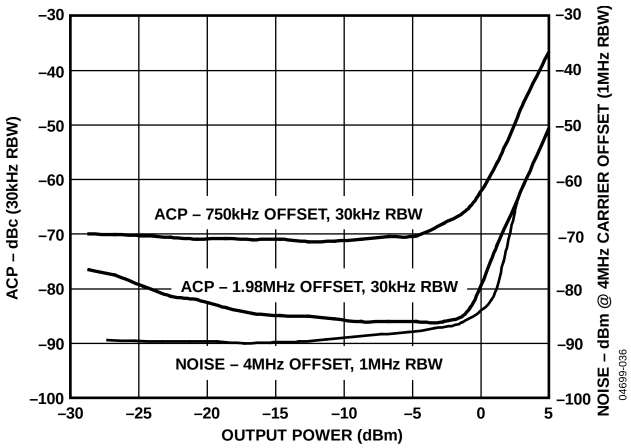


Figure 36. Noise and ACP vs. Output Power, Single-Carrier CDMA2000 Test Model, $V_I = V_Q = 0.353$, ACP Measured in 30 kHz RBW at ±750 kHz and ±1.98 MHz Carrier Offset, Noise Measured at ±4 MHz Carrier Offset

The results show that at an output power of 3 dBm, ACP is still in compliance with the standard (<–45 dBc at 750 MHz and <–60 dBc at 1.98 MHz). At low output power levels, ACP at 1.98 MHz, carrier offset degrades as the noise floor of the AD8340 becomes the dominant contributor to measured ACP. Measured noise at 4 MHz carrier offset begins to increase sharply above 0 dBm output power. This increase is not due to noise. but results from increased carrier-induced distortion. As output power drops below 0 dBm, the noise floor drops towards –90 dBm.

With a fixed input power of 2.4 dBm, the output power was again swept by exercising the I and Q inputs. V_I and V_Q were kept equal and were swept from 10 mV to 500 mV. The resulting output power, ACP, and noise floor are shown in Figure 37.

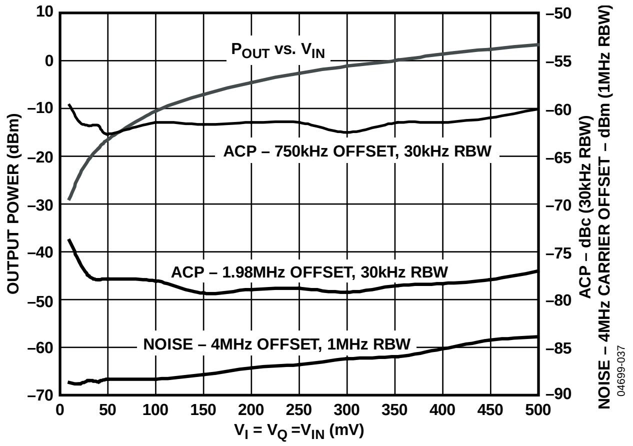


Figure 37. Output Power, Noise, and ACP vs. I and Q Control Voltages, CDMA2000 Test Model, $V_I = V_Q$, ACP Measured in 30 kHz RBW at ±750 kHz and ±1.98 MHz Carrier Offset, Noise Measured at ±4 MHz Carrier Offset

In contrast to Figure 36, Figure 37 shows that for a fixed input power, ACP remains fairly constant as gain and phase are changed (this is not true for very high input powers). The noise floor still drops with decreasing gain, but it never reaches the –90 dBm level shown in Figure 37.

Figure 38 shows the output spectrum for a 3-carrier CDMA2000 spectrum. Again, the signal being applied to the AD8340 is filtered by a cavity-tuned filter with a –3 dB bandwidth of 4.6 MHz. To reduce distortion, the total output carrier power was reduced to approximately –8 dBm (*per-carrier power* = –12.6 dBm). Adjacent channel power ratios of –61 dBc (2 MHz from center of spectrum) and –82 dBc (3.23 MHz from center of spectrum) were measured. The noise floor, measured at 5.25 MHz carrier offset, is approximately –149 dBm/Hz (–89 dBm in a 1 MHz bandwidth). While some dynamic range is lost due to output power back-off, ACP stays approximately equal and noise floor improves slightly.

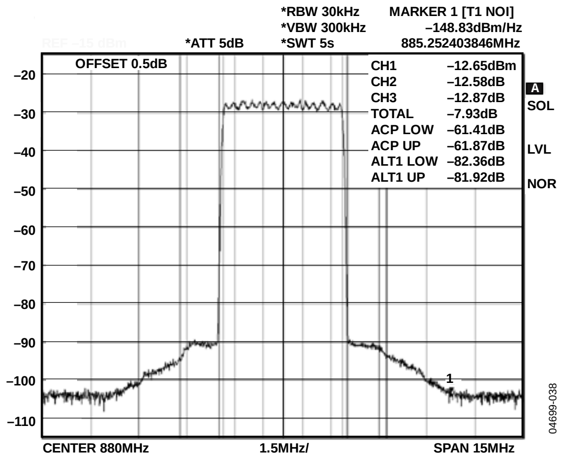


Figure 38. Output Spectrum, 3-Carrier CDMA2000 Test Model at –12.5 dBm/Carrier, $V_I = V_Q = 0.353$ V, ACP Measured at 2 MHz and 3.23 kHz Offset from Center of Spectrum, Noise Measured at 5.25 MHz Carrier Offset, Input Signal Filtered Using a Cavity-Tuned Filter (Pass Band = 4.6 MHz)

EVALUATION BOARD

The evaluation board circuit schematic for the AD8340 is shown in Figure 39.

The evaluation board is configured to be driven from a single-ended 50 Ω source. Although the input of the AD8340 is differential, it may be driven single-ended with no loss of performance.

The low-pass corner frequency of the baseband I and Q channels can be reduced by installing capacitors in the C11 and C12 positions. The low-pass corner frequency for either channel is approximated by

$$f_{3\,\mathrm{dB}} \approx \frac{45\ \mathrm{kHz} \times 10\ \mathrm{nF}}{C_{EXTERNAL} + 0.5\ \mathrm{pF}}$$

On the evaluation board, the I and Q baseband circuits are identical, so the following description applies equally to each. The connections and circuit configuration for the Q baseband inputs are described in Table 4.

The baseband input of the AD8340 requires a differential voltage drive. The evaluation board is set up to allow such a drive by connecting the differential voltage source to QBBP and QBBM. The common-mode voltage should be maintained at approximately 0.5 V. For this configuration, Jumper W1 to Jumper W4 should be removed.

The baseband input of the evaluation board can also be driven with a single-ended voltage. In this case, a bias level is provided to the unused input from Potentiometer R10 by installing either W1 or W2.

Setting SW1 in Position B disables the AD8340 output amplifier. With SW1 set to Position A, the output amplifier is enabled and an external voltage signal, such as a pulse, can be applied to the DSOP SMA connector to exercise the output amplifier enable/disable function.

Table 4. Evaluation Board Configuration Options

Components	Description	Default Conditions
R7, R9, R11, R14, R15, R19, R20, R21, C15, C19, W3, W4	I Channel Baseband Interface. Resistor R7 and Resistor R9 can be installed to accommodate a baseband source that requires a specific terminating impedance. C15 and C19 are bypass capacitors. For single-ended baseband drive, Potentiometer R11 can be used to provide a bias level to the unused input (install either W3 or W4).	R7, R9 = open R11 = potentiometer, 2 kΩ, 10 turns (Bourns) R14 = 4 kΩ (Size 0603) R15 = 44 kΩ (Size 0603) R19, R20, R21 = 0 Ω (Size 0603) C15, C19 = 0.1 μF (Size 0603) W3 = jumper (installed) W4 = jumper (open)
R1, R3, R10, R12, R13, R16, R17, R18, C16, C20, W1, W2	Q Channel Baseband Interface. See the I Channel Baseband Interface description.	R1, R3 = open R10 = potentiometer, 2 kΩ, 10 turns (Bourns) R12 = 4 kΩ (Size 0603) R13 = 44 kΩ (Size 0603) R16, R17, R18 = 0 Ω (Size 0603) C16, C20 = 0.1 μF (Size 0603) W1 = jumper (installed) W2 = jumper (open)
C11, C12	Baseband Low-Pass Filtering. By adding Capacitor C11 between QFLP and QFLM, and Capacitor C12 between IFLP and IFLM, the 3 dB low-pass corner frequency of the baseband interface can be reduced from 230 MHz (nominal). See the equation in the Evaluation Board section.	C11, C12 = open
T1, C17, C18, L1, L2	Output Interface. The 1:1 balun transformer, T1, converts the 50 Ω differential output to 50 Ω single-ended. C17 and C18 are dc blocks. L1 and L2 provide dc bias for the output.	C17, C18 = 100 pF (Size 0603) T1 = ETC1-1-13 (M/A-COM) L1, L2 = 120 nH (Size 0603)
L3, L4, C5, C6	Input Interface. The input impedance of the AD8340 requires 5.6 nH inductors in series with RFIP and RFIM for optimum return loss when driven by a single-ended 50 Ω line. C5 and C6 are dc blocks.	L3, L4 = 5.6 nH (Size 0402) C5, C6 = 100 pF (Size 0603)
C2, C4, C7, C9, C14, C1, C3, C8, C10, R2, R4, R5, R6	Supply Decoupling.	C2, C4, C7, C9 = open (Size 0603) C1, C3, C8, C10, C14 = 0.1 μF (Size 0603) R2, R4, R5, R6 = 0 Ω (Size 0603)
R8, SW1	Output Disable Interface. The output stage of the AD8340 is disabled by applying a high voltage to the DSOP pin by moving SW1 to Position B. The output stage is enabled by moving SW1 to Position A. The output disable function can also be exercised by applying an external high or low voltage to the DSOP SMA connector with SW1 in Position A.	R8 = 10 kΩ (Size 0603) SW1 = SPDT (Position A, output enabled)

SCHEMATIC AND ARTWORK

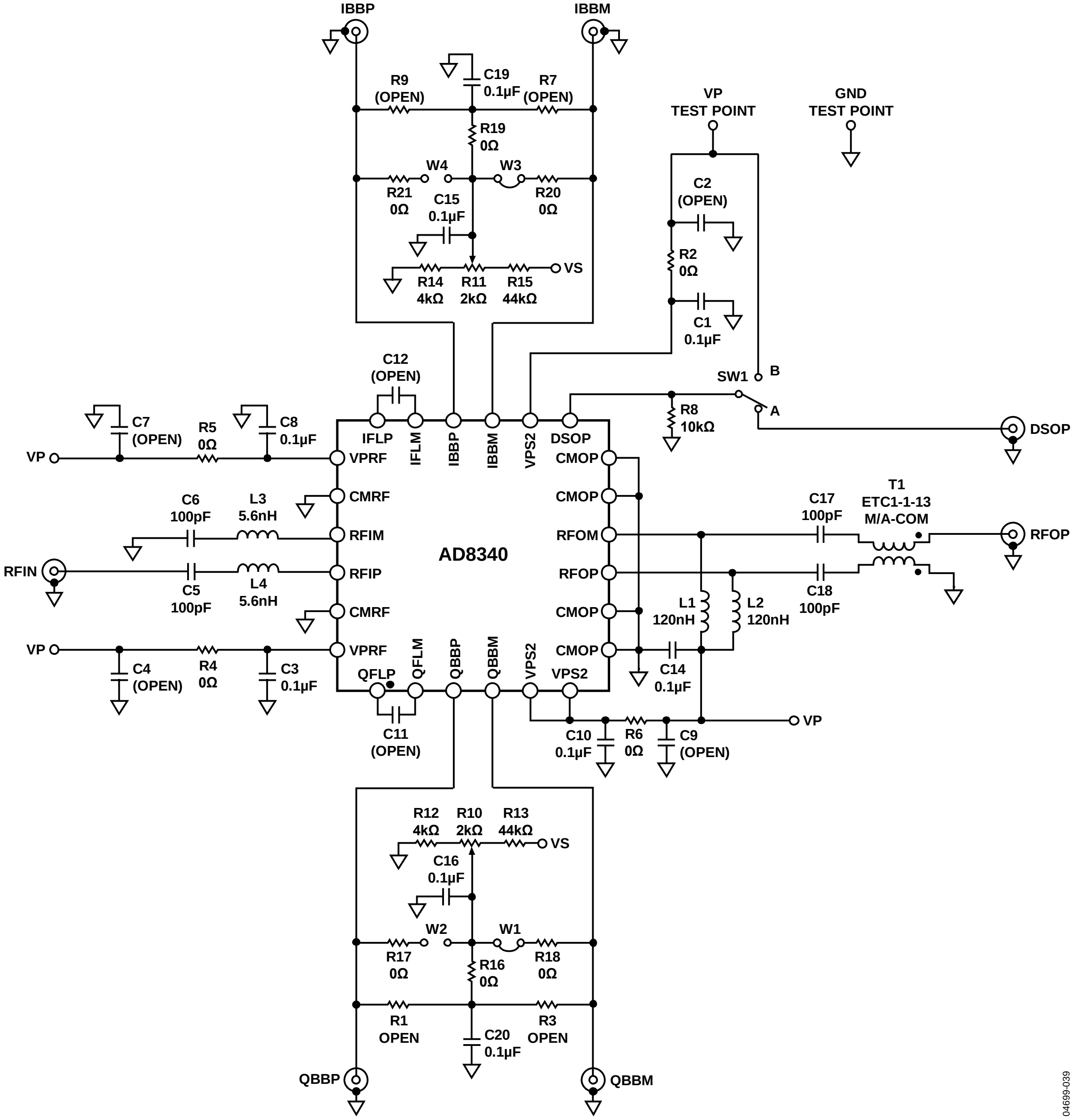


Figure 39. Evaluation Board Schematic

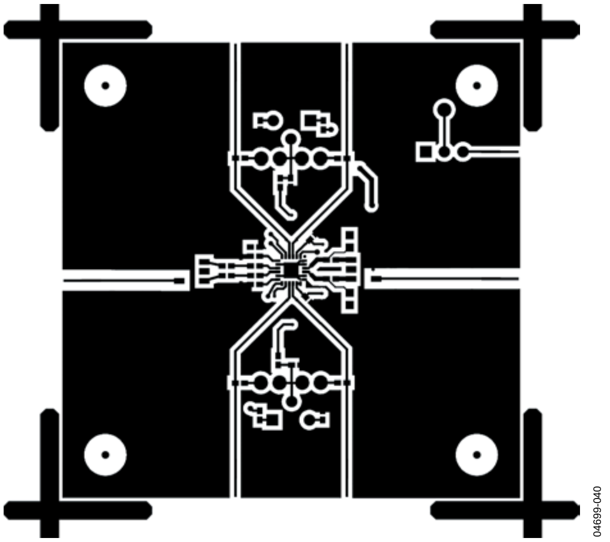


Figure 40. Component Side Layout

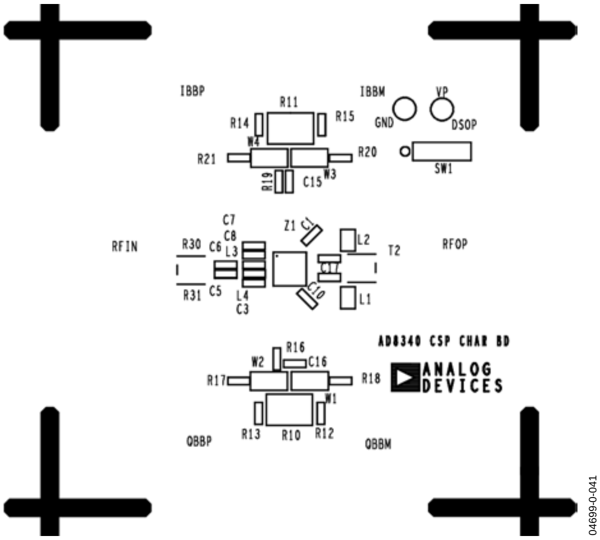


Figure 41. Component Side Silkscreen

OUTLINE DIMENSIONS

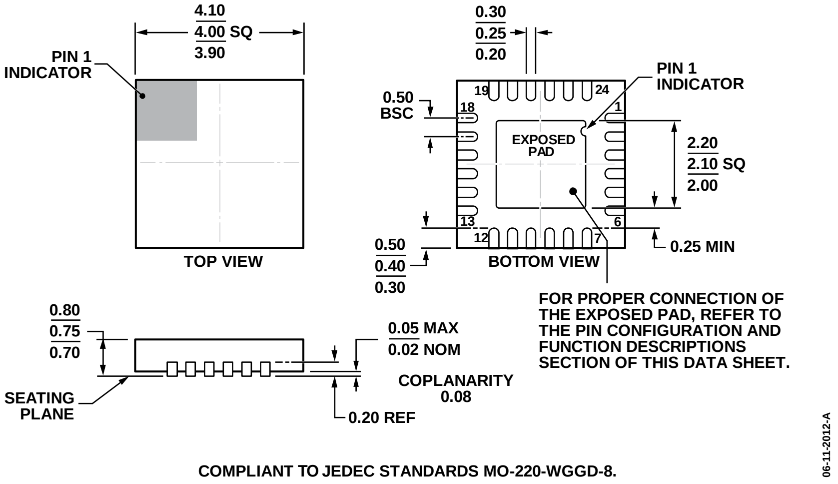


Figure 42. 24-Lead Lead Frame Chip Scale Package [LFCSP_WQ]
4 mm × 4 mm Body, Very Very Thin Quad
(CP-24-10)
Dimensions shown in millimeters

ORDERING GUIDE

Model[1, 2]	Temperature Range	Package Description	Package Option	Ordering Quantity
AD8340ACPZ-WP	−40°C to +85°C	24-Lead Lead Frame Chip Scale Package [LFCSP_WQ]	CP-24-10	64
AD8340ACPZ-REEL7	−40°C to +85°C	24-Lead Lead Frame Chip Scale Package [LFCSP_WQ]	CP-24-10	1,500
AD8340-EVALZ		Evaluation Board		1

[1] Z = RoHS Compliant Part.
[2] WP = Waffle pack.