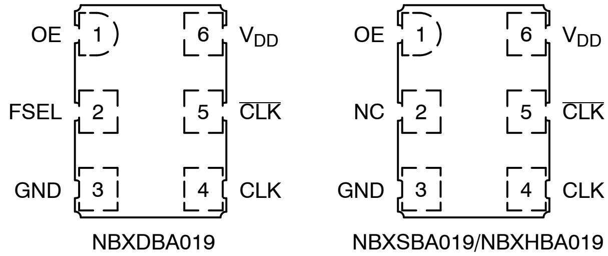


Figure 2. Pin Connections (Top View)

Table 1. PIN DESCRIPTION

Pin No.	Symbol	I/O	Description
1	OE	LVTTL/LVCMOS Control Input	Output Enable Pin. When left floating pin defaults to logic HIGH and output is active. See OE pin description Table 2.
2	FSEL/ NC*	LVTTL/LVCMOS Control Input	Output Frequency Select Pin. Pin will default to logic HIGH when left open. See Output Frequency Select pin description Table 3.
3	GND	Power Supply	Ground 0 V
4	CLK	LVPECL Output	Non−Inverted Clock Output. Typically loaded with 50 Ω receiver termination resistor to $V_{TT} = V_{DD} - 2$ V.
5	$\overline{CLK}$	LVPECL Output	Inverted Clock Output. Typically loaded with 50 Ω receiver termination resistor to $V_{TT} = V_{DD} - 2$ V.
6	V_{DD}	Power Supply	Positive power supply voltage. Voltage should not exceed 3.3 V ±10%.

*NBXSBA019 and NBXHBA019 only.

Table 2. OUTPUT ENABLE TRI−STATE FUNCTION

OE Pin	Output Pins
Open	Active
HIGH Level	Active
LOW Level	High Z

Table 3. OUTPUT FREQUENCY SELECT

FSEL Pin	Output Frequency (MHz)
Open (pin will float high)	125
HIGH Level	125
LOW Level	250

Table 4. ATTRIBUTES

Characteristic		Value
Input Default State Resistor		170 kΩ
ESD Protection	Human Body Model Machine Model	2 kV 200 V
Meets or Exceeds JEDEC Standard EIA/JESD78 IC Latchup Test		

1. For additional Moisture Sensitivity information, refer to Application Note AND8003/D.

Table 5. MAXIMUM RATINGS

Symbol	Parameter	Condition 1	Condition 2	Rating	Units
V_{DD}	Positive Power Supply	GND = 0 V		4.6	V
I_{out}	LVPECL Output Current	Continuous Surge		25 50	mA
T_A	Operating Temperature Range			−40 to +85	°C
T_{stg}	Storage Temperature Range			−55 to +120	°C
T_{sol}	Wave Solder	See Figure 6		260	°C

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

Table 6. DC CHARACTERISTICS (V_{DD} = 3.3 V ± 10%, GND = 0 V, T_A = −40°C to +85°C) (Note 2)

Symbol	Characteristic	Conditions	Min.	Typ.	Max.	Units
I_{DD}	Power Supply Current			78	100	mA
V_{IH}	OE and FSEL Input HIGH Voltage		2000		V_{DD}	mV
V_{IL}	OE and FSEL Input LOW Voltage		GND − 300		800	mV
I_{IH}	Input HIGH Current OE FSEL		−100 −100		+100 +100	μA
I_{IL}	Input LOW Current OE FSEL		−100 −100		+100 +100	μA
V_{OH}	Output HIGH Voltage	 V_{DD} = 3.3 V	V_{DD}−1195 2105		V_{DD}−945 2355	mV
V_{OL}	Output LOW Voltage	 V_{DD} = 3.3 V	V_{DD}−1945 1355		V_{DD}−1600 1700	mV
V_{OUTPP}	Output Voltage Amplitude			660		mV

NOTE: Device will meet the specifications after thermal equilibrium has been established when mounted in a test socket or printed circuit board with maintained transverse airflow greater than 500 lfpm. Electrical parameters are guaranteed only over the declared operating temperature range. Functional operation of the device exceeding these conditions is not implied. Device specification limit values are applied individually under normal operating conditions and not valid simultaneously.

2. Measurement taken with outputs terminated with 50 ohm to V_{DD}−2 V. See Figure 5.

Table 7. AC CHARACTERISTICS (V_{DD} = 3.3 V ± 10%, GND = 0 V, T_A = −40°C to +85°C) (Note 3)

Symbol	Characteristic	Conditions	Min.	Typ.	Max.	Units
f_{CLKOUT}	Output Clock Frequency	FSEL = HIGH		125		MHz
		FSEL = LOW		250		
Δf	Frequency Stability − NBXDBA019/NBXSBA019/NBXHBA019	(Note 4)			±50	ppm
Φ_{NOISE}	Phase−Noise Performance	100 Hz of Carrier		−112/−105		dBc/Hz
	f_{CLKout} = 125 MHz/250 MHz (See Figures 3 and 4)	1 kHz of Carrier		−123/−116		dBc/Hz
		10 kHz of Carrier		−131/−124		dBc/Hz
		100 kHz of Carrier		−131/−124		dBc/Hz
		1 MHz of Carrier		−139/−133		dBc/Hz
		10 MHz of Carrier		−161/−158		dBc/Hz
$t_{jit}(\Phi)$	RMS Phase Jitter	12 kHz to 20 MHz		0.4	0.9	ps
t_{jitter}	Cycle to Cycle, RMS	1000 Cycles		1	8	ps
	Cycle to Cycle, Peak−to−Peak	1000 Cycles		7	30	ps
	Period, RMS	10,000 Cycles		0.6	4	ps
	Period, Peak−to−Peak	10,000 Cycles		5	20	ps
$t_{OE/OD}$	Output Enable/Disable Time				200	ns
t_{DUTY_CYCLE}	Output Clock Duty Cycle (Measured at Cross Point)		48	50	52	%
t_R	Output Rise Time (20% and 80%)			250	400	ps
t_F	Output Fall Time (80% and 20%)			250	400	ps
t_{start}	Start−up Time			1	5	ms
	Aging	1^{st} Year			3	ppm
		Every Year After 1^{st}			1	ppm

NOTE: Device will meet the specifications after thermal equilibrium has been established when mounted in a test socket or printed circuit board with maintained transverse airflow greater than 500 lfpm. Electrical parameters are guaranteed only over the declared operating temperature range. Functional operation of the device exceeding these conditions is not implied. Device specification limit values are applied individually under normal operating conditions and not valid simultaneously.

3. Measurement taken with outputs terminated with 50 ohm to V_{DD}−2 V. See Figure 5.
4. Parameter guarantees 10 years of aging. Includes initial stability at 25°C, shock, vibration, and first year aging.

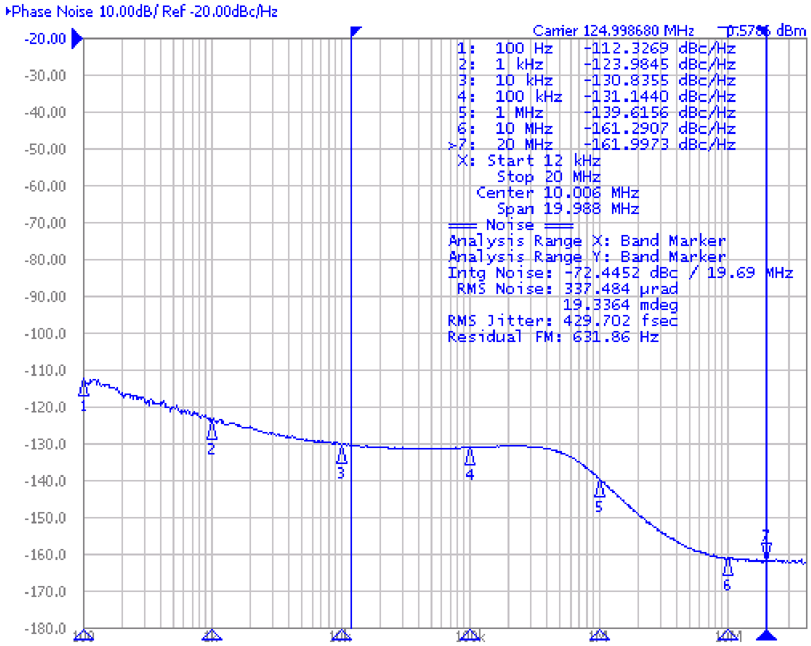


Figure 3. Typical Phase Noise Plot at 125 MHz

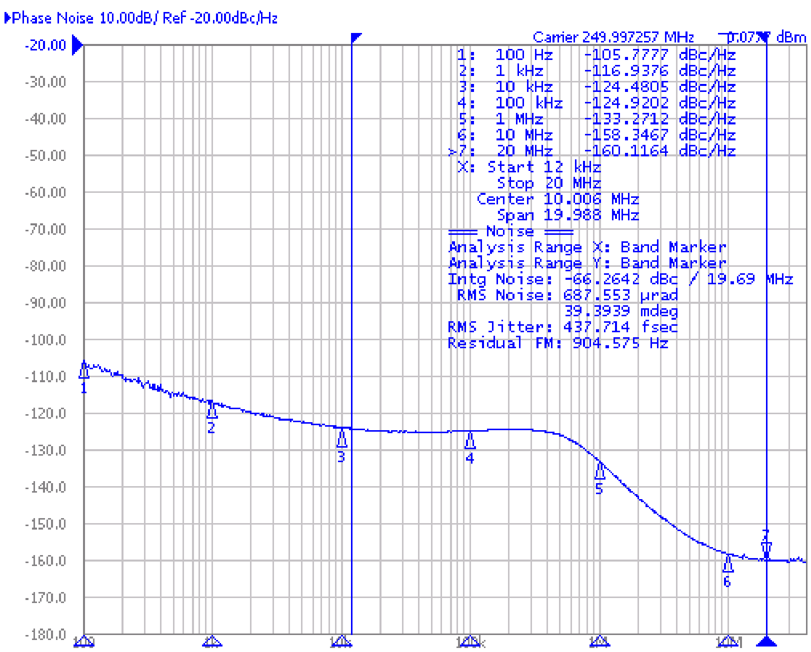


Figure 4. Typical Phase Noise Plot at 250 MHz

Table 8. RELIABILITY COMPLIANCE

Parameter	Standard	Method
Shock	Mechanical	MIL−STD−833, Method 2002, Condition B
Solderability	Mechanical	MIL−STD−833, Method 2003
Vibration	Mechanical	MIL−STD−833, Method 2007, Condition A
Solvent Resistance	Mechanical	MIL−STD−202, Method 215
Thermal Shock	Environment	MIL−STD−833, Method 1011, Condition A
Moisture Level Sensitivity	Environment	MSL1 260°C per IPC/JEDEC J−STD−020D

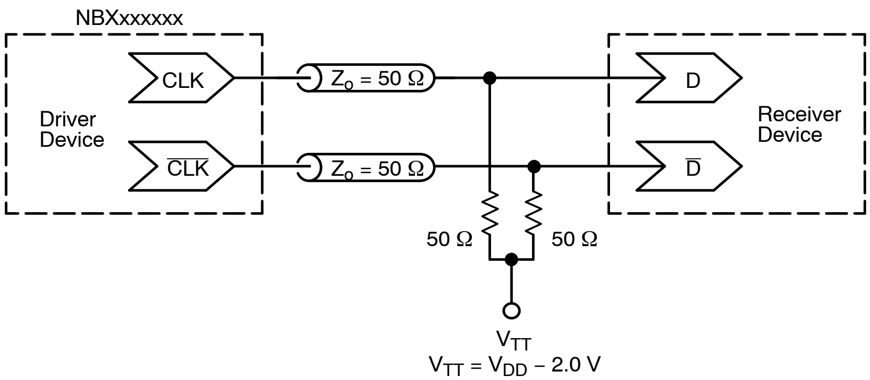


Figure 5. Typical Termination for Output Driver and Device Evaluation (See Application Note AND8020/D − Termination of ECL Logic Devices.)

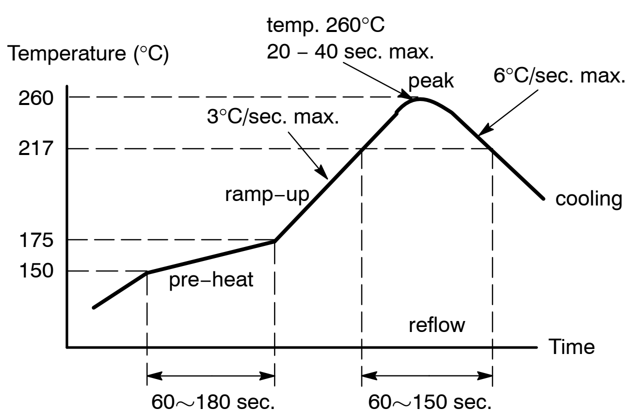
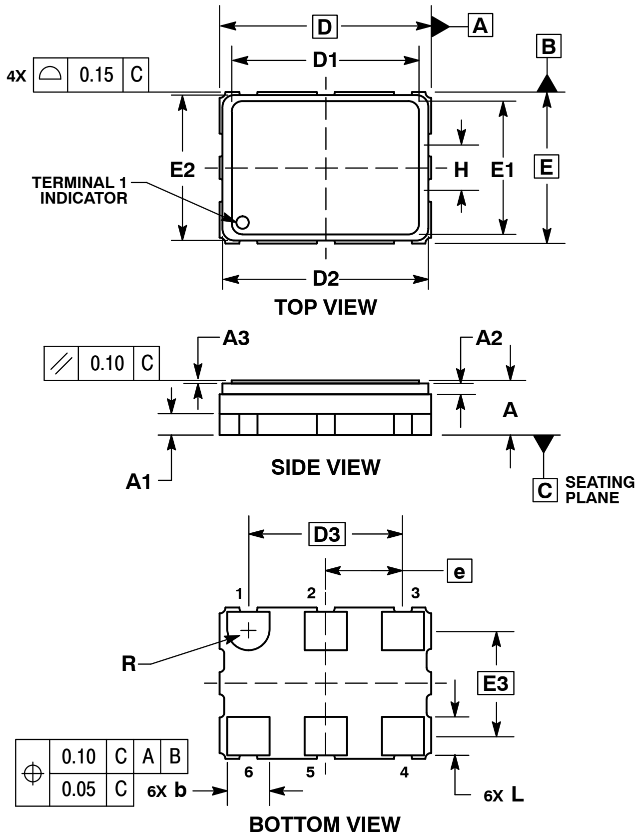


Figure 6. Recommended Reflow Soldering Profile

PACKAGE DIMENSIONS

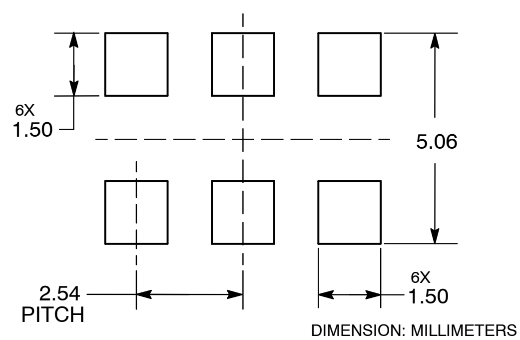
6 PIN CLCC, 7x5, 2.54P
CASE 848AB−01
ISSUE C



NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.

DIM	MILLIMETERS MIN	NOM	MAX
A	1.70	1.80	1.90
A1		0.70 REF	
A2		0.36 REF	
A3	0.08	0.10	0.12
b	1.30	1.40	1.50
D		7.00 BSC	
D1	6.17	6.20	6.23
D2	6.66	6.81	6.96
D3		5.08 BSC	
E		5.00 BSC	
E1	4.37	4.40	4.43
E2	4.65	4.80	4.95
E3		3.49 BSC	
e		2.54 BSC	
H		1.80 REF	
L	1.17	1.27	1.37
R		0.70 REF	

SOLDERING FOOTPRINT*



*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

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