Absolute Maximum Ratings

Voltage Between V+ and V- Terminals 36V
$\pm V_{SUPPLY}$ to Ground (V+, V-) . . . . . $\pm$18V
V_R to Ground . . . . . $-V_{SUPPLY}$
V_L to Ground . . . . . $+V_{SUPPLY}$
Digital and Analog Input Voltage (V_A, V_S, V_D) . . . . . $+V_{SUPPLY}$ +4V
$-V_{SUPPLY}$ -4V
Peak Current (Source to Drain)
(Pulse at 1ms, 10% Duty Cycle Max) 70mA
Continuous Current Any Pin 20mA
ESD Rating . . . . . <2000V

Thermal Information

Thermal Resistance	θ_{JA} (°C/W)	θ_{JC} (°C/W)
CerDIP Package	82	20

Package Power Dissipation at +75°C
CerDIP Package 1.0W
Package Power Dissipation Derating Factor above +75°C
CerDIP Package . . . . . 12.3mW/°C
Junction Temperature . . . . . +175°C
Storage Temperature Range . . . . . -65°C to +150°C
Lead Temperature (Soldering 10s) . . . . . +300°C

Recommended Operating Conditions

Operating Temperature Range . . . . . -55°C to +125°C
Operating Supply Voltage Range . . . . . $\pm$15V
Logic Supply Voltage (V_L) . . . . . +5.0V
Logic Reference Voltage (V_R) 0.0V
Analog Input Voltage (V_S) . . . . . $\pm V_{SUPPLY}$
Address Low Level (V_{AL}) . . . . . 0V to 0.8V
Address High Level (V_{AH}) . . . . . 2.4V to +5.0V

CAUTION: Do not operate at or near the maximum ratings listed for extended periods of time. Exposure to such conditions may adversely impact product reliability and result in failures not covered by warranty.

TABLE 1. D.C. ELECTRICAL PERFORMANCE SPECIFICATIONS

Device Tested at: Supply Voltage = $\pm$15V, V_L = +5.0V, V_R = 0.0V, V_{AH} = 2.4V, V_{AL} = +0.8V, unused pins are grounded, unless otherwise specified.

D.C. PARAMETERS	SYMBOL	CONDITIONS	GROUP A SUBGROUPS	TEMPERATURE (°C)	MIN	MAX	UNITS
Switch "ON" Resistance	R_{DS2}	V_D = -10V, I_S = 10mA S1/S2/S3/S4	1	+25	-	45	Ω
			2, 3	-55 to +125	-	50	Ω
		V_D = 10V, I_S = -10mA S1/S2/S3/S4	1	+25	-	45	Ω
			2, 3	-55 to +125	-	50	Ω
Source "OFF" Leakage Current	$I_{S(OFF)}$	V_S = -10V, V_D = 10V S1/S2/S3/S4	1	+25	-1	1	nA
			2, 3	-55 to +125	-100	100	nA
		V_S = 10V, V_D = -10V S1/S2/S3/S4	1	+25	-1	1	nA
			2, 3	-55 to +125	-100	100	nA
Drain "OFF" Leakage Current	$I_{D(OFF)}$	V_D = -10V, V_S = 10V S1/S2/S3/S4	1	+25	-1	1	nA
			2, 3	-55 to +125	-100	100	nA
		V_D = 10V, V_S = -10V S1/S2/S3/S4	1	+25	-1	1	nA
			2, 3	-55 to +125	-100	100	nA
Channel "ON" Leakage Current	$I_{D(ON)}$	V_D = V_S = 10V S1/S2/S3/S4	1	+25	-2	2	nA
			2, 3	-55 to +125	-200	200	nA
		V_D = V_S = -10V S1/S2/S3/S4	1	+25	-2	2	nA
			2, 3	-55 to +125	-200	200	nA
Low Level Address Current	I_{AL}	V_A = 0V	1	+25	-1	1	µA
			2, 3	-55 to +125	-10	1	µA
High Level Address Current	I_{AH}	V_A = 2.4V, 5V	1	+25	-1	1	µA
			2, 3	-55 to +125	-1	10	µA
Positive Supply Current	$+I_{CC}$	V_A = 0V, 5V	1	+25	-	200	µA
			2, 3	-55 to +125	-	300	µA
Negative Supply Current	$-I_{CC}$	V_A = 0V, 5V	1	+25	-200	-	µA
			2, 3	-55 to +125	-300	-	µA

TABLE 1. D.C. ELECTRICAL PERFORMANCE SPECIFICATIONS (Continued)

Device Tested at: Supply Voltage = ±15V, V_L = +5.0V, V_R = 0.0V, V_{AH} = 2.4V, V_{AL} = +0.8V, unused pins are grounded, unless otherwise specified.

D.C. PARAMETERS	SYMBOL	CONDITIONS	GROUP A SUBGROUPS	TEMPERATURE (°C)	MIN	MAX	UNITS
Logic Supply Current	$+I_L$	V_A = 0V, 5V	1	+25	-	200	µA
			2, 3	-55 to +125	-	300	µA
Reference Supply Current	$+I_R$	V_A = 0V, 5V	1	+25	-200	-	µA
			2, 3	-55 to +125	-300	-	µA

TABLE 2. A.C. ELECTRICAL PERFORMANCE SPECIFICATIONS

Device Tested at: Supply Voltage = ±15V, V_L = +5.0V, V_R = 0.0V, V_{AH} = +5.0V, V_{AL} = +0.0V, unused pins are grounded, unless otherwise specified.

PARAMETERS	SYMBOL	CONDITIONS	GROUP A SUBGROUPS	TEMPERATURE (°C)	MIN	MAX	UNITS
Turn "ON" Time	$t_{(ON)}$	V_S = 10V, -10V C_L = 10pF R_L = 1kΩ	11	-55	-	450	ns
			9	+25	-	500	ns
			10	+125	-	800	ns
Turn "OFF" Time	$t_{(OFF)}$	V_S = 10V, -10V C_L = 10pF R_L = 1kΩ	11	-55	-	350	ns
			9	+25	-	450	ns
			10	+125	-	600	ns

TABLE 3. ELECTRICAL PERFORMANCE SPECIFICATIONS (NOTE 1)

Device Characterized at: $+V_{SUPPLY}$ = +15V, $-V_{SUPPLY}$ = −15V, GND = 0V

PARAMETERS	SYMBOL	CONDITIONS	NOTE	TEMPERATURE (°C)	MIN	MAX	UNITS
"ON" Resistance Match (Channel to Channel)	r_{ON2} Match	V_D = ±10V I_D = 10mA	1	+25	-	10	Ω
Address Capacitance	C_A	V_A = 0V, 5V	1	+25	-	45	pF
Switch Input Capacitance	$C_{S\ (OFF)}$	Switch Off: V_A = 0V	1	+25	-	60	pF
Switch Output Capacitance	$C_{D\ (OFF)}$	Switch Off: V_A = 0V	1	+25	-	60	pF
	$C_{D\ (ON)}$	Switch On: V_A = 5V	1	+25	-	60	pF
Drain to Source Capacitance	$C_{DS\ (OFF)}$	Switch Off: V_A = 0V	1	+25	-	10	pF
Off Isolation	V_{ISO}	V_S = $2V_{P-P}$ @ f = 100kHz, R_L = 100Ω	1	+25	1	60	dB
Crosstalk	V_{CT}	V_S = $2V_{P-P}$ @ f = 100kHz, R_L = 100Ω	1	+25	1	60	dB
Charge Transfer Error	V_{CTE}	V_S = GND, C_L = 0.01µF V_A = 0V to 4V @ f = 200kHz	1	+25	-	30	mV

NOTE:

1. Parameters listed in Table 3 are controlled via design or process parameters and are not directly tested at final production. These parameters are lab characterized upon initial design release, or upon design changes. These parameters are guaranteed by characterization based upon data from multiple production runs which reflect lot to lot and within lot variation.

TABLE 4. ELECTRICAL TEST REQUIREMENTS

MIL-STD-883 TEST REQUIREMENTS	SUBGROUPS (Tables 1 and 2)
Interim Electrical Parameters (Pre Burn-in)	1
Final Electrical Test Parameters	1 (Note 2), 2, 3, 9, 10, 11
Group A Test Requirements	1, 2, 3, 9, 10, 11
Groups C & D Endpoints	1

NOTE:

2. PDA applies to Subgroup 1 only.

Test Circuits

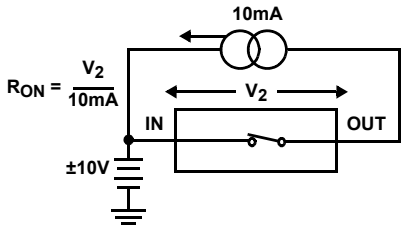


FIGURE 1. R_{DS}

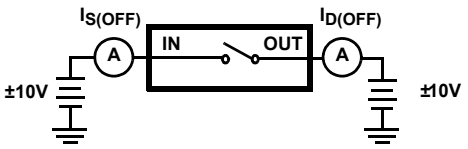


FIGURE 2. $I_{S(OFF)}$

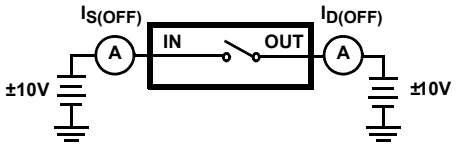


FIGURE 3. $I_{D(OFF)}$

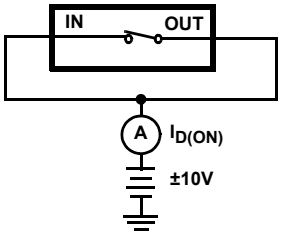


FIGURE 4. $I_{D(ON)}$

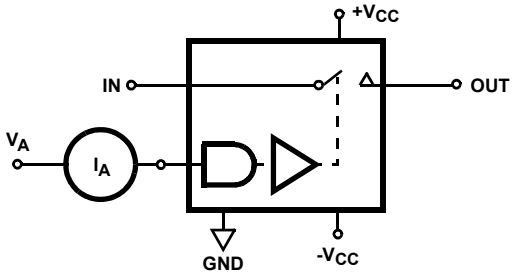


FIGURE 5. ADDRESS CURRENTS

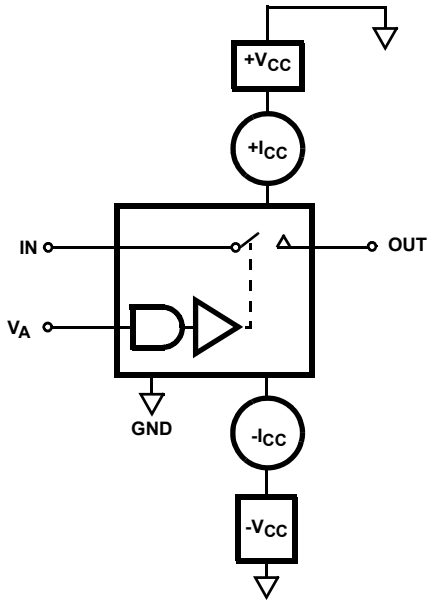


FIGURE 6. SUPPLY CURRENTS

Test Circuits (Continued)

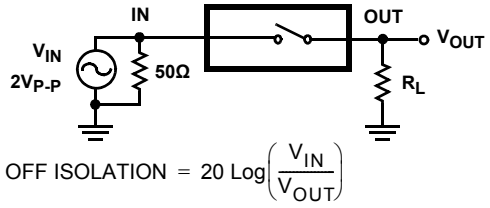
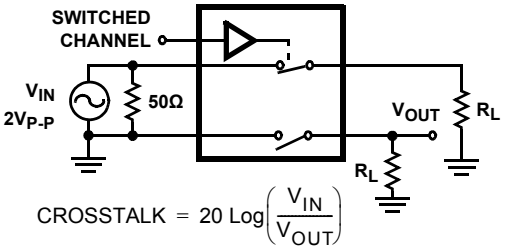
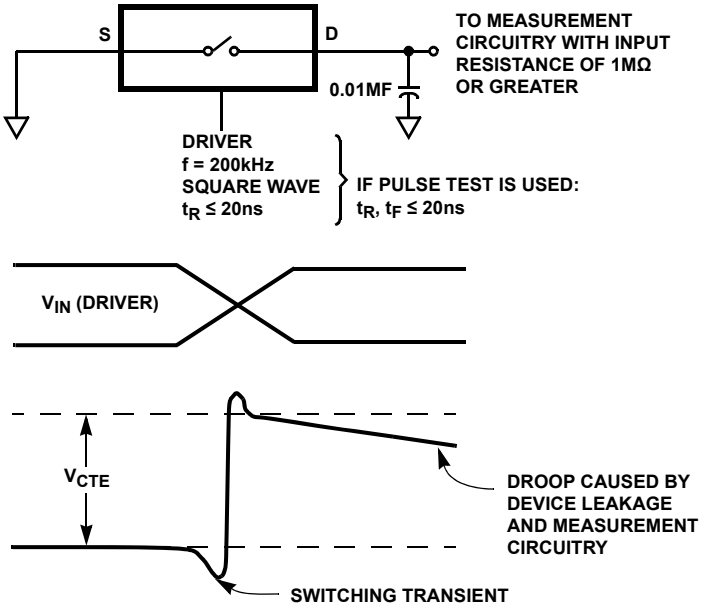


FIGURE 7. OFF ISOLATION



NOTE: Applies only to dual or double throw switches.

FIGURE 8. CROSSTALK



NOTE: V_{CTE} may be a positive or negative value.

FIGURE 9. CHARGE TRANSFER

Test Characteristics

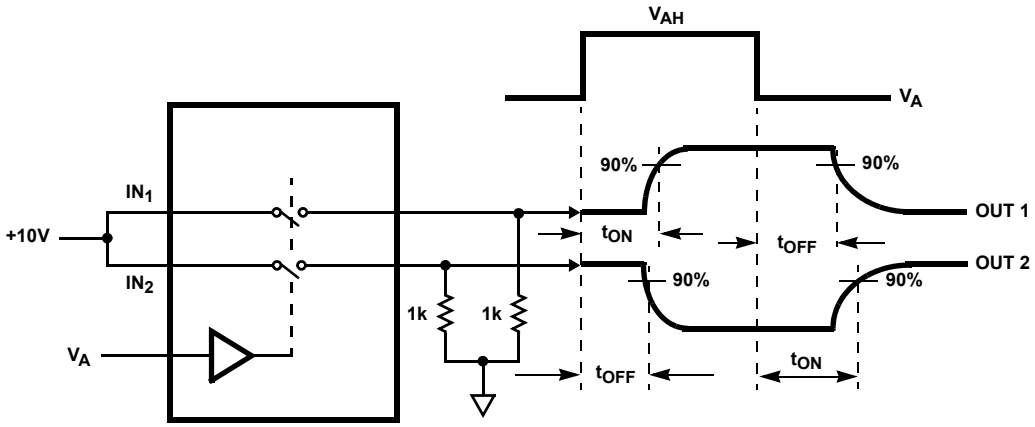


FIGURE 10. ON/OFF SWITCH TIME (t_{ON}, t_{OFF})

Test Characteristics (Continued)

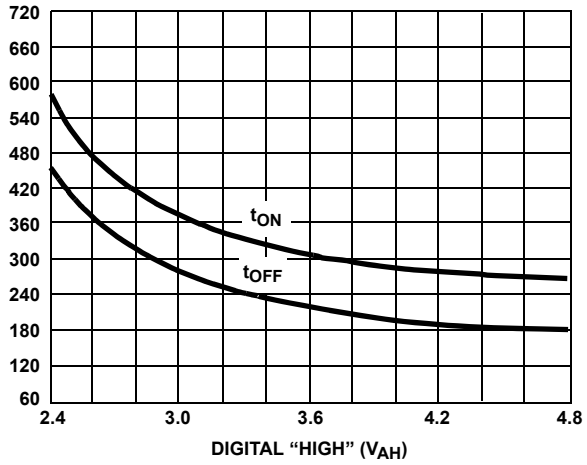


FIGURE 11. SWITCHING TIMES FOR DIGITAL TRANSITION

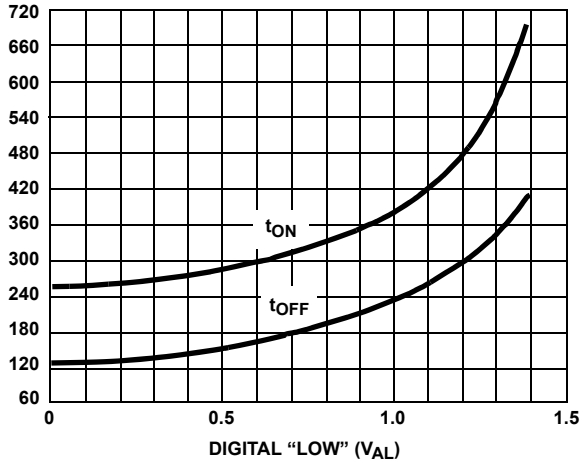
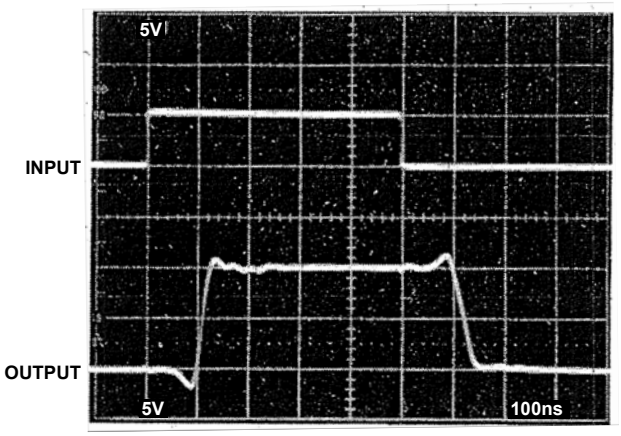


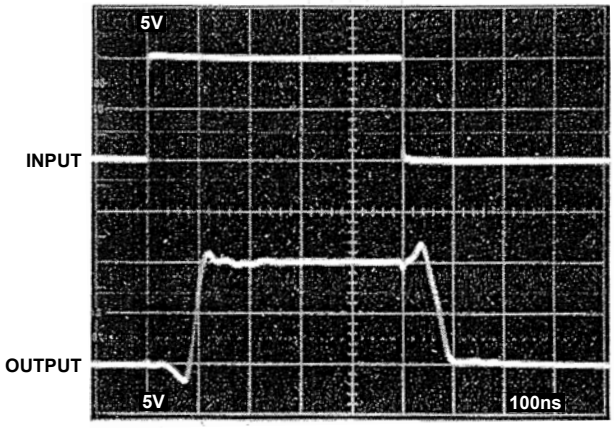
FIGURE 12. SWITCHING TIMES FOR NEGATIVE DIGITAL TRANSITION

Test Waveforms



Vertical Scale: Input = 5V/Div, (TTL; V_{AH} = 5V, V_{AL} = 0V)
Output = 5V/Div
Horizontal Scale: 100ns/Div

FIGURE 13.

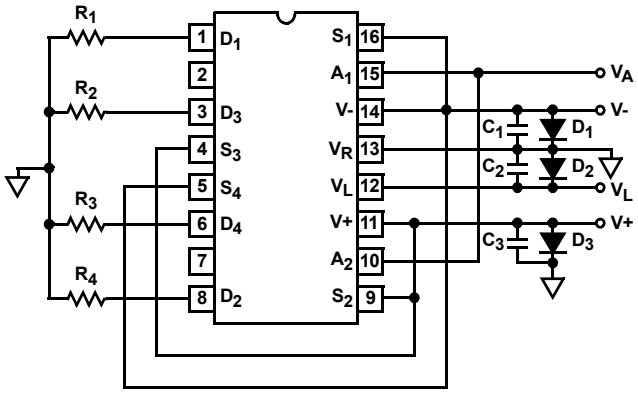


Vertical Scale: Input = 5V/Div, (CMOS; V_{AH} = 10V, V_{AL} = 0V)
Output = 5V/Div
Horizontal Scale: 100ns/Div

FIGURE 14.

Burn-In Circuit

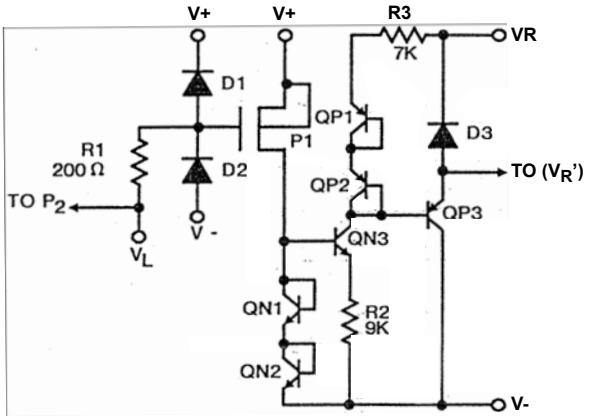
HI-5046A/883 CERAMIC DIP



NOTES:

R_1 thru R_4 = 10kΩ, ±5%, 1/4W (Min)
C_1, C_2, C_3 = 0.01µF/Socket (Min) or 0.1µF/Row, (Min)
D_1, D_2, D_3 = 1N4002 or Equivalent/Board
V_L = 5.5V ±0.5V
A_2 = A_2 = 5.5V ±0.5V
| (V+) - (V-) | = 30V

Schematic Diagrams



NOTE: Connect V+ to V_L for minimizing power consumption when driving from CMOS circuits.

FIGURE 15. TTL/CMOS REFERENCE CIRCUIT

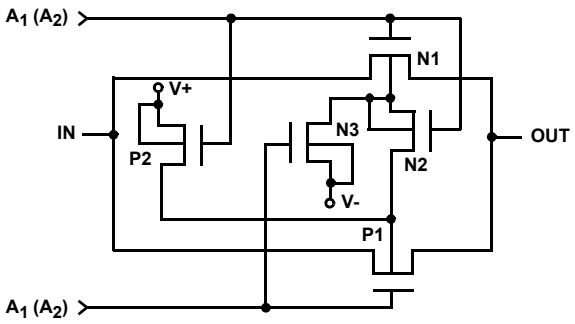
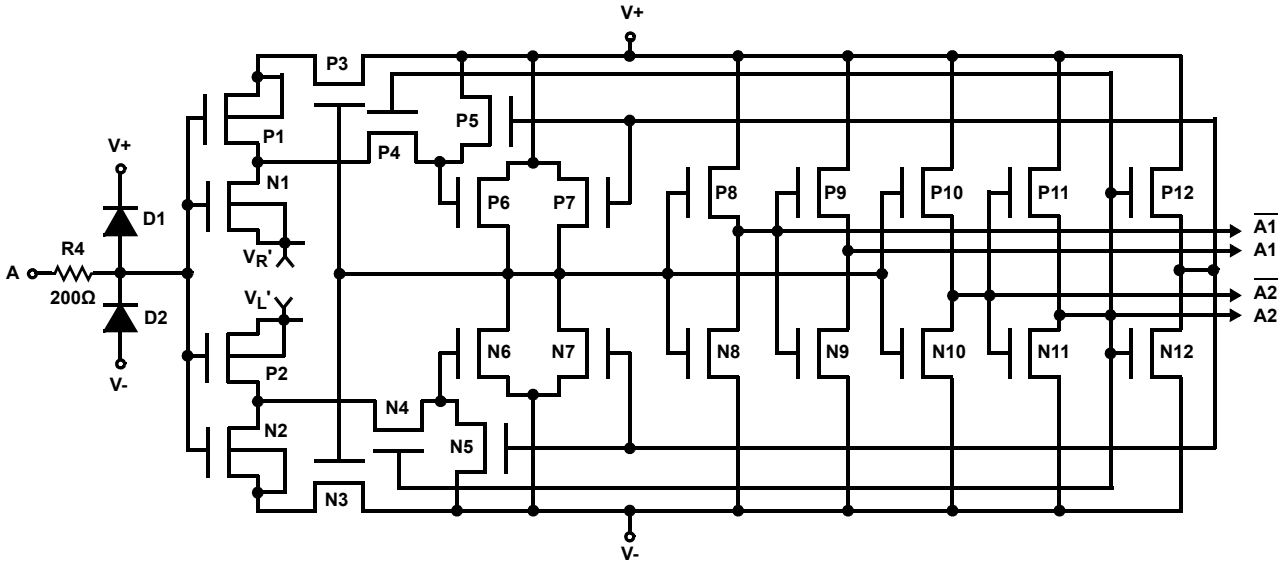


FIGURE 16. SWITCH CELL



All N-Channel bodies to V-, all P-Channel bodies to V+, except as shown.

DIGITAL INPUT BUFFER AND LEVEL SHIFTER

Die Characteristics

DIE DIMENSIONS:

96mils x 81mils x 19mils
(2430µm x 2050µm x 480µm

METALLIZATION:

Type: Aluminum
Thickness: 16kÅ ±2kÅ

GLASSIVATION:

Type: Nitride over Silox
Silox Thickness: 12kÅ ±2kÅ
Nitride Thickness: 3.5kÅ ±1kÅ

SUBSTRATE POTENTIAL (Powered-up): V-

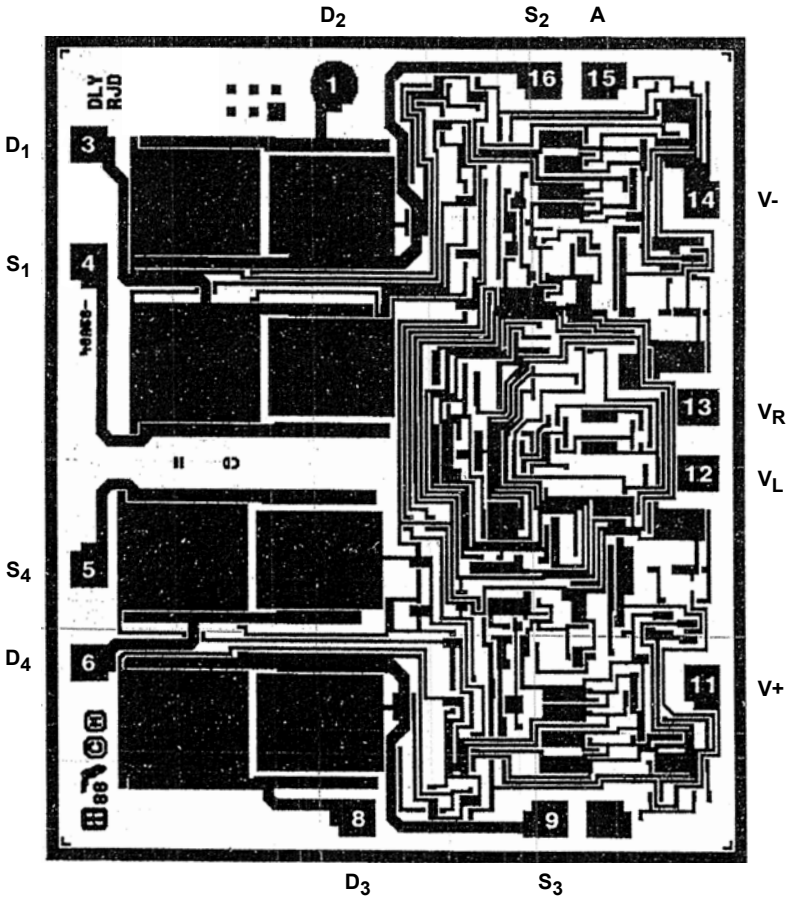
DEVICE COUNT: 82

WORST CASE CURRENT DENSITY:

$1.0 \times 10^5 A/cm^2$ at 20mA

Metallization Mask Layout

HI-5046A/883



NOTE: Unused pins may be connected. Ground all unused pins.

Design Information

The information contained in this section has been developed through characterization and is for use as application and design information only. No guarantee is implied.

Typical Performance Curves $T_A = +25°C$, $V_{SUPPLY} = \pm15V$

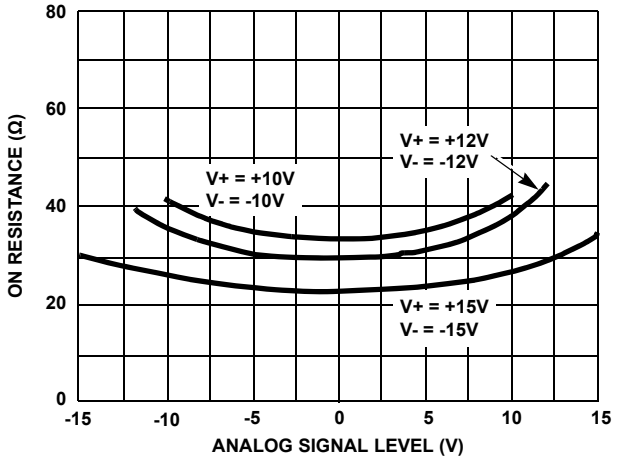


FIGURE 17. ON RESISTANCE vs ANALOG SIGNAL LEVEL AND POWER SUPPLY VOLTAGE

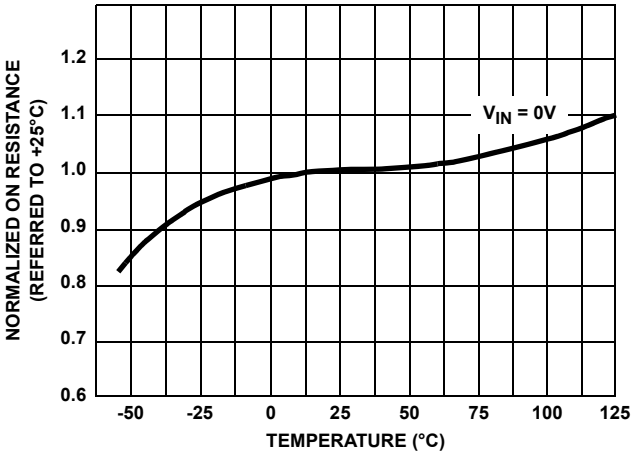


FIGURE 18. NORMALIZED ON RESISTANCE vs TEMPERATURE

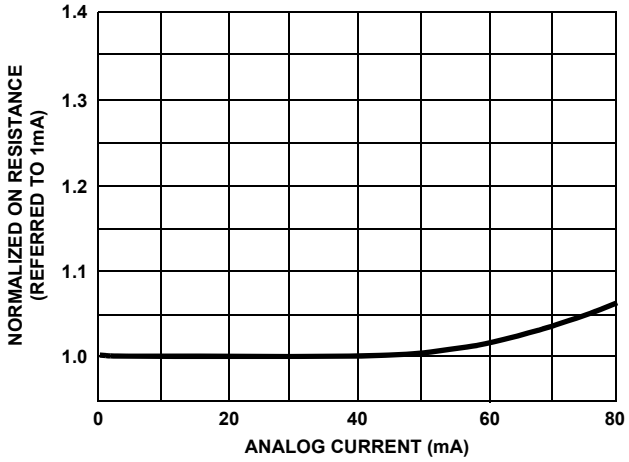


FIGURE 19. NORMALIZED ON RESISTANCE vs ANALOG CURRENT

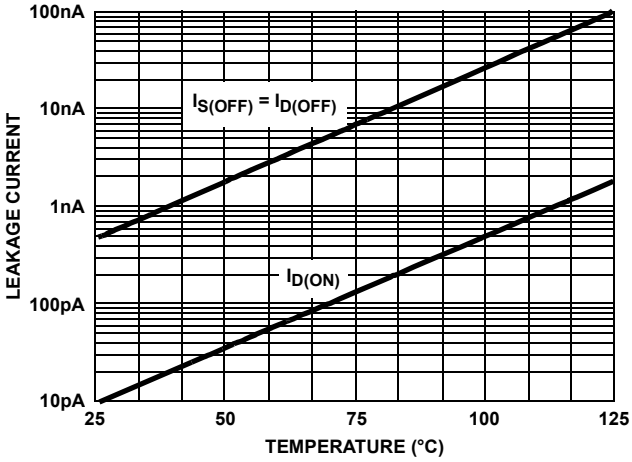


FIGURE 20. ON/OFF LEAKAGE CURRENTS vs TEMPERATURE

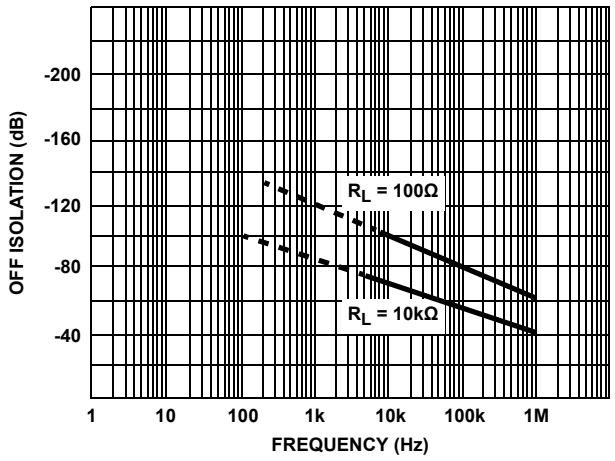


FIGURE 21. OFF ISOLATION vs FREQUENCY

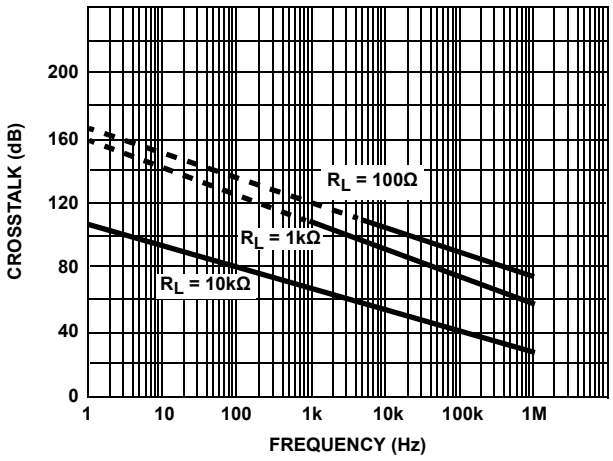


FIGURE 22. CROSSTALK vs FREQUENCY

Design Information

The information contained in this section has been developed through characterization and is for use as application and design information only. No guarantee is implied.

Typical Performance Curves $T_A = +25°C$, $V_{SUPPLY} = \pm15V$ (Continued)

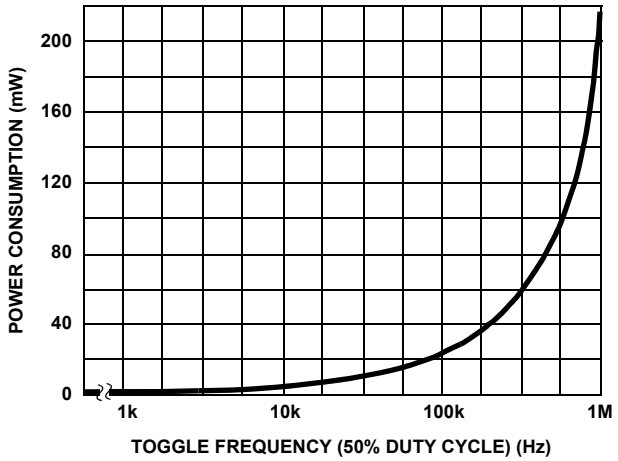
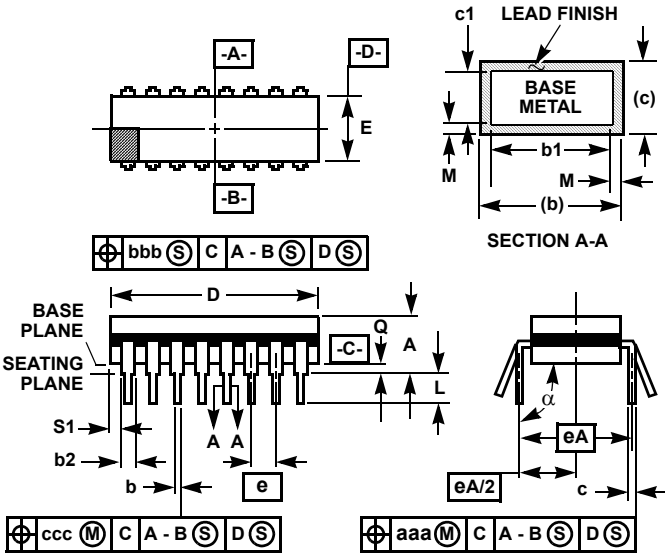


FIGURE 23. POWER CONSUMPTION vs FREQUENCY

Ceramic Dual-In-Line Frit Seal Packages (CERDIP)



NOTES:

1. Index area: A notch or a pin one identification mark shall be located adjacent to pin one and shall be located within the shaded area shown. The manufacturer's identification shall not be used as a pin one identification mark.
2. The maximum limits of lead dimensions b and c or M shall be measured at the centroid of the finished lead surfaces, when solder dip or tin plate lead finish is applied.
3. Dimensions b1 and c1 apply to lead base metal only. Dimension M applies to lead plating and finish thickness.
4. Corner leads (1, N, N/2, and N/2+1) may be configured with a partial lead paddle. For this configuration dimension b3 replaces dimension b2.
5. This dimension allows for off-center lid, meniscus, and glass overrun.
6. Dimension Q shall be measured from the seating plane to the base plane.
7. Measure dimension S1 at all four corners.
8. N is the maximum number of terminal positions.
9. Dimensioning and tolerancing per ANSI Y14.5M - 1982.
10. Controlling dimension: INCH.

F16.3 MIL-STD-1835 GDIP1-T16 (D-2, CONFIGURATION A)
16 LEAD CERAMIC DUAL-IN-LINE FRIT SEAL PACKAGE

SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	-	0.200	-	5.08	-
b	0.014	0.026	0.36	0.66	2
b1	0.014	0.023	0.36	0.58	3
b2	0.045	0.065	1.14	1.65	-
b3	0.023	0.045	0.58	1.14	4
c	0.008	0.018	0.20	0.46	2
c1	0.008	0.015	0.20	0.38	3
D	-	0.840	-	21.34	5
E	0.220	0.310	5.59	7.87	5
e	0.100 BSC		2.54 BSC		-
eA	0.300 BSC		7.62 BSC		-
eA/2	0.150 BSC		3.81 BSC		-
L	0.125	0.200	3.18	5.08	-
Q	0.015	0.060	0.38	1.52	6
S1	0.005	-	0.13	-	7
α	90^o	105^o	90^o	105^o	-
aaa	-	0.015	-	0.38	-
bbb	-	0.030	-	0.76	-
ccc	-	0.010	-	0.25	-
M	-	0.0015	-	0.038	2, 3
N	16		16		8

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