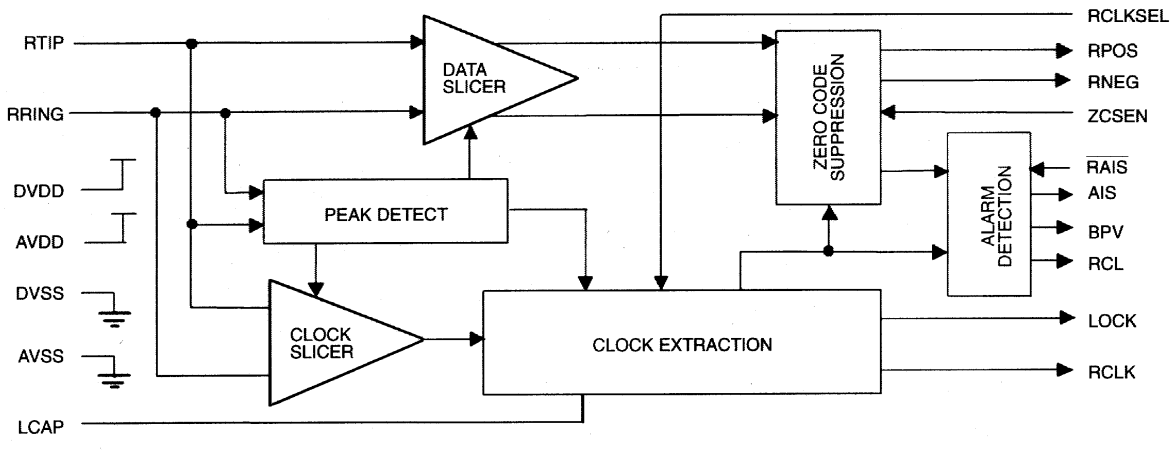
DS2187 BLOCK DIAGRAM Figure 1



LINE INPUT

Input signals are coupled to the DS2187 via a 1:2 center-tapped transformer as shown in Figure 2. For T1 applications, R1 and R2 must be 200 ohms in order to properly terminate the line at 100 ohms. R1 and R2 are set at 150 or 240 ohms for CEPT applications. Special internal circuitry of the RTIP and RRING inputs permits negative signal excursions below V_{SS}, which will occur in the circuit in Figure 2.

PEAK DETECTOR AND SLICERS

Signal pulses present at RTIP and RRING are sampled by an internal peak detect circuit. The clock and data slicer threshold are set for 50% of the sampled peak voltage.

Peak input levels at RRIP and RRING must exceed 0.6 volts to establish minimum slicer thresholds. Signals below this level will cause RCL to transition high after 192 bit times.

CLOCK EXTRACTION

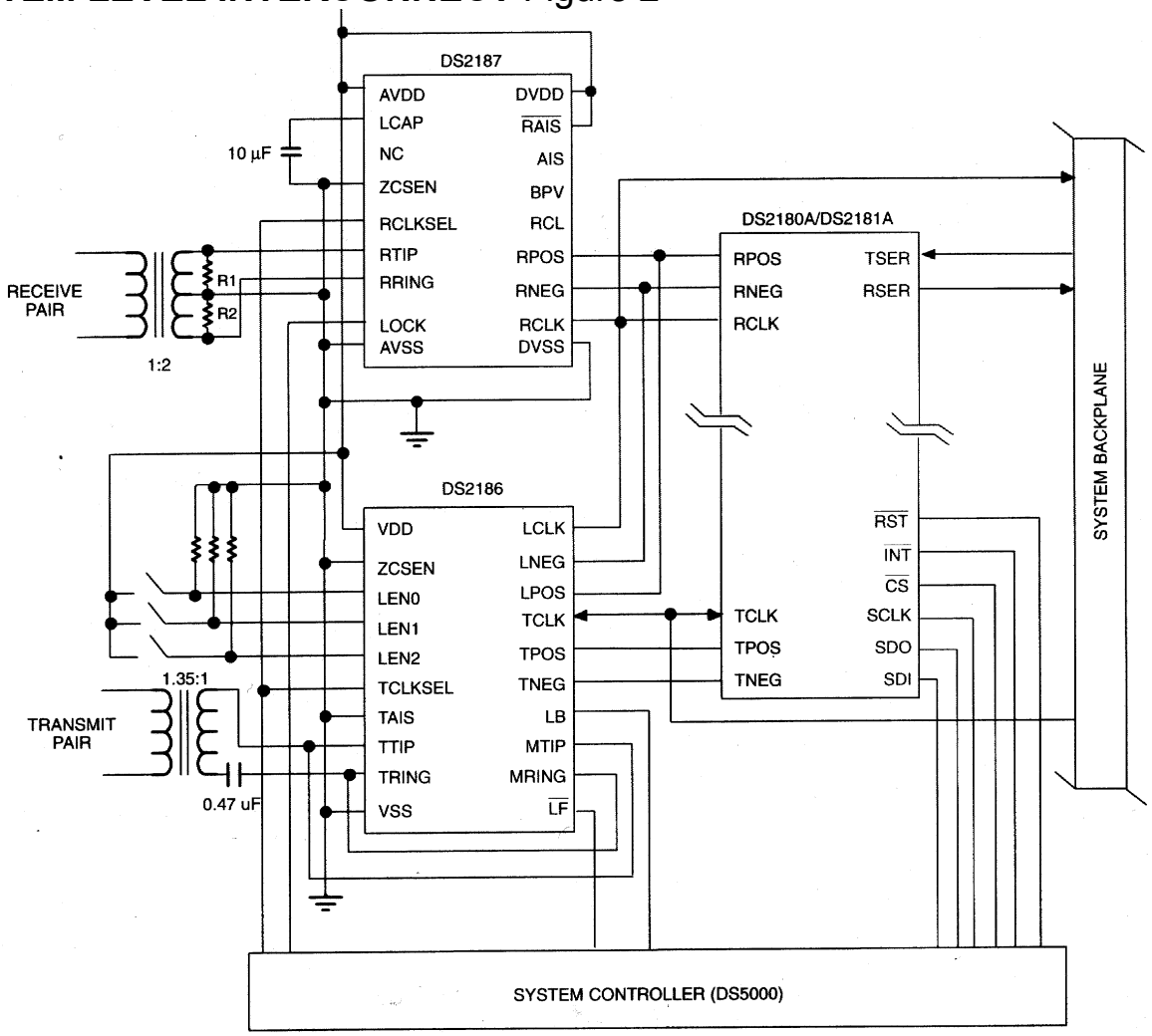
The DS2187 utilizes both frequency locked (FLL) and digital phase locked (DPLL) loops to recover data and clock from the incoming AMI signal. T1 applications utilize a 18.528 MHz clock divided by either 11, 12, or 13 to match the phase of the incoming jittered line signal. This technique affords exceptional jitter tracking which enables the DS2187 to meet the latest AT&T TR 62411 and ECSA jitter specifications. A 24.576 MHz clock divided by 11, 12, or 13 provides jitter tracking in the CEPT mode. The DPLL output is buffered and presented at RCLK. An on-chip, laser-trimmed, voltage-controlled oscillator (V_{CO}) provides the precision 18.528 MHz and 24.576 MHz frequency sources utilized in the FLL. The FLL is a high-Q circuit which tracks the average frequency of the incoming signal, minimizing the effect of the DPLL on output jitter.

During the acquisition time or if RCL goes high, the LOCK pin will go low to indicate a loss of synchronization to the line signal. Once this pin goes high, the FLL has achieved frequency lock and valid data is present at the RPOS and RNEG outputs.

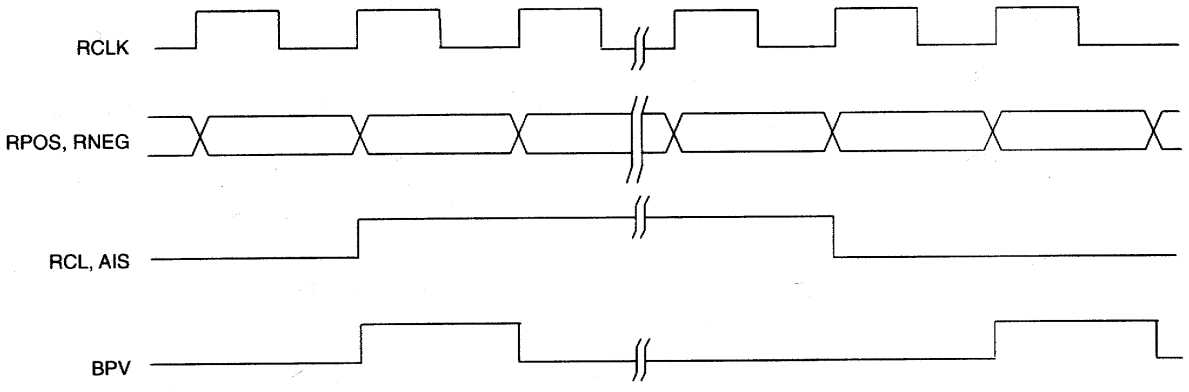
PIN DESCRIPTION Table 1

PIN	SYMBOL	TYPE	DESCRIPTION
1	AVDD	-	**Analog Positive Supply.** 5.0 volts.
2	$\overline{\text{RAIS}}$	I	**Reset Alarm Indication Signal.** Every other low pulse at this input establishes the AIS alarm detection period.
3	ZCSEN	I	**0 Code Suppression Enable.** When high, incoming B8ZS (RCLKSEL=0) or HDB3 (RCLKSEL=1) code words are replaced with all 0s at RPOS and RNEG; when low, no code replacement occurs.
4	LCAP	-	**Loop Cap.** Part of internal loop filter; attach a 10 microfarad capacitor from this pin to V_{SS}.
5	RCLKSEL	I	**Receive Clock Select.** Tie to V_{SS} for 1.544 MHz (T1) applications, to V_{DD} for 2.048 MHz (CEPT) applications.
6 7	RTIP RRING	I	**Receive Tip and Ring.** Connect to line transformer as shown in Figure 2.
8	LOCK	O	**Frequency Lock.** High state indicates that internal circuitry is phase- and frequency-locked to the incoming signal at RRING and RTIP.
9	AVSS	-	**Analog Signal Ground.** 0.0 volts.
10	DVSS	-	**Digital Signal Ground.** 0.0 volts.
11	RCLK	O	**Receive Clock.** Extracted line rate clock.
12 13	RNEG RPOS	O	**Receive Data.** Extracted receive data; updated on rising edge of RCLK.
14	NC	-	**No Connect.** Do not connect to this pin.
15	BPV	O	**Bipolar Violation.** Transitions high for the full bit period when a bit in violation appears at RPOS or RNEG; B8ZS code words are not accused when ZCSEN=1. BPV not valid for RCLKSEL=1 and ZCSEN=1.
16	AIS	O	**Alarm Indication Signal.** High when the received data stream has contained less than three 0s during the last two periods of the $\overline{\text{RAIS}}$ signal.
17	RCL	O	**Receive Carrier Loss.** High if 192 0s appear at RPOS and RNEG; reset on next occurrence of a one.
18	DVDD	-	**Digital Positive Supply.** 5.0 volts

SYSTEM LEVEL INTERCONNECT Figure 2



OUTPUT TIMING Figure 3



0 CODE SUPPRESSION

The device will decode incoming B8ZS (RCLKSEL=0) or HDB3 (RCLKSEL=1) code words and replace them with an all-0 code when ZCSEN=1. When ZCSEN=0, code words will pass through the device without being altered. This feature can be disabled when the DS2187 is used with transceiver devices such as the DS2180A DS2181A, DS2141A, or DS2143.

ALARM DETECTION

The extracted data is monitored for network alarm and error conditions. RCL is set when 192 consecutive 0s occur; it is cleared on the next one occurrence. AIS is set when less than three 0s have appeared at RPOS and RNEG during the last two periods of the $\overline{\text{RAIS}}$ signal; once set, AIS will remain high for the next two periods of $\overline{\text{RAIS}}$. AIS will return low when more than two 0s appear. BPV reports bipolar violations as they occur at RPOS and RNEG; B8ZS code words will not be flagged by BPV when ZCSEN=1.

BYPASSING AND LAYOUT CONSIDERATIONS

The DS2187 contains both precision analog and high-speed digital circuitry on the same chip. The power supplies of these circuits (AVDD, AVSS, DVDD and DVSS) should be connected to system analog and digital supplies. If separate system supplies do not exist, the appropriate supply pins can be tied together. Tying the analog and digital supplies together on the DS2187 will not degrade its performance, provided the power supply is sufficiently decoupled.

To assure optimum performance, the length of LCAP, RTIP and RRING printed circuit board traces should be minimized and isolated from neighboring interconnect.

ABSOLUTE MAXIMUM RATINGS*

Voltage on Any Pin Relative to Ground	-0.1V to +7.0V
Operating Temperature	0° to 70°C
Storage Temperature	-55°C to +125°C
Soldering Temperature	260°C for 10 seconds

* This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operation sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods of time may affect reliability.

** Inputs other than RTIP and RRING

RECOMMENDED DC OPERATING CONDITIONS (0°C to 70°C)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Input Logic 1	V_{IH}	2.0		V_{CC}+.3	V	1
Input Logic 0	V_{IL}	-0.3		+0.8	V	1
Supply	V_{DD}	4.75		5.25	V	
Input Voltage Swing RTIP,RRING	V_{IN}	-7.0		12.0	V	

DC ELECTRICAL CHARACTERISTICS (0°C to 70°C)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Supply Current	I_{DD}		18	25	mA	2
Input Leakage	I_L	-1.0		+10	µA	1, 3
Output Current @ 2.4V	I_{OH}	-1.0			mA	4
Output Current @ 0.4V	I_{OL}	+4.0			mA	4

NOTES:

1. All inputs except RTIP and RRING.

2. Outputs open.

3. $0.0V < V_{IN} < V_{DD}$.

4. All outputs.

ANALOG ELECTRICAL CHARACTERISTICS (0°C to 70°C; V_{DD} = 5.0V ± 5%)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Clock Acquisition	t_{LOCK}		50		ms	1
RTIP, RRING Minimum Sensitivity	V_{THRES}		.4	.6	V_{pk}	2
FLL Loop Bandwidth	f_{BW}		50		Hz	3
Capture Range	f_{CAP}		± 6		%	4
Input Jitter Tolerance	J_{IN}	200			UI	5

NOTES:

1. Time from reappearance of a valid signal at RPOS and RNEG to a LOCK=1.
2. Minimum peak voltage necessary for proper processing of signal.
3. Loop bandwidth when in lock (LOCK=1).
4. When out of lock (LOCK=0), measured as a percent of incoming clock frequency.
5. Maximum input jitter in unit intervals at 10 Hz.

CAPACITANCE (T_A = 25°C)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Input Capacitance	C_{IN}			5	pF	
Output Capacitance	C_{OUT}			7	pF	

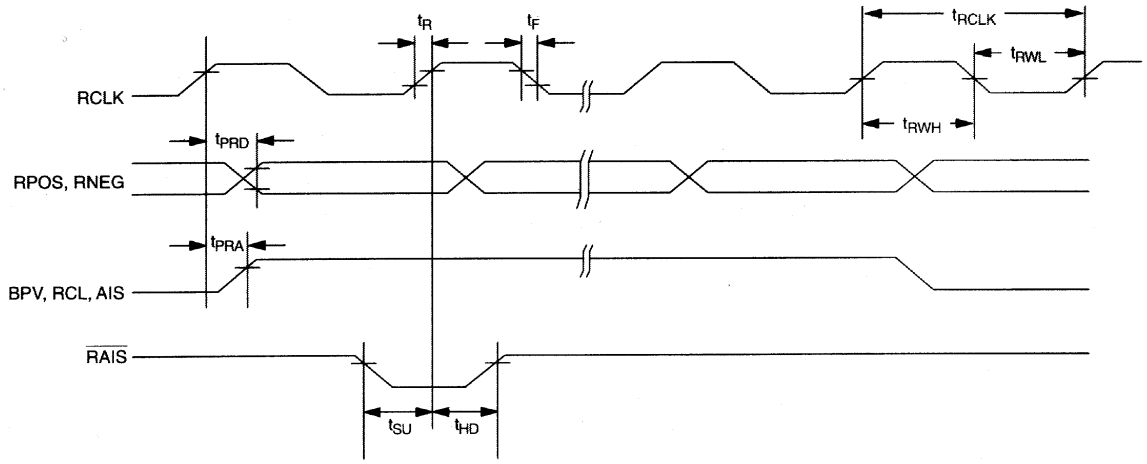
AC ELECTRICAL CHARACTERISTICS (0°C to 70°C; V_{DD} = 5.0V ± 5%)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
RCLK Period	t_{RCLK}	594	648	702	ns	1,3
RCLK Period	t_{RCLK}	445	488	530	ns	2,3
RCLK Pulse Width	t_{RWH}, t_{RWL}		324		ns	1
RCLK Pulse Width	t_{RWH}, t_{RWL}		244		ns	2
RCLK Rise and Fall Times	t_R, t_F			20	ns	
Propagation delay RCLK TO RPOS, RNEG	t_{PRD}			75	ns	
Propagation delay RCLK to BPV, RCL, AIS	t_{PRA}			75	ns	
$\overline{RAIS}$ Setup	t_{SU}, t_{HD}	50			ns	

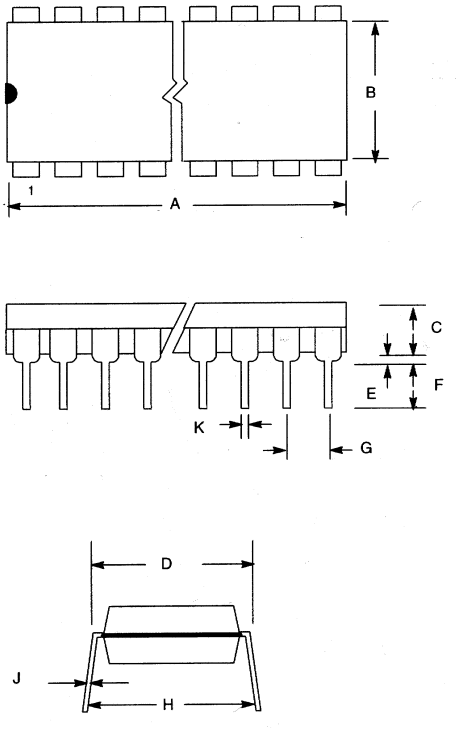
NOTES:

1. T1 applications (RCLKSEL=0).
2. CEPT applications (RCLKSEL=1).
3. Minimum and maximum limits shown reflect changes in DPLL divide ratio as required to track jitter.

AC TIMING DIAGRAM Figure 4

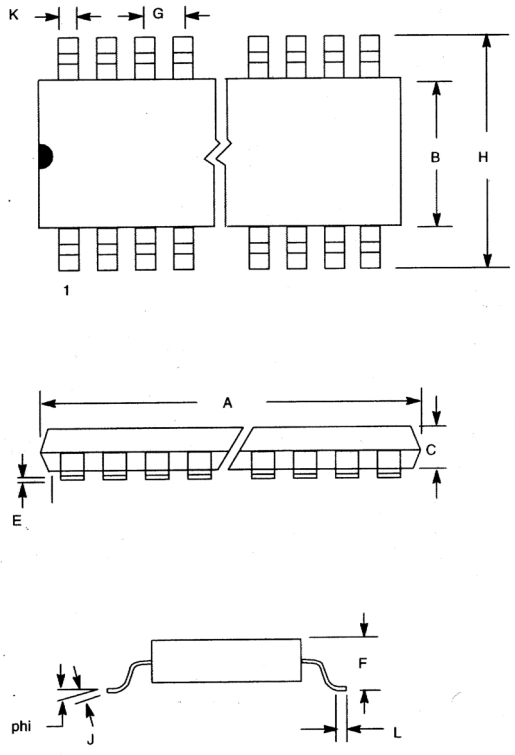


DS2187 RECEIVE LINE INTERFACE 18-PIN DIP



PKG	18-PIN	
DIM	MIN	MAX
A IN	0.890	0.920
MM		
B IN	0.240	0.260
MM	6.10	6.60
C IN	0.120	0.140
MM	3.05	3.56
D IN	0.300	0.325
MM	7.62	8.26
E IN	0.015	0.040
MM	0.38	1.02
F IN	0.120	0.140
MM	3.04	3.56
G IN	0.090	0.110
MM	2.23	2.79
H IN	0.320	0.370
MM	8.13	9.40
J IN	0.008	0.012
MM	0.20	0.30
K IN	0.015	0.021
MM	0.38	0.53

DS2187S RECEIVE LINE INTERFACE 20-PIN SOIC



PKG	18-PIN	
DIM	**MIN**	**MAX**
A IN	0.500	0.511
MM	12.70	12.99
B IN	0.290	0.300
MM	7.37	7.65
C IN	0.089	0.095
MM	2.26	2.41
E IN	0.004	0.012
MM	0.102	0.30
F IN	0.094	0.105
MM	2.38	2.68
G IN	0.050 BSC	
MM	1.27 BSC	
H IN	0.398	0.416
MM	10.11	10.57
J IN	0.009	0.013
MM	0.229	0.33
K IN	0.013	0.019
MM	0.33	0.48
L IN	0.016	0.040
MM	0.406	1.20
phi	0°	8°

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