ABSOLUTE MAXIMUM RATINGS

VCCIN to GND...+7V, -0.3V
VPPIN to GND ....+13.2V, -0.3V
DRV5, DRV3, DRV to GND ....(VPPIN + 0.3V), -0.3V
AVPP, BVPP to GND ....(VPPIN + 0.3V), -0.3V
All Other Pins to GND ....(VCCIN + 0.3V), -0.3V
Continuous Power Dissipation (T_A = +70°C)
8-Pin Plastic DIP (derate 9.09mW/°C above +70°C) 727mW
8-Pin SO (derate 5.88mW/°C above +70°C).......................471mW
14-Pin Plastic DIP (derate 10.00mW/°C above +70°C).......800mW
14-Pin SO (derate 8.33mW/°C above +70°C) 667mW

Operating Temperature Ranges:
MAX61_C__ ....0°C to +70°C
MAX61_E__ ....-40°C to +85°C
Storage Temperature Range ....-65°C to +160°C
Lead Temperature (soldering, 10sec) ....+300°C

Stresses beyond those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

(VCCIN = +5V, VPPIN = +12V, T_A = T_{MIN} to T_{MAX}, unless otherwise noted.)

PARAMETER	CONDITIONS			MIN	TYP	MAX	UNITS
POWER REQUIREMENTS							
VCCIN Input Voltage Range				2.85		5.5	V
VPPIN Input Voltage Range				0		12.6	V
VPPIN Supply Current (12V Mode)	AVPP = BVPP = VPPIN = 12.6V	MAX613	$\overline{SHDN}$ = 0V		0.05	1	µA
			$\overline{SHDN}$ = VCCIN		2.25	10	
		MAX614			0.05	1	
VPPIN Supply Current (5V Mode)	VPPIN = 12.6V, AVPP = BVPP= VCCIN	MAX613	$\overline{SHDN}$ = 0V		0.05		µA
			$\overline{SHDN}$ = VCCIN		2		
		MAX614			0.05		
VPPIN Supply Current (0V Mode)	AVPP = BVPP = 0V	MAX613	$\overline{SHDN}$ = 0V		0.05		µA
			$\overline{SHDN}$ = VCCIN		2.25		
		MAX614			0.05		
VCCIN Supply Current (12V Mode)	AVPP = BVPP = VPPIN	MAX613	$\overline{SHDN}$ = 0V		3.5		µA
			$\overline{SHDN}$ = VCCIN		20		
		MAX614			3.5		
VCCIN Supply Current (5V Mode)	AVPP = BVPP = VCCIN	MAX613	$\overline{SHDN}$ = 0V		3.5	10	µA
			$\overline{SHDN}$ = VCCIN		22	50	
		MAX614			3.5	10	
VCCIN Supply Current (0V Mode)	AVPP = BVPP = 0V	MAX613	$\overline{SHDN}$ = 0V		3.5		µA
			$\overline{SHDN}$ = VCCIN		20		
		MAX614			3.5		

ELECTRICAL CHARACTERISTICS (continued)

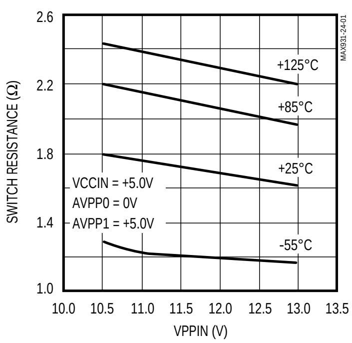
(V_{CCIN} = +5V, V_{PPIN} = +12V, T_A = T_{MIN} to T_{MAX}, unless otherwise noted.)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
DC CHARACTERISTICS					
AVPP, BVPP Switch Resistance	VPPIN = 11.4V, 0mA < I_{LOAD} < 120mA (12V mode)		1.60	2.45	Ω
	VCCIN = 4.5V, 0mA < I_{LOAD} < 1mA (5V mode)		30	50	
	VPPIN = 11.4V, 0mA < I_{LOAD} < 1mA (0V mode)		135	300	
DRV, DRV3, DRV5 Leakage Current	High-impedance mode		1	75	nA
DRV, DRV3, DRV5 Output Voltage Low	I_{LOAD} = 1mA		0.1	0.4	V
LOGIC SECTION					
Logic Input Leakage Current				1	µA
Logic Input High		2.4			V
Logic Input Low				0.8	V
VCC to DRV_ Propagation Delay			50		ns

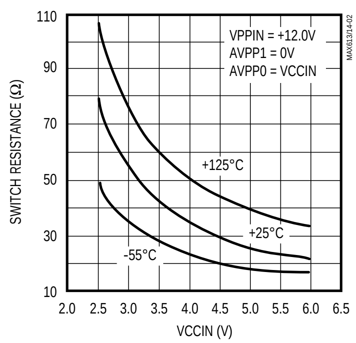
Typical Operating Characteristics

(Circuit of Figure 1, T_A = +25°C, unless otherwise noted.)

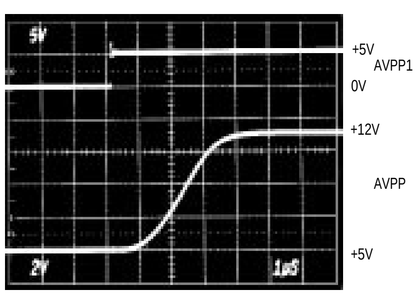
AVPP SWITCH RESISTANCE (12V MODE)



AVPP SWITCH RESISTANCE (5V MODE)



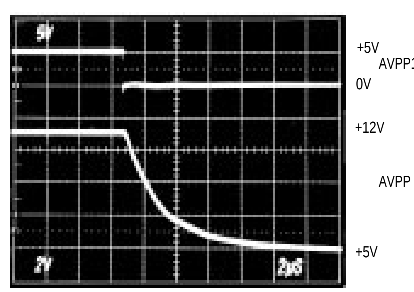
AVPP SWITCHING 5V TO 12V



1µs/div

C_{VPPIN} = 1µF, AVPP0 = $\overline{AVPP1}$, C_{AVPP} = 0.1µF

AVPP SWITCHING 12V TO 5V



2µs/div

C_{VPPIN} = 1µF, AVPP0 = $\overline{AVPP1}$, C_{AVPP} = 0.1µF

Dual-Slot PCMCIA Analog Power Controllers

Pin Description

PIN		NAME	FUNCTION
MAX613	MAX614		
1	1	GND	Ground
2	2	AVPP1	Logic inputs that control the voltage on AVPP (see Table 1 in *Detailed Description*).
3	3	AVPP0	
4	—	BVPP1	Logic inputs that control the voltage on BVPP (see Table 2 in *Detailed Description*).
5	—	BVPP0	
6	—	VCC1	Logic input that controls the state of DRV3 and DRV5 (see Table 3 in *Detailed Description*).
7	4	VCC0	Logic input that controls the state of DRV on the MAX614. On the MAX613, both VCC0 and VCC1 control the state of DRV3 and DRV5 (see Table 3 in *Detailed Description*).
—	5	DRV	Open-drain power MOSFET gate-driver output used to switch the slot VCC supply voltage. DRV sinks current when VCC0 is high and goes high impedance when VCC0 is low.
8	—	DRV5	Open-drain power MOSFET gate-driver output used to switch the slot VCC supply voltage (see Table 3 in *Detailed Description*).
9	—	DRV3	Open-drain power MOSFET gate-driver output used to switch the slot VCC supply voltage (see Table 3 in *Detailed Description*).
10	—	$\overline{SHDN}$	Logic-level shutdown input. When $\overline{SHDN}$ is low, DRV3 and DRV5 sink current regardless of the state of VCC0 and VCC1. When $\overline{SHDN}$ is high, DRV3 and DRV5 are controlled by VCC0 and VCC1.
11	—	BVPP	Switched output, controlled by BVPP1 and BVPP0, that outputs 0V, +5V, or +12V. BVPP can also be programmed to go high impedance (see Table 2 in *Detailed Description*).
12	6	AVPP	Switched output, controlled by AVPP1 and AVPP0, that outputs 0V, +5V, or +12V. AVPP can also be programmed to go high impedance (see Table 1 in *Detailed Description*).
13	7	VCCIN	+5V power input
14	8	VPPIN	+12V power input. VPPIN can have 0V or +5V applied as long as VCCIN > 2.85V.

Detailed Description

VPP Switching

The MAX613/MAX614 allow simple switching of PCMCIA card VPP to 0V, +5V, and +12V. On-chip power MOSFETs connect AVPP and BVPP to either GND, VCCIN, or VPPIN. The AVPP0 and AVPP1 control logic inputs determine AVPP's state. Likewise, BVPP0 and BVPP1 control BVPP. AVPP and BVPP can also be programmed to be high impedance.

Each PCMCIA card slot has two VPP voltage inputs labeled VPP1 and VPP2. Typically, VPP1 supplies the flash chips that store the low-order byte of the 16-bit words, and VPP2 supplies the chips that contain the high-order byte. Programming the high-order bytes separately from the low-order bytes may be necessary to minimize +12V current consumption. A single 8-bit flash chip typically requires at most 30mA of +12V VPP current during erase or programming.

Thus, systems with less than 60mA current capability from +12V cannot program two 8-bit flash chips simultaneously, and need separate controls for VPP1 and VPP2. Figure 1 shows an example of a power-control circuit using the MAX613 to control VPP1 and VPP2 separately. Figure 1's circuit uses a MAX662 charge-pump DC-DC converter to convert +5V to +12V at 30mA output current capability without an inductor. When higher VPP current is required, the MAX734 can supply 120mA.

Use the MAX614 for single-slot applications that do not require a separate VPP1 and VPP2. Figure 2 shows the MAX614 interfaced to the Vadem VG-465 single-slot controller.

To prevent VPP overshoot resulting from parasitic inductance in the +12V supply, the VPPIN bypass capacitor's value must be at least 10 times greater than the capacitance from AVPP or BVPP to GND; the AVPP and BVPP bypass capacitors must be at least 0.01µF.

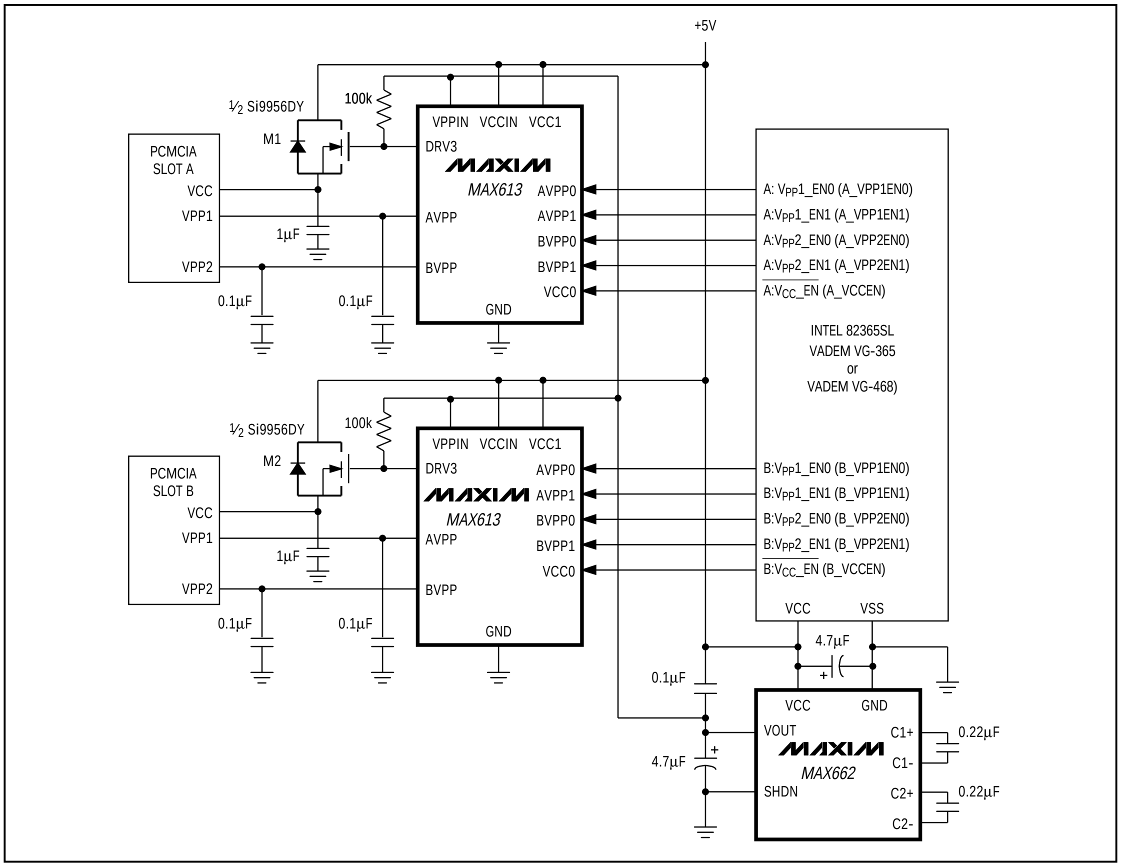


Figure 1. MAX613 Dual Slot, Separate VPP1 and VPP2, 5V Only VCC Operating Circuit

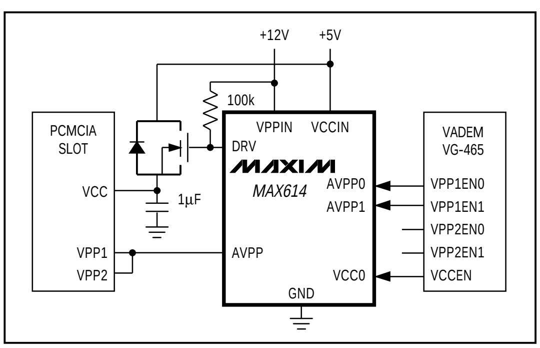


Figure 2. MAX614 Single-Slot Application

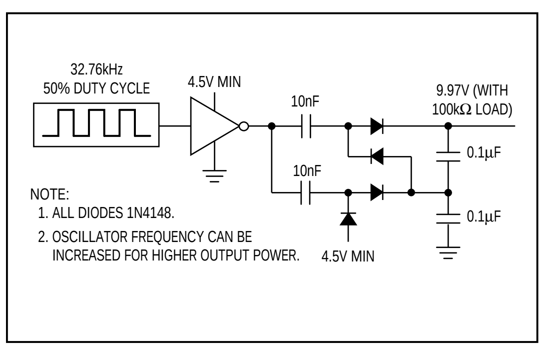


Figure 3. Charge Pump

VCC Switching

The MAX613/MAX614 contain level shifters that simplify driving external power MOSFETs to switch PCMCIA card VCC. While a PCMCIA card is being inserted into the socket, the VCC pins on the card edge connector should be powered down to 0V to prevent "hot insertion" that may damage the PCMCIA card. The MAX613/MAX614 MOSFET drivers are open drain. Their rise time is controlled by an external pull-up resistor, allowing slow turn-on of VCC power to the PCMCIA card.

The DRV3 and DRV5 pins on the MAX613 and the DRV pin on the MAX614 are open-drain outputs pulled down with internal N-channel devices. The gate drive to these internal N-channel devices is powered from VCCIN, regardless of VPPIN's voltage. If VCCIN is left unconnected or less than 2V is applied to VCCIN, the DRV3/DRV5/DRV gate drivers will not sink current.

To switch VCC (M1 and M2 in Figure 1), use external N-channel power MOSFETs. M1 and M2 should be logic-level N-channel power MOSFETs with low on resistance. The Motorola MTP3055EL and Siliconix Si9956DY MOSFETs are both good choices. Turn on M1 and M2 by pulling their gates above +5V. With the gates pulled up to VPPIN as shown in Figure 1, VPPIN should be at least 10V so that with VCC = 5.5V, M1 and M2 have at least 4.5V of gate drive.

Table 1. AVPP Control Logic

LOGIC INPUT		OUTPUT
AVPP1	AVPP0	AVPP
0	0	0V
0	1	VCCIN
1	0	VPPIN
1	1	HI-Z

Table 2. BVPP Control Logic

LOGIC INPUT		OUTPUT
BVPP1	BVPP0	BVPP
0	0	0V
0	1	VCCIN
1	0	VPPIN
1	1	HI-Z

Table 3. MAX613 DRV3 and DRV5 Control Logic ($\overline{\text{SHDN}}$ = VCCIN)

LOGIC INPUT		OUTPUT	
VCC1	VCC0	DRV3	DRV5
0	0	0V	0V
0	1	HI-Z	0V
1	0	0V	HI-Z
1	1	0V	0V

The gates of M1 and M2 can be pulled up to any 10V to 20V source, and do not need to be pulled up to VPPIN. Typically, the +12V used for VPPIN is supplied from a +5V to +12V switching regulator. To save power, the +5V to +12V switching regulator can be shut down when not using the VPP programming voltage, allowing VPPIN to fall below +5V.

In this case, M1 and M2 should not be pulled up to VPPIN, since M1 and M2 cannot be turned on reliably when VPPIN falls below +10V. Any clock source can be used to generate a high-side gate-drive voltage by using capacitors and diodes to build an inexpensive charge pump. Figure 3 shows a charge-pump circuit that generates 10V from a +5V logic clock source.

Applications Information

The MAX613 contains all the gate drivers and switching circuitry needed to support a +3.3V/+5V VCC PCMCIA slot with minimal external components. Figure 4 shows the analog power control necessary to support two dual voltage PCMCIA slots. The A:VCC and B:VCC pins on the Intel 82365SL DF power the drivers for the control signals that directly connect to the PCMCIA card.

A 3.3V card needs 3.3V logic-level control signals and the capability to program VPP1 and VPP2 to 3.3V. The MAX613's VCCIN is switched with slot VCC, so AVPP0 = 1 and AVPP1 = 0 causes AVPP = slot VCC. Likewise, A:VCC and B:VCC are connected to VCCIN, so the Intel 82365SL DF control signals to the PCMCIA card are the right logic levels.

PCMCIA card interface controllers other than the Intel 82365SL DF can be used with Figure 4's circuit. Table 4 shows the pins on the Cirrus Logic CL-PD6720 that perform the same function as the Intel 82365SL DF pins.

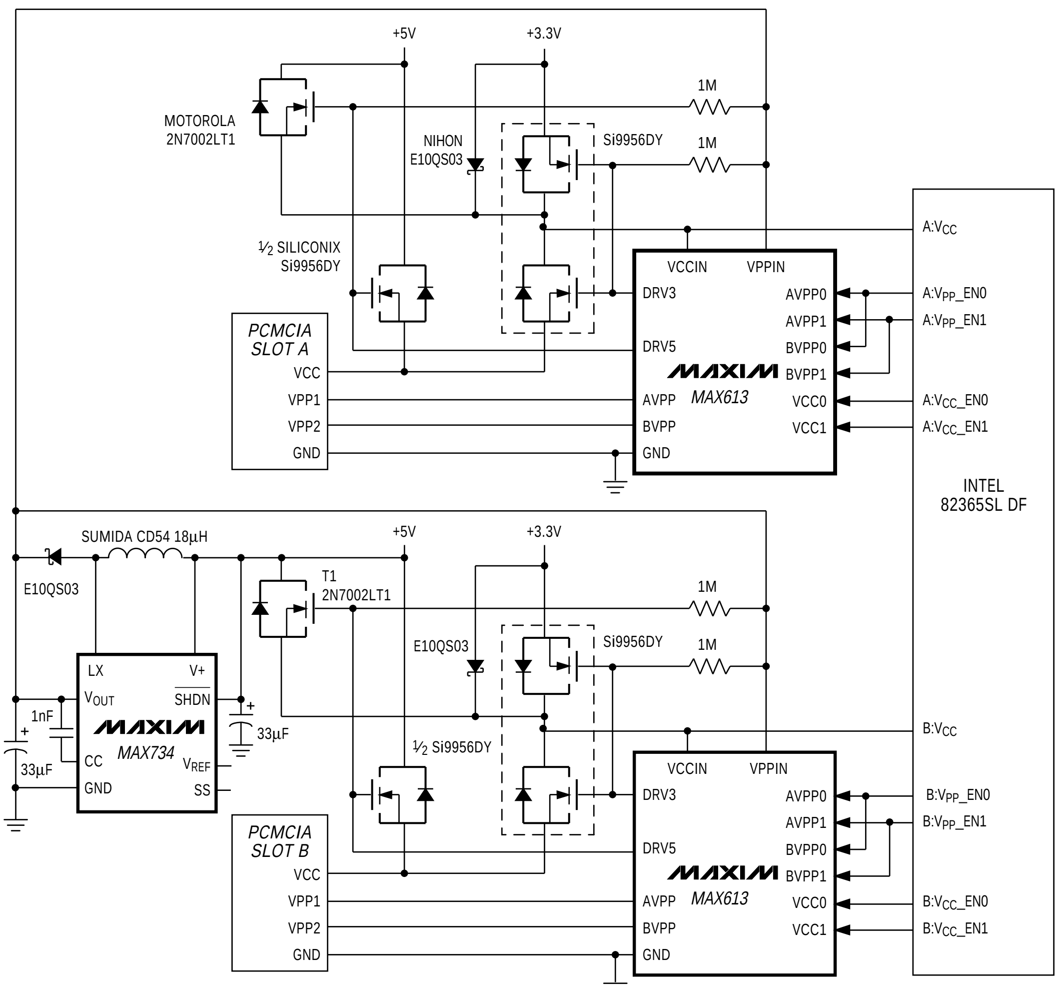


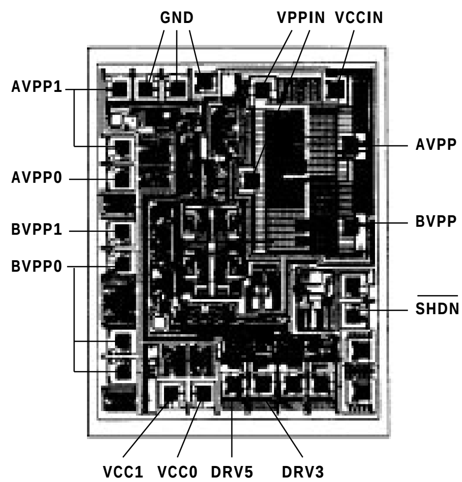
Figure 4. Mixed 3.3V/5V VCC Application Circuit

Table 4. Interchangeable Interface Controllers

INTEL	CIRRUS LOGIC
82365SL DF	CL-PD6720
A:V_{CC}	A_SLOT_VCC
A:V_{PP}_EN0	A_VPP_VCC
A:V_{PP}_EN1	A_VPP_PGM
A:V_{CC}_EN0	A_-VCC_5
A:V_{CC}_EN1	A_-VCC_3
B:V_{CC}	B_SLOT_VCC
V:V_{PP}_EN0	B_VPP_VCC
B:V_{PP}_EN1	B_VPP_PGM
B:V_{CC}_EN0	B_-VCC_5
B:V_{CC}_EN1	B_-VCC_3

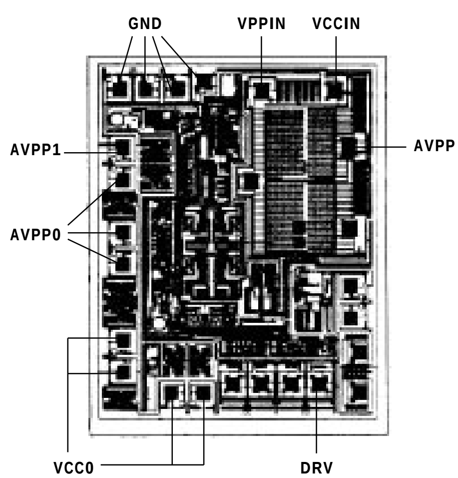
Chip Topographies

MAX613



TRANSISTOR COUNT: 982;
SUBSTRATE CONNECTED TO GND.

MAX614



TRANSISTOR COUNT: 982;
SUBSTRATE CONNECTED TO GND.