1 MC145151-2 Parallel-Input (Interfaces with Single-Modulus Prescalers)

The MC145151-2 is programmed by 14 parallel-input data lines for the N counter and three input lines for the R counter. The device features consist of a reference oscillator, selectable-reference divider, digital-phase detector, and 14-bit programmable divide-by-N counter.

The MC145151-2 is an improved-performance drop-in replacement for the MC145151-1. The power consumption has decreased and ESD and latch-up performance have improved.

1.1 Features

- Operating Temperature Range: - 40 to 85°C
- Low Power Consumption Through Use of CMOS Technology
- 3.0 to 9.0 V Supply Range
- On- or Off-Chip Reference Oscillator Operation
- Lock Detect Signal
- ÷ N Counter Output Available
- Single Modulus/Parallel Programming
- 8 User-Selectable ÷ R Values: 8, 128, 256, 512, 1024, 2048, 2410, 8192
- ÷ N Range = 3 to 16383
- “Linearized” Digital Phase Detector Enhances Transfer Function Linearity
- Two Error Signal Options: Single-Ended (Three-State) or Double-Ended
- Chip Complexity: 8000 FETs or 2000 Equivalent Gates

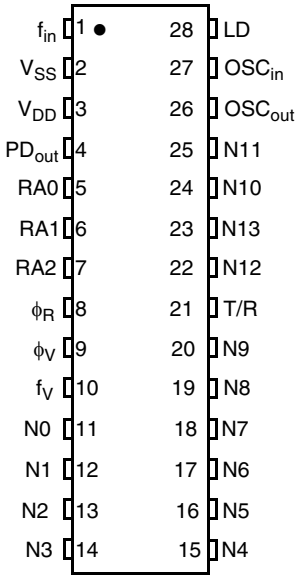
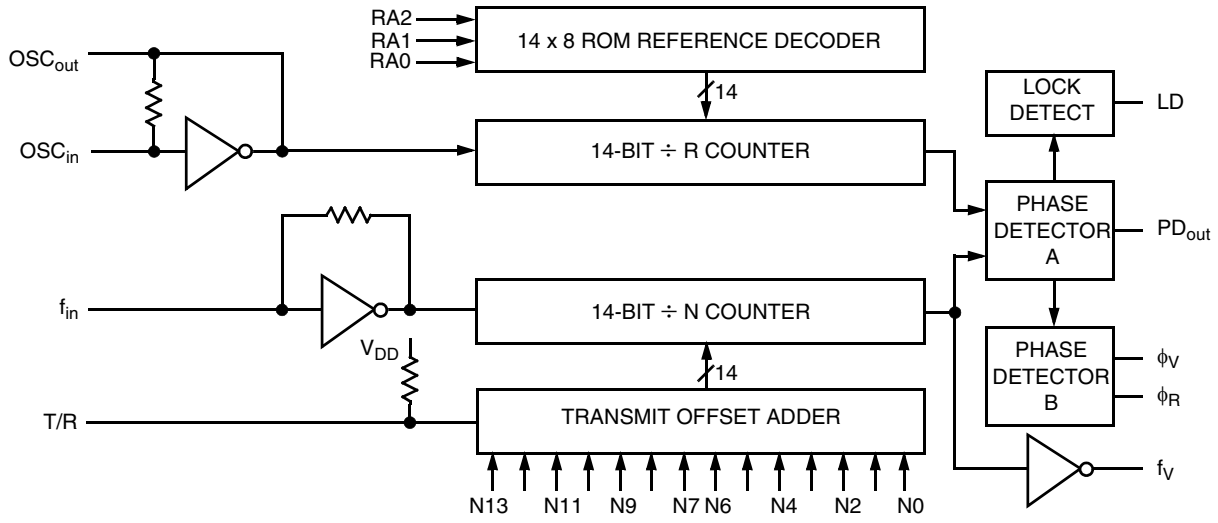


Figure 1. MC145151-2 Pin Assignment



NOTE: N0 - N13 inputs and inputs RA0, RA1, and RA2 have pull-up resistors that are not shown.

Figure 2. MC145151-2 Block Diagram

1.2 Pin Descriptions

1.2.1 Input Pins

f_{in}
Frequency Input (Pin 1)

Input to the ÷N portion of the synthesizer. f_{in} is typically derived from loop VCO and is ac coupled into the device. For larger amplitude signals (standard CMOS logic levels) dc coupling may be used.

RA0 - RA2
Reference Address Inputs (Pins 5, 6, 7)

These three inputs establish a code defining one of eight possible divide values for the total reference divider, as defined by the table below.

Pull-up resistors ensure that inputs left open remain at a logic 1 and require only a SPST switch to alter data to the zero state.

Reference Address Code			Total Divide Value
RA2	RA1	RA0	
0	0	0	8
0	0	1	128
0	1	0	256
0	1	1	512
1	0	0	1024
1	0	1	2048
1	1	0	2410
1	1	1	8192

N0 - N11
N Counter Programming Inputs (Pins 11 - 20, 22 - 25)

These inputs provide the data that is preset into the ÷N counter when it reaches the count of zero. N0 is the least significant and N13 is the most significant. Pull-up resistors ensure that inputs left open remain at a logic 1 and require only an SPST switch to alter data to the zero state.

T/R
Transmit/Receive Offset Adder Input (Pin 21)

This input controls the offset added to the data provided at the N inputs. This is normally used for offsetting the VCO frequency by an amount equal to the IF frequency of the transceiver. This offset is fixed at 856 when T/R is low and gives no offset when T/R is high. A pull-up resistor ensures that no connection will appear as a logic 1 causing no offset addition.

OSC_{in}, OSC_{out}
Reference Oscillator Input/Output (Pins 27, 26)

These pins form an on-chip reference oscillator when connected to terminals of an external parallel resonant crystal. Frequency setting capacitors of appropriate value must be connected from OSC_{in} to ground and OSC_{out} to ground. OSC_{in} may also serve as the input for an externally-generated reference signal. This signal is typically ac coupled to OSC_{in}, but for larger amplitude signals (standard CMOS logic levels) dc coupling may also be used. In the external reference mode, no connection is required to OSC_{out}.

1.2.2 Output Pins

PD_{out}
Phase Detector A Output (Pin 4)

Three-state output of phase detector for use as loop-error signal. Double-ended outputs are also available for this purpose (see ϕ_V and ϕ_R).

Frequency $f_V > f_R$ or f_V Leading: Negative Pulses

Frequency $f_V < f_R$ or f_V Lagging: Positive Pulses

Frequency $f_V = f_R$ and Phase Coincidence: High-Impedance State

ϕ_R, ϕ_V
Phase Detector B Outputs (Pins 8, 9)

These phase detector outputs can be combined externally for a loop-error signal. A single-ended output is also available for this purpose (see **PD_{out}**).

If frequency f_V is greater than f_R or if the phase of f_V is leading, then error information is provided by ϕ_V pulsing low. ϕ_R remains essentially high.

If the frequency f_V is less than f_R or if the phase of f_V is lagging, then error information is provided by ϕ_R pulsing low. ϕ_V remains essentially high.

If the frequency of $f_V = f_R$ and both are in phase, then both ϕ_V and ϕ_R remain high except for a small minimum time period when both pulse low in phase.

f_V
N Counter Output (Pin 10)

This is the buffered output of the ÷ N counter that is internally connected to the phase detector input. With this output available, the ÷ N counter can be used independently.

LD
Lock Detector Output (Pin 28)

Essentially a high level when loop is locked (f_R, f_V of same phase and frequency). Pulses low when loop is out of lock.

1.2.3 Power Supply

V_{DD}
Positive Power Supply (Pin 3)

The positive power supply potential. This pin may range from + 3 to + 9 V with respect to V_{SS}.

V_{SS}
Negative Power Supply (Pin 2)

The most negative supply potential. This pin is usually ground.

1.3 Typical Applications

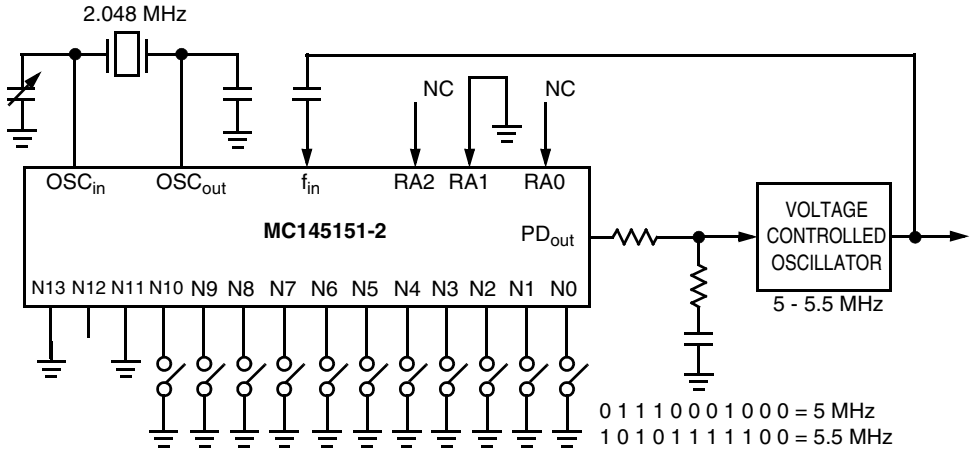
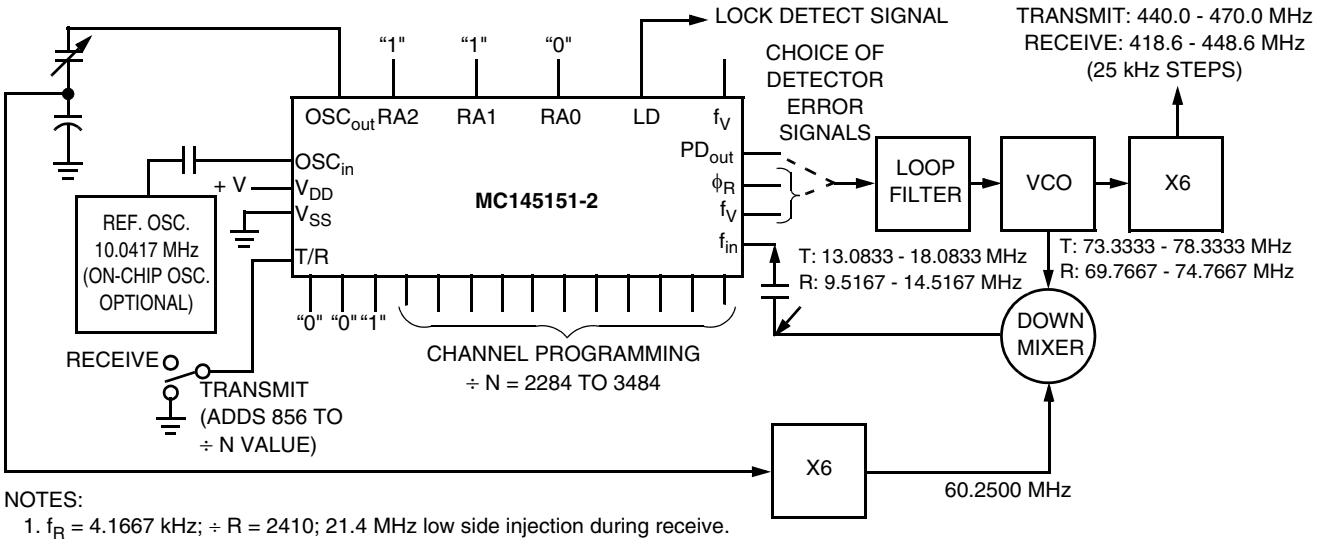


Figure 3. 5 MHz to 5.5 MHz Local Oscillator Channel Spacing = 1 kHz



NOTES:
1. f_R = 4.1667 kHz; ÷ R = 2410; 21.4 MHz low side injection during receive.
2. Frequency values shown are for the 440 - 470 MHz band. Similar implementation applies to the 406 - 440 MHz band. For 470 - 512 MHz, consider reference oscillator frequency X9 for mixer injection signal (90.3750 MHz).

Figure 4. Synthesizer for Land Mobile Radio UHF Bands

2 MC145152-2 Parallel-Input (Interfaces with Dual-Modulus Prescalers)

The MC145152-2 is programmed by sixteen parallel inputs for the N and A counters and three input lines for the R counter. The device features consist of a reference oscillator, selectable-reference divider, two-output phase detector, 10-bit programmable divide-by-N counter, and 6-bit programmable divide-by-A counter.

The MC145152-2 is an improved-performance drop-in replacement for the MC145152-1. Power consumption has decreased and ESD and latch-up performance have improved.

2.1 Features

- Operating Temperature Range: -40 to 85°C
- Low Power Consumption Through Use of CMOS Technology
- 3.0 to 9.0 V Supply Range
- On- or Off-Chip Reference Oscillator Operation
- Lock Detect Signal
- Dual Modulus/Parallel Programming
- 8 User-Selectable ÷ R Values: 8, 64, 128, 256, 512, 1024, 1160, 2048
- ÷ N Range = 3 to 1023, ÷ A Range = 0 to 63
- Chip Complexity: 8000 FETs or 2000 Equivalent Gates

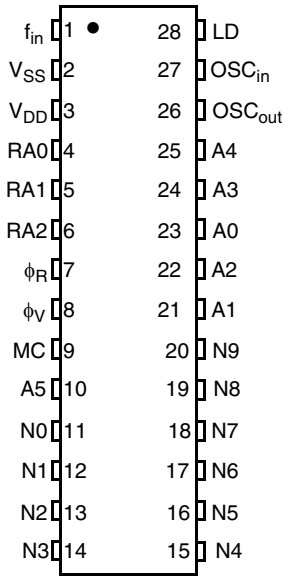
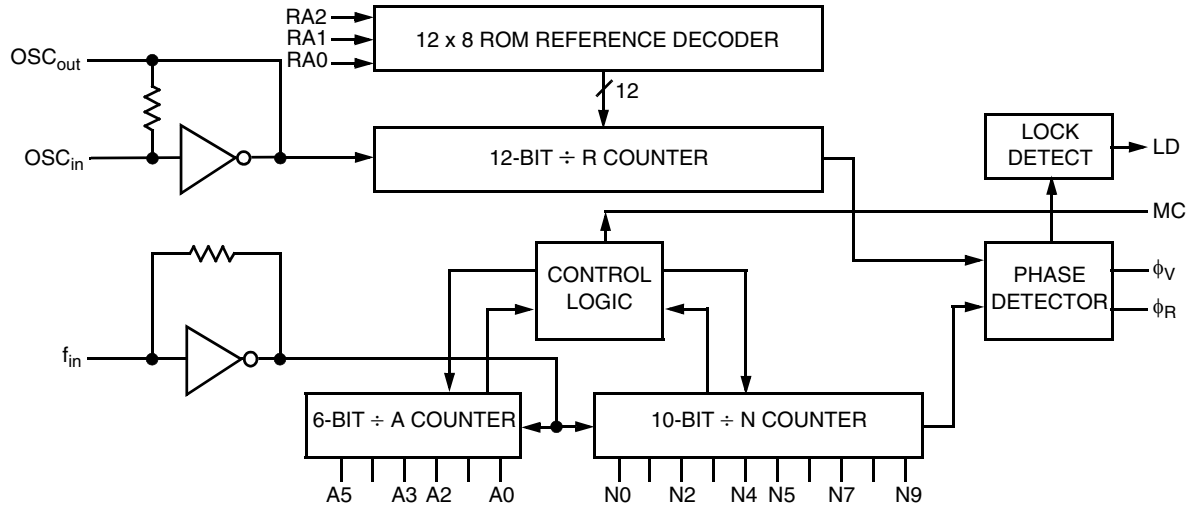


Figure 5. MC145152-2 Pin Assignment



NOTE: N0 - N9, A0 - A5, and RA0 - RA2 have pull-up resistors that are not shown.

Figure 6. MC145152-2 Block Diagram

2.2 Pin Descriptions

2.2.1 Input Pins

f_{in}
Frequency Input (Pin 1)

Input to the positive edge triggered ÷ N and ÷ A counters. f_{in} is typically derived from a dual-modulus prescaler and is AC coupled into the device. For larger amplitude signals (standard CMOS logic levels) DC coupling may be used.

RA0, RA1, RA2
Reference Address Inputs (Pins 4, 5, 6)

These three inputs establish a code defining one of eight possible divide values for the total reference divider. The total reference divide values are as follows:

Reference Address Code			Total Divide Value
RA2	RA1	RA0	
0	0	0	8
0	0	1	64
0	1	0	128
0	1	1	256
1	0	0	512
1	0	1	1024
1	1	0	1160
1	1	1	2048

N0 - N9
N Counter Programming Inputs (Pins 11 - 20)

The N inputs provide the data that is preset into the ÷ N counter when it reaches the count of 0. N0 is the least significant digit and N9 is the most significant. Pull-up resistors ensure that inputs left open remain at a logic 1 and require only a SPST switch to alter data to the zero state.

A0 - A5
A Counter Programming Inputs
(Pins 23, 21, 22, 24, 25, 10)

The A inputs define the number of clock cycles of f_{in} that require a logic 0 on the MC output (see Section 4.3, “Dual-Modulus Prescaling,” on page 21). The A inputs all have internal pull-up resistors that ensure that inputs left open will remain at a logic 1.

OSC_{in}, OSC_{out}
Reference Oscillator Input/Output (Pins 27, 26)

These pins form an on-chip reference oscillator when connected to terminals of an external parallel resonant crystal. Frequency setting capacitors of appropriate value must be connected from OSC_{in} to ground and OSC_{out} to ground. OSC_{in} may also serve as the input for an externally-generated reference signal. This signal is typically ac coupled to OSC_{in}, but for larger amplitude signals (standard CMOS logic levels) dc coupling may also be used. In the external reference mode, no connection is required to OSC_{out}.

2.2.2 Output Pins

ϕ_R, ϕ_V
Phase Detector B Outputs (Pins 7, 8)

These phase detector outputs can be combined externally for a loop-error signal.

If the frequency f_V is greater than f_R or if the phase of f_V is leading, then error information is provided by ϕ_V pulsing low. ϕ_R remains essentially high.

If the frequency f_V is less than f_R or if the phase of f_V is lagging, then error information is provided by ϕ_R pulsing low. ϕ_V remains essentially high.

If the frequency of $f_V = f_R$ and both are in phase, then both ϕ_V and ϕ_R remain high except for a small minimum time period when both pulse low in phase.

MC
Dual-Modulus Prescale Control Output (Pin 9)

Signal generated by the on-chip control logic circuitry for controlling an external dual-modulus prescaler. The MC level will be low at the beginning of a count cycle and will remain low until the ÷ A counter has counted down from its programmed value. At this time, MC goes high and remains high until the ÷ N counter has counted the rest of the way down from its programmed value (N - A additional counts since both ÷ N and ÷ A are counting down during the first portion of the cycle). MC is then set back low, the counters preset to their respective programmed values, and the above sequence repeated. This provides for a total programmable divide value (N_T) = N • P + A where P and P + 1 represent the dual-modulus prescaler

divide values respectively for high and low MC levels, N the number programmed into the ÷ N counter, and A the number programmed into the ÷ A counter.

LD
Lock Detector Output (Pin 28)

Essentially a high level when loop is locked (f_R, f_V of same phase and frequency). Pulses low when loop is out of lock.

2.2.3 Power Supply

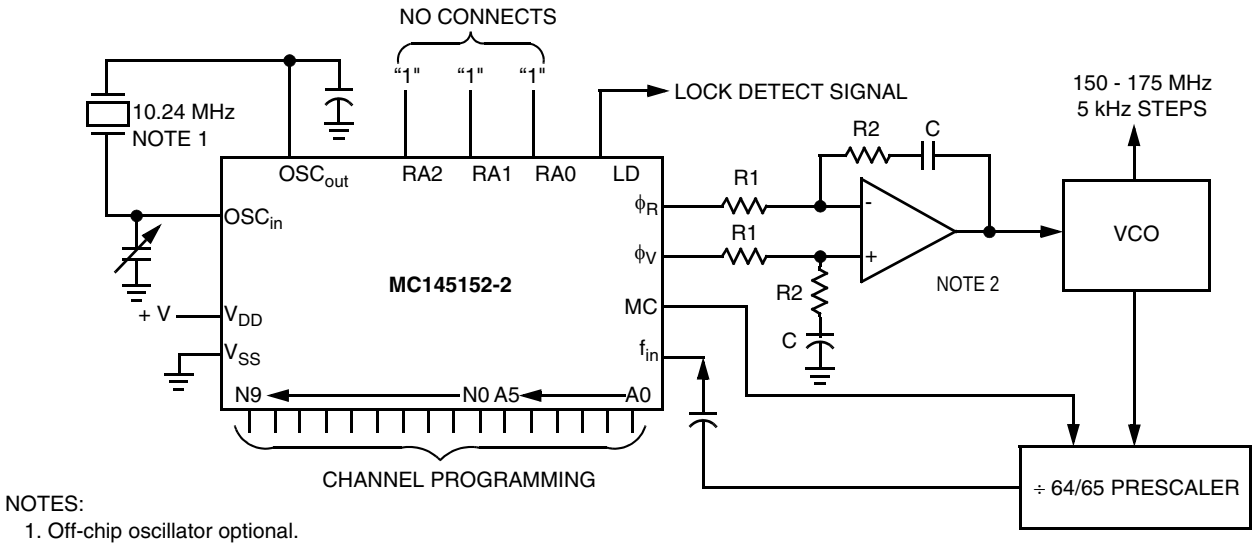
V_{DD}
Positive Power Supply (Pin 3)

The positive power supply potential. This pin may range from + 3 to + 9 V with respect to V_{SS}.

V_{SS}
Negative Power Supply (Pin 2)

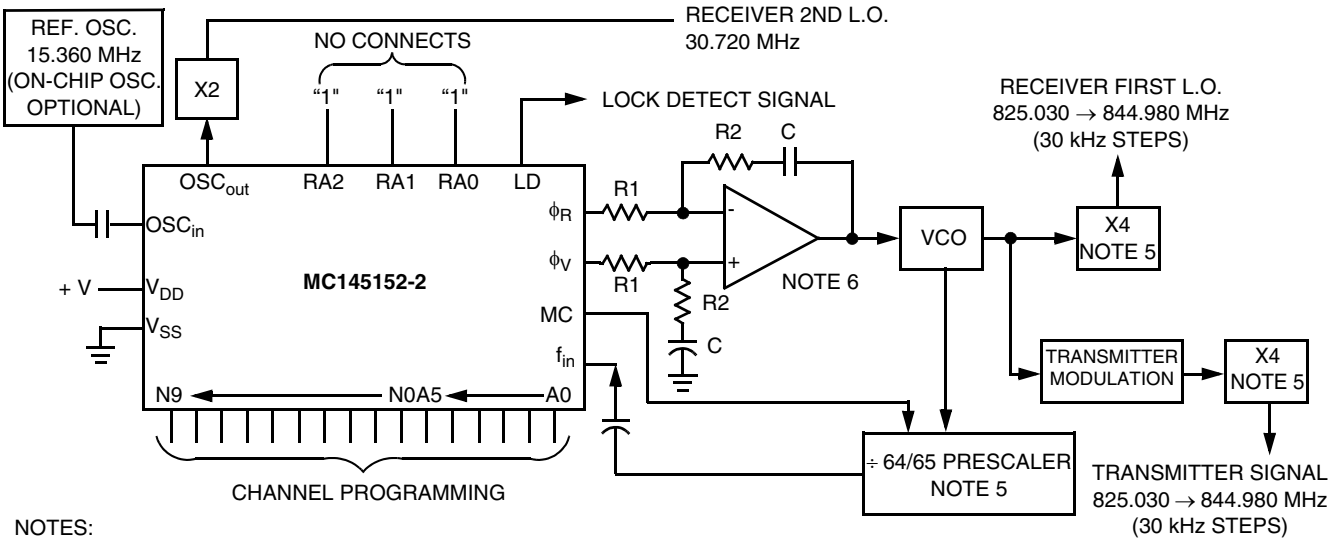
The most negative supply potential. This pin is usually ground.

2.3 Typical Applications



NOTES:
1. Off-chip oscillator optional.
2. The ϕ_R and ϕ_V outputs are fed to an external combiner/loop filter. See the Phase-Locked Loop - Low-Pass Filter Design page for additional information. The ϕ_R and ϕ_V outputs swing rail-to-rail. Therefore, the user should be careful not to exceed the common mode input range of the op amp used in the combiner/loop filter.

Figure 7. Synthesizer for Land Mobile Radio VHF Bands



NOTES:

1. Receiver 1st I.F. = 45 MHz, low side injection; Receiver 2nd I.F. = 11.7 MHz, low side injection.
2. Duplex operation with 45 MHz receiver/transmit separation.
3. f_R = 7.5 kHz; ÷ R = 2048.
4. N_{total} = N • 64 + A = 27501 to 28166; N = 429 to 440; A = 0 to 63.
5. High frequency prescalers may be used for higher frequency VCO and f_{ref} implementations.
6. The ϕ_R and ϕ_V outputs are fed to an external combiner/loop filter. See the Phase-Locked Loop - Low-Pass Filter Design page for additional information. The ϕ_R and ϕ_V outputs swing rail-to-rail. Therefore, the user should be careful not to exceed the common mode input range of the op amp used in the combiner/loop filter.

Figure 8. 666-Channel Computer-Controlled, Mobile Radiotelephone Synthesizer for 800 MHz Cellular Radio Systems

3 MC145151-2 and MC145152-2 Electrical Characteristics

These devices contain protection circuitry to protect against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to these high-impedance circuits. For proper operation, V_{in} and V_{out} should be constrained to the range $V_{SS} \le (V_{in}$ or $V_{out}) \le V_{DD}$ except for SW1 and SW2.

SW1 and SW2 can be tied through external resistors to voltages as high as 15 V, independent of the supply voltage.

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either V_{SS} or V_{DD}), except for inputs with pull-up devices. Unused outputs must be left open.

Table 1. Maximum Ratings[1]
(Voltages Referenced to VSS)

Ratings	Symbol	Value	Unit
DC Supply Voltage	V_{DD}	- 0.5 to + 10.0	V
Input or Output Voltage (DC or Transient) except SW1, SW2	V_{in}, V_{out}	- 0.5 to V_{DD} + 0.5	V
Output Voltage (DC or Transient), SW1, SW2 ($R_{pull\text{-}up}$ = 4.7 kΩ)	V_{out}	- 0.5 to + 15	V
Input or Output Current (DC or Transient), per Pin	I_{in}, I_{out}	± 10	mA
Supply Current, V_{DD} or V_{SS} Pins	I_{DD}, I_{SS}	± 30	mA
Power Dissipation, per Package†	P_D	500	mW
Storage Temperature	T_{stg}	-65 to + 150	°C
Lead Temperature, 1 mm from Case for 10 seconds	T_L	260	°C

[1] Maximum Ratings are those values beyond which damage to the device may occur. Functional operation should be restricted to the limits in the Electrical Characteristics tables or Pin Descriptions section.

† Power Dissipation Temperature Derating:
Plastic DIP: - 12 mW/°C from 65 to 85°C
SOG Package: - 7 mW/°C from 65 to 85°C

Table 2. Electrical Characteristics
(Voltages Referenced to V_{SS})

Symbol	Parameter	Test Condition	V_{DD} V	- 40°C		25°C		85°C		Unit
				Min	Max	Min	Max	Min	Max	
V_{DD}	Power Supply Voltage Range		-	3	9	3	9	3	9	V
I_{ss}	Dynamic Supply Current	$f_{in} = OSC_{in}$ = 10 MHz, 1 V p-p ac coupled sine wave R = 128, A = 32, N = 128	3 5 9	- - -	3.5 10 30	- - -	3 7.5 24	- - -	3 7.5 24	mA
I_{SS}	Quiescent Supply Current (not including pull-up current component)	$V_{in} = V_{DD}$ or V_{SS} I_{out} = 0 μA	3 5 9	- - -	800 1200 1600	- - -	800 1200 1600	- - -	1600 2400 3200	μA
V_{in}	Input Voltage - f_{in}, OSC_{in}	Input ac coupled sine wave	-	500	-	500	-	500	-	mV p-p
V_{IL}	Low-Level Input Voltage - f_{in}, OSC_{in}	$V_{out} \geq$ 2.1 V Input dc $V_{out} \geq$ 3.5 V coupled $V_{out} \geq$ 6.3 V square wave	3 5 9	- - -	0 0 0	- - -	0 0 0	- - -	0 0 0	V
V_{IH}	High-Level Input Voltage - f_{in}, OSC_{in}	$V_{out} \leq$ 0.9 V Input dc $V_{out} \leq$ 1.5 V coupled $V_{out} \leq$ 2.7 V square wave	3 5 9	3.0 5.0 9.0	- - -	3.0 5.0 9.0	- - -	3.0 5.0 9.0	- - -	V
V_{IL}	Low-Level Input Voltage - except f_{in}, OSC_{in}		3 5 9	- - -	0.9 1.5 2.7	- - -	0.9 1.5 2.7	- - -	0.9 1.5 2.7	V
V_{IH}	High-Level Input Voltage - except f_{in}, OSC_{in}		3 5 9	2.1 3.5 6.3	- - -	2.1 3.5 6.3	- - -	2.1 3.5 6.3	- - -	V
I_{in}	Input Current (f_{in}, OSC_{in})	$V_{in} = V_{DD}$ or V_{SS}	9	± 2	± 50	± 2	± 25	± 2	± 22	μA
I_{IL}	Input Leakage Current (Data, CLK, ENB - without pull-ups)	$V_{in} = V_{SS}$	9	-	- 0.3	-	- 0.1	-	- 1.0	μA
I_{IH}	Input Leakage Current (all inputs except f_{in}, OSC_{in})	$V_{in} = V_{DD}$	9	-	0.3	-	0.1	-	1.0	μA

Table 3. DC Electrical Characteristics

Symbol	Parameter	Test Condition	V_{DD} V	- 40°C		25°C		85°C		Unit
				Min	Max	Min	Max	Min	Max	
I_{IL}	Pull-up Current (all inputs with pull-ups)	$V_{in} = V_{SS}$	9	- 20	- 400	- 20	- 200	- 20	- 170	μA
C_{in}	Input Capacitance		-	-	10	-	10	-	10	pF
V_{OL}	Low-Level Output Voltage - OSC_{out}	$I_{out} \approx 0$ μA $V_{in} = V_{DD}$	3 5 9	- - -	0.9 1.5 2.7	- - -	0.9 1.5 2.7	- - -	0.9 1.5 2.7	V
V_{OH}	High-Level Output Voltage - OSC_{out}	$I_{out} \approx 0$ μA $V_{in} = V_{SS}$	3 5 9	2.1 3.5 6.3	- - -	2.1 3.5 6.3	- - -	2.1 3.5 6.3	- - -	V
V_{OL}	Low-Level Output Voltage - Other Outputs	$I_{out} \approx 0$ μA	3 5 9	- - -	0.05 0.05 0.05	- - -	0.05 0.05 0.05	- - -	0.05 0.05 0.05	V
V_{OH}	High-Level Output Voltage - Other Outputs	$I_{out} \approx 0$ μA	3 5 9	2.95 4.95 8.95	- - -	2.95 4.95 8.95	- - -	2.95 4.95 8.95	- - -	V
$V_{(BR)DSS}$	Drain-to-Source Breakdown Voltage - SW1, SW2	$R_{pull-up} = 4.7$ kΩ	-	15	-	15	-	15	-	V
I_{OL}	Low-Level Sinking Current - MC	$V_{out} = 0.3$ V $V_{out} = 0.4$ V $V_{out} = 0.5$ V	3 5 9	1.30 1.90 3.80	- - -	1.10 1.70 3.30	- - -	0.66 1.08 2.10	- - -	mA
I_{OH}	High-Level Sourcing Current - MC	$V_{out} = 2.7$ V $V_{out} = 4.6$ V $V_{out} = 8.5$ V	3 5 9	- 0.60 - 0.90 - 1.50	- - -	- 0.50 - 0.75 - 1.25	- - -	- 0.30 - 0.50 - 0.80	- - -	mA
I_{OL}	Low-Level Sinking Current - LD	$V_{out} = 0.3$ V $V_{out} = 0.4$ V $V_{out} = 0.5$ V	3 5 9	0.25 0.64 1.30	- - -	0.20 0.51 1.00	- - -	0.15 0.36 0.70	- - -	mA
I_{OH}	High-Level Sourcing Current - LD	$V_{out} = 2.7$ V $V_{out} = 4.6$ V $V_{out} = 8.5$ V	3 5 9	- 0.25 - 0.64 - 1.30	- - -	- 0.20 - 0.51 - 1.00	- - -	- 0.15 - 0.36 - 0.70	- - -	mA
I_{OL}	Low-Level Sinking Current - SW1, SW2	$V_{out} = 0.3$ V $V_{out} = 0.4$ V $V_{out} = 0.5$ V	3 5 9	0.80 1.50 3.50	- - -	0.48 0.90 2.10	- - -	0.24 0.45 1.05	- - -	mA
I_{OL}	Low-Level Sinking Current - Other Outputs	$V_{out} = 0.3$ V $V_{out} = 0.4$ V $V_{out} = 0.5$ V	3 5 9	0.44 0.64 1.30	- - -	0.35 0.51 1.00	- - -	0.22 0.36 0.70	- - -	mA
I_{OH}	High-Level Sourcing Current - Other Outputs	$V_{out} = 2.7$ V $V_{out} = 4.6$ V $V_{out} = 8.5$ V	3 5 9	- 0.44 - 0.64 - 1.30	- - -	- 0.35 - 0.51 - 1.00	- - -	- 0.22 - 0.36 - 0.70	- - -	mA
I_{OZ}	Output Leakage Current - PD_{out}	$V_{out} = V_{DD}$ or V_{SS} Output in Off State	9	-	± 0.3	-	± 0.1	-	± 1.0	μA
I_{OZ}	Output Leakage Current - SW1, SW2	$V_{out} = V_{DD}$ or V_{SS} Output in Off State	9	-	± 0.3	-	± 0.1	-	± 3.0	μA
C_{out}	Output Capacitance - PD_{out}	PD_{out} - Three-State	-	-	10	-	10	-	10	pF

Table 4. AC Electrical Characteristics
(C_L = 50 pF, Input $t_r = t_f$ = 10 ns)

Symbol	Parameter	V_{DD} V	Guaranteed Limit 25°C	Guaranteed Limit -40 to 85°C	Unit
t_{PLH}, t_{PHL}	Maximum Propagation Delay, f_{in} to MC (Figure 9a and Figure 9d)	3 5 9	110 60 35	120 70 40	ns
t_{PHL}	Maximum Propagation Delay, ENB to SW1, SW2 (Figure 9a and Figure 9e)	3 5 9	160 80 50	180 95 60	ns
t_w	Output Pulse Width, ϕ_R, ϕ_V, and LD with f_R in Phase with f_V (Figure 9b and Figure 9d)	3 5 9	25 to 200 20 to 100 10 to 70	25 to 260 20 to 125 10 to 80	ns
t_{TLH}	Maximum Output Transition Time, MC (Figure 9c and Figure 9d)	3 5 9	115 60 40	115 75 60	ns
t_{THL}	Maximum Output Transition Time, MC (Figure 9c and Figure 9d)	3 5 9	60 34 30	70 45 38	ns
t_{TLH}, t_{THL}	Maximum Output Transition Time, LD (Figure 9c and Figure 9d)	3 5 9	180 90 70	200 120 90	ns
t_{TLH}, t_{THL}	Maximum Output Transition Time, Other Outputs (Figure 9c and Figure 9d)	3 5 9	160 80 60	175 100 65	ns

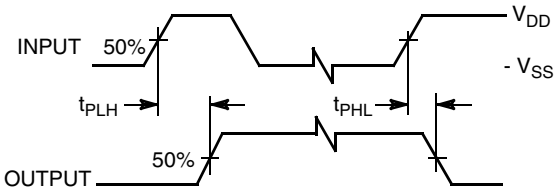
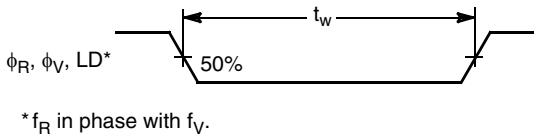


Figure 9a. Maximum Propagation Delay



*f_R in phase with f_V.

Figure 9b. Output Pulse Width

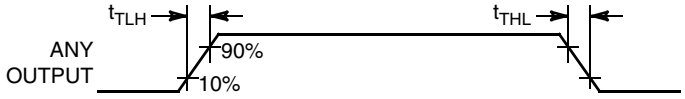
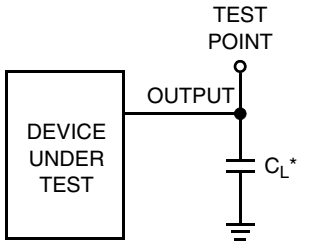
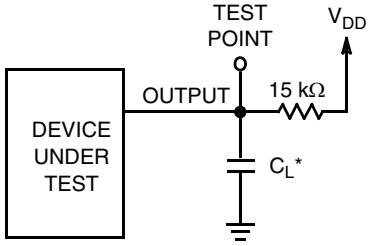


Figure 9c. Maximum Output Transition Time



*Includes all probe and fixture capacitance.

Figure 9d. Test Circuit



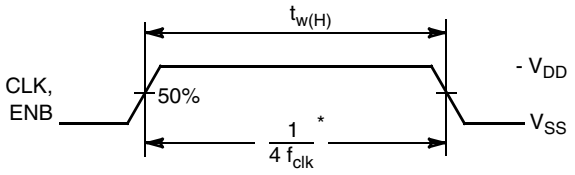
*Includes all probe and fixture capacitance.

Figure 9e. Test Circuit

Figure 9. Switching Waveforms

Table 5. Timing Requirements
(Input $t_r = t_f = 10$ ns unless otherwise indicated)

Symbol	Parameter	V_{DD} V	Guaranteed Limit 25°C	Guaranteed Limit - 40 to 85°C	Unit
f_{clk}	Serial Data Clock Frequency, Assuming 25% Duty Cycle NOTE: Refer to CLK $t_{w(H)}$ below (Figure 10a)	3 5 9	dc to 5.0 dc to 7.1 dc to 10	dc to 3.5 dc to 7.1 dc to 10	MHz
t_{su}	Minimum Setup Time, Data to CLK (Figure 10b)	3 5 9	30 20 18	30 20 18	ns
t_h	Minimum Hold Time, CLK to Data (Figure 10b)	3 5 9	40 20 15	40 20 15	ns
t_{su}	Minimum Setup Time, CLK to ENB (Figure 10b)	3 5 9	70 32 25	70 32 25	ns
t_{rec}	Minimum Recovery Time, ENB to CLK (Figure 10b)	3 5 9	5 10 20	5 10 20	ns
$t_{w(H)}$	Minimum Pulse Width, CLK and ENB (Figure 10a)	3 5 9	50 35 25	70 35 25	ns
t_r, t_f	Maximum Input Rise and Fall Times - Any Input (Figure 10c)	3 5 9	5 4 2	5 4 2	µs



*Assumes 25% Duty Cycle.

Figure 10a. Serial Data Clock Frequency and Minimum Pulse Width

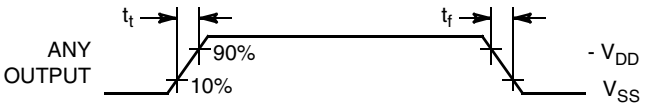


Figure 10c. Maximum Input Rise and Fall Times

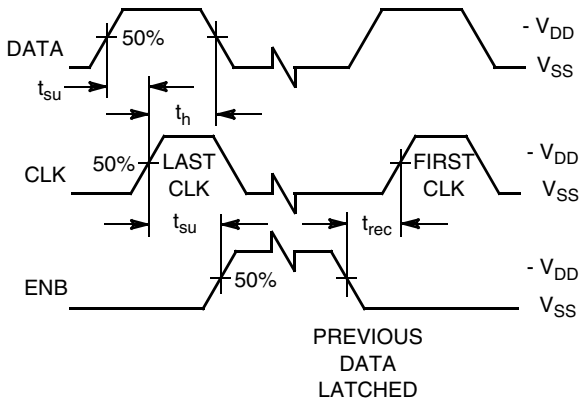


Figure 10b. Minimum Setup, Hold, and Recovery Times

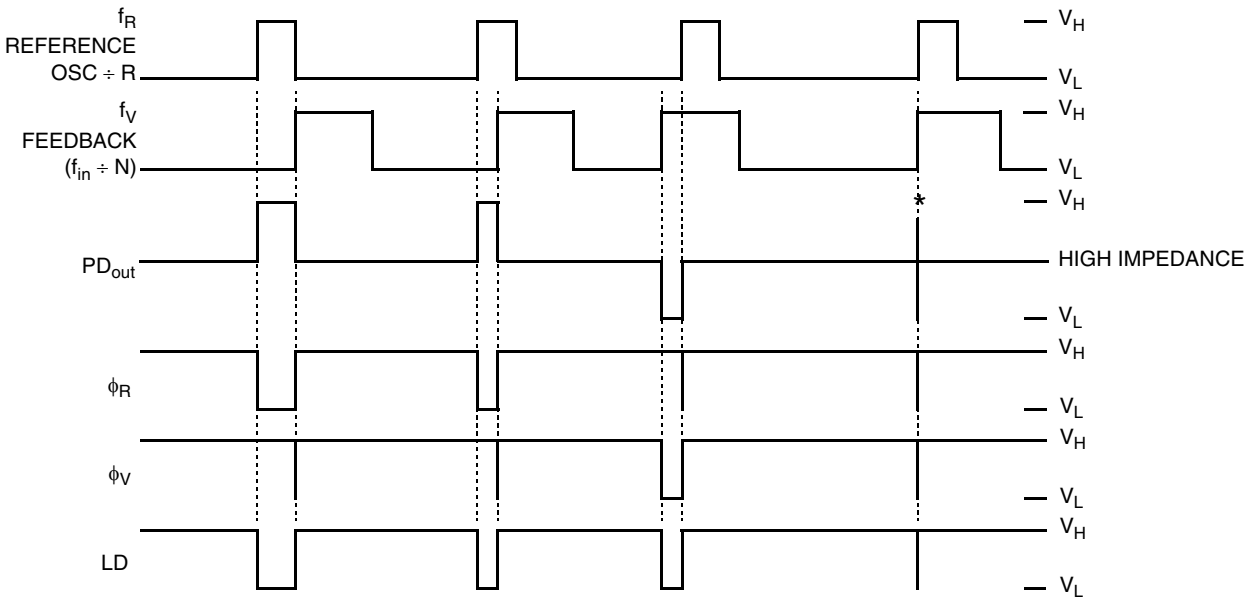
Figure 10. Switching Waveforms

Table 6. Frequency Characteristics

(Voltages References to V_{SS}, C_L = 50 pF, Input $t_r = t_f$ =10 ns unless otherwise indicated)

Symbol	Parameter	Test Condition	V_{DD} V	- 40°C		25°C		85°C		Unit
				Min	Max	Min	Max	Min	Max	
f_i	Input Frequency (f_{in}, OSC_{in})	R ≥ 8, A ≥ 0, N ≥ 8 V_{in} = 500 mV p-p ac coupled sine wave	3 5 9	- - -	6 15 15	- - -	6 15 15	- - -	6 15 15	MHz
		R ≥ 8, A ≥ 0, N ≥ 8 V_{in} = 1 V p-p ac coupled sine wave	3 5 9	- - -	12 22 25	- - -	12 20 22	- - -	7 20 22	MHz
		R ≥ 8, A ≥ 0, N ≥ 8 V_{in} = V_{DD} to V_{SS} dc coupled square wave	3 5 9	- - -	13 25 25	- - -	12 22 25	- - -	8 22 25	MHz

Note: Usually, the PLL's propagation delay from f_{in} to MC plus the setup time of the prescaler determines the upper frequency limit of the system. The upper frequency limit is found with the following formula: $f = P/(t_P + t_{set})$ where f is the upper frequency in Hz, P is the lower of the dual modulus prescaler ratios, t_P is the f_{in} to MC propagation delay in seconds, and t_{set} is the prescaler setup time in seconds. For example, with a 5 V supply, the f_{in} to MC delay is 70 ns. If the MC12028A prescaler is used, the setup time is 16 ns. Thus, if the 64/65 ratio is utilized, the upper frequency limit is $f = P/(t_P + t_{set}) = 64/(70 + 16) = 744$ MHz.



V_H=High Voltage Level.

V_L=Low Voltage Level.

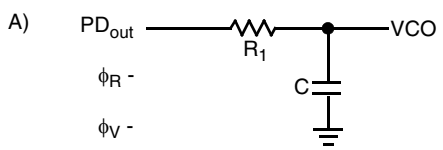
* At this point, when both f_R and f_V are in phase, the output is forced to near mid-supply.

NOTE: The PD_{out} generates error pulses during out-of-lock conditions. When locked in phase and frequency the output is high and the voltage at this pin is determined by the low-pass filter capacitor.

Figure 11. Phase Detector/Lock Detector Output Waveforms

4 Design Considerations

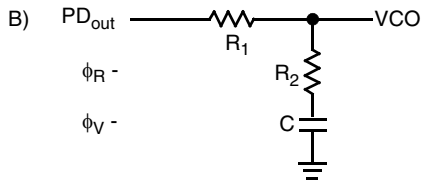
4.1 Phase-Locked Loop — Low-Pass Filter Design



$$\omega_n = \sqrt{\frac{K_\phi K_{VCO}}{NR_1C}}$$

$$\zeta = \frac{N\omega_n}{2K_\phi K_{VCO}}$$

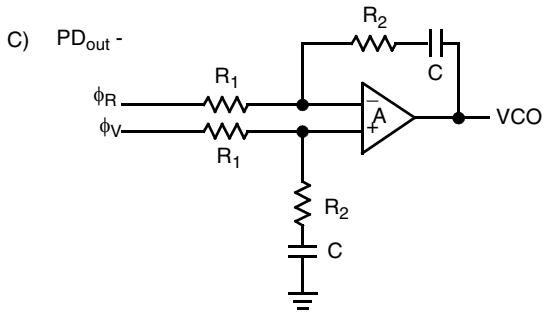
$$F(s) = \frac{1}{R_1sC + 1}$$



$$\omega_n = \sqrt{\frac{K_\phi K_{VCO}}{NC(R_1 + R_2)}}$$

$$\zeta = 0.5\,\omega_n\left(R_2C + \frac{N}{K_\phi K_{VCO}}\right)$$

$$F(s) = \frac{R_2sC+1}{(R_1+R_2)sC+1}$$



$$\omega_n = \sqrt{\frac{K_\phi K_{VCO}}{NCR_1}}$$

$$\zeta = \frac{\omega_n R_2 C}{2}$$

Assuming gain A is very large, then:

$$F(s) = \frac{R_2sC + 1}{R_1sC}$$

NOTE: Sometimes R_1 is split into two series resistors, each $R_1 \div 2$. A capacitor C_C is then placed from the midpoint to ground to further filter ϕ_V and ϕ_R. The value of C_C should be such that the corner frequency of this network does not significantly affect ω_n.
The ϕ_R and ϕ_V outputs swing rail-to-rail. Therefore, the user should be careful not to exceed the common mode input range of the op amp used in the combiner/loop filter.

Definitions:
N = Total Division Ratio in feedback loop
K_ϕ (Phase Detector Gain) = $V_{DD}/4\pi$ for PD_{out}
K_ϕ (Phase Detector Gain) = $V_{DD}/2\pi$ for ϕ_V and ϕ_R

K_{VCO} (VCO Gain) = $\frac{2\pi\Delta f_{VCO}}{\Delta V_{VCO}}$

for a typical design w_n (Natural Frequency) ≈ $\frac{2\pi fr}{10}$ (at phase detector input).

Damping Factor: $\zeta \cong 1$

Figure 12. Phase-Locked Loop — Low-Pass Filter Design

4.2 Crystal Oscillator Considerations

The following options may be considered to provide a reference frequency to Freescale's CMOS frequency synthesizers.

4.2.1 Use of a Hybrid Crystal Oscillator

Commercially available temperature-compensated crystal oscillators (TCXOs) or crystal-controlled data clock oscillators provide very stable reference frequencies. An oscillator capable of sinking and sourcing 50 μA at CMOS logic levels may be direct or dc coupled to OSC_{in}. In general, the highest frequency capability is obtained utilizing a direct-coupled square wave having a rail-to-rail (V_{DD} to V_{SS}) voltage swing. If the oscillator does not have CMOS logic levels on the outputs, capacitive or ac coupling to OSC_{in} may be used. OSC_{out}, an unbuffered output, should be left floating.

4.2.2 Design an Off-Chip Reference

The user may design an off-chip crystal oscillator using ICs specifically developed for crystal oscillator applications, or using discrete transistors. The reference signal from the oscillator is ac coupled to OSC_{in}. For large amplitude signals (standard CMOS logic levels), dc coupling is used. OSC_{out}, an unbuffered output, should be left floating. In general, the highest frequency capability is obtained with a direct-coupled square wave having rail-to-rail voltage swing.

4.2.3 Use of the On-Chip Oscillator Circuitry

The on-chip amplifier (a digital inverter) along with an appropriate crystal may be used to provide a reference source frequency. A fundamental mode crystal, parallel resonant at the desired operating frequency, should be connected as shown in Figure 13.

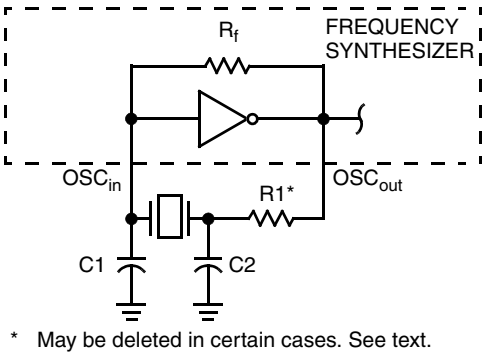


Figure 13. Pierce Crystal Oscillator Circuit

For V_{DD} = 5.0 V, the crystal should be specified for a loading capacitance, C_L, which does not exceed 32 pF for frequencies to approximately 8.0 MHz, 20 pF for frequencies in the area of 8.0 to 15 MHz, and 10 pF for higher frequencies. These are guidelines that provide a reasonable compromise between IC capacitance, drive capability, swamping variations in stray and IC input/output capacitance, and realistic C_L values. The shunt load capacitance, C_L, presented across the crystal can be estimated to be:

$$C_L = \frac{C_{in}C_{out}}{C_{in} + C_{out}} + C_a + C_o + \frac{C1 \cdot C2}{C1 + C2}$$

where

C_{in} = 5 pF (see Figure 14)
C_{out} = 6 pF (see Figure 14)
C_a = 1 pF (see Figure 14)
C_O = the crystal's holder capacitance (see Figure 15)

C1 and C2 = external capacitors (see Figure 13)

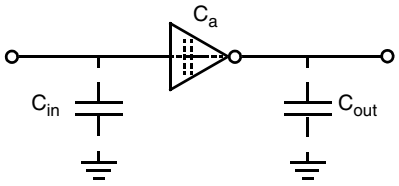
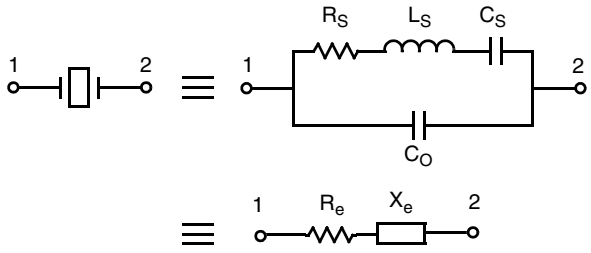


Figure 14. Parasitic Capacitances of the Amplifier



NOTE: Values are supplied by crystal manufacturer
(parallel resonant crystal).

Figure 15. Equivalent Crystal Networks

The oscillator can be “trimmed” on-frequency by making a portion or all of C1 variable. The crystal and associated components must be located as close as possible to the OSC_{in} and OSC_{out} pins to minimize distortion, stray capacitance, stray inductance, and startup stabilization time. In some cases, stray capacitance should be added to the value for C_{in} and C_{out}.

Power is dissipated in the effective series resistance of the crystal, R_e, in Figure 15. The drive level specified by the crystal manufacturer is the maximum stress that a crystal can withstand without damage or excessive shift in frequency. R1 in Figure 13 limits the drive level. The use of R1 may not be necessary in some cases (i.e., R1 = 0 Ω).

To verify that the maximum dc supply voltage does not overdrive the crystal, monitor the output frequency as a function of voltage at OSC_{out}. (Care should be taken to minimize loading.) The frequency should increase very slightly as the dc supply voltage is increased. An overdriven crystal will decrease in frequency or become unstable with an increase in supply voltage. The operating supply voltage must be reduced or R1 must be increased in value if the overdriven condition exists. The user should note that the oscillator start-up time is proportional to the value of R1.

Through the process of supplying crystals for use with CMOS inverters, many crystal manufacturers have developed expertise in CMOS oscillator design with crystals. Discussions with such manufacturers can prove very helpful.

4.3 Dual-Modulus Prescaling

4.3.1 Overview

The technique of dual-modulus prescaling is well established as a method of achieving high performance frequency synthesizer operation at high frequencies. Basically, the approach allows relatively low-frequency programmable counters to be used as high-frequency programmable counters with speed capability of several hundred MHz. This is possible without the sacrifice in system resolution and performance that results if a fixed (single-modulus) divider is used for the prescaler.

In dual-modulus prescaling, the lower speed counters must be uniquely configured. Special control logic is necessary to select the divide value P or P + 1 in the prescaler for the required amount of time (see modulus control definition).

4.3.2 Design Guidelines

The system total divide value, N_{total} (N_T) will be dictated by the application:

$$N_T = \frac{\text{frequency into the prescaler}}{\text{frequency into the phase detector}} = N \bullet P + A$$

N is the number programmed into the ÷ N counter, A is the number programmed into the ÷ A counter, P and P + 1 are the two selectable divide ratios available in the dual-modulus prescalers. To have a range of N_T values in sequence, the ÷ A counter is programmed from zero through P - 1 for a particular value N in the ÷ N counter. N is then incremented to N + 1 and the ÷ A is sequenced from 0 through P - 1 again.

There are minimum and maximum values that can be achieved for N_T. These values are a function of P and the size of the ÷ N and ÷ A counters.

The constraint $N \geq A$ always applies. If $A_{max} = P - 1$, then $N_{min} \geq P - 1$. Then $N_{Tmin} = (P - 1) P + A$ or $(P - 1) P$ since A is free to assume the value of 0.

$$N_{Tmax} = N_{max} \bullet P + A_{max}$$

To maximize system frequency capability, the dual-modulus prescaler output must go from low to high after each group of P or P + 1 input cycles. The prescaler should divide by P when its modulus control line is high and by P + 1 when its MC is low.

For the maximum frequency into the prescaler (f_{VCOmax}), the value used for P must be large enough such that:

1. f_{VCOmax} divided by P may not exceed the frequency capability of f_{in} (input to the ÷ N and ÷ A counters).
2. The period of f_{VCO} divided by P must be greater than the sum of the times:
   a) Propagation delay through the dual-modulus prescaler.
   b) Prescaler setup or release time relative to its MC signal.
   c) Propagation time from f_{in} to the MC output for the frequency synthesizer device.

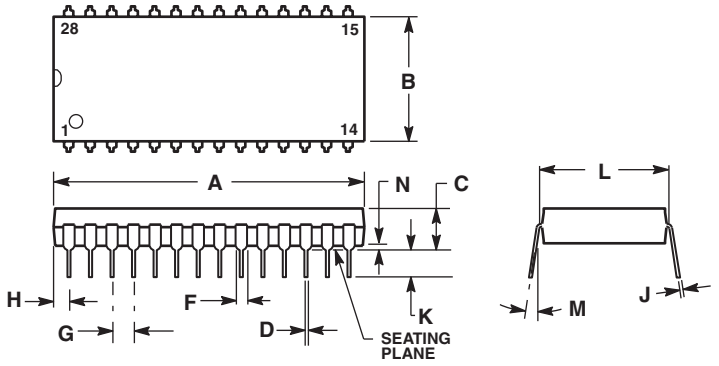
A sometimes useful simplification in the programming code can be achieved by choosing the values for P of 8, 16, 32, or 64. For these cases, the desired value of N_T results when N_T in binary is used as the program code to the ÷ N and ÷ A counters treated in the following manner:

1. Assume the ÷ A counter contains "a" bits where $2^a \geq P$.
2. Always program all higher order ÷ A counter bits above "a" to 0.
3. Assume the ÷ N counter and the ÷ A counter (with all the higher order bits above "a" ignored) combined into a single binary counter of n + a bits in length (n = number of divider stages in the ÷ N counter). The MSB of this "hypothetical" counter is to correspond to the MSB of ÷ N and the LSB is to correspond to the LSB of ÷ A. The system divide value, N_T, now results when the value of N_T in binary is used to program the "new" n + a bit counter.

By using the two devices, several dual-modulus values are achievable.

5 Package Dimensions

P SUFFIX
PLASTIC DIP

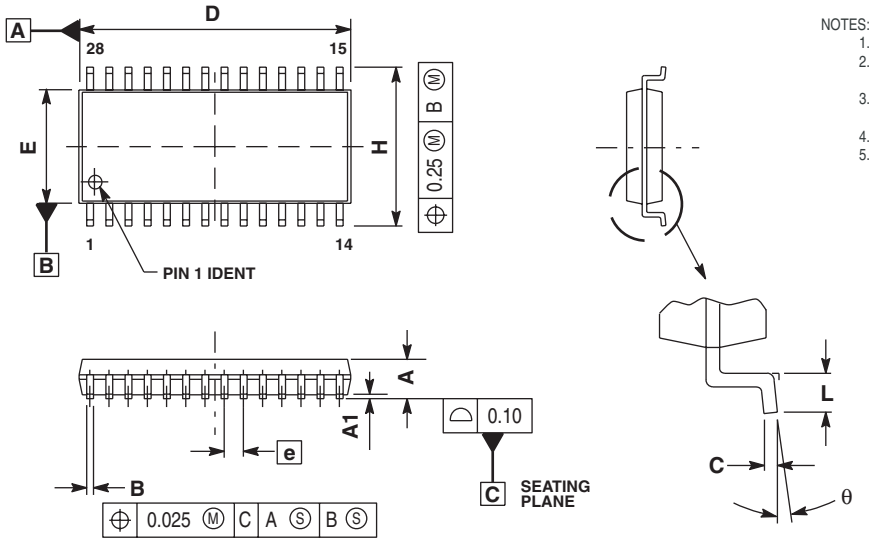


NOTES:
1. POSITIONAL TOLERANCE OF LEADS (D), SHALL BE WITHIN 0.25 (0.010) AT MAXIMUM MATERIAL CONDITION, IN RELATION TO SEATING PLANE AND EACH OTHER.
2. DIMENSION L TO CENTER OF LEADS WHEN FORMED PARALLEL.
3. DIMENSION B DOES NOT INCLUDE MOLD FLASH.
4. CONTROLLING DIMENSION: INCH.

	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	1.435	1.465	36.45	37.21
B	0.540	0.560	13.72	14.22
C	0.155	0.200	3.94	5.08
D	0.014	0.022	0.36	0.56
F	0.040	0.060	1.02	1.52
G	0.100 BSC		2.54 BSC	
H	0.065	0.085	1.65	2.16
J	0.008	0.015	0.20	0.38
K	0.115	0.135	2.92	3.43
L	0.600 BSC		15.24 BSC	
M	0°	15°	0°	15°
N	0.020	0.040	0.51	1.02

Figure 16. Outline Dimensions for Plastic DIP
(Case Outline 710-02, Issue B)

DW SUFFIX
SOG PACKAGE



NOTES:
1. DIMENSIONS ARE IN MILLIMETERS.
2. INTERPRET DIMENSIONS AND TOLERANCES PER ASME Y14.5M, 1994.
3. DIMENSIONS D AND E DO NOT INCLUDE MOLD PROTRUSIONS.
4. MAXIMUM MOLD PROTRUSION 0.015 PER SIDE.
5. DIMENSION B DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.13 TOTAL IN EXCESS OF B DIMENSION AT MAXIMUM MATERIAL CONDITION.

	MILLIMETERS	
DIM	MIN	MAX
A	2.35	2.65
A1	0.13	0.29
B	0.35	0.49
C	0.23	0.32
D	17.80	18.05
E	7.40	7.60
e	1.27 BSC	
H	10.05	10.55
L	0.41	0.90
θ	0°	8°

Figure 17. Outline Dimensions for SOG Package
(Case Outline 751F-05, Issue F)

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