

Vishay General Semiconductor

ELECTRICAL CHARACTERISTICS (T _A = 25 °C unless otherwise noted)								
PARAMETER	TEST CONDITIONS		SYMBOL	TYP.	MAX.	UNIT		
Instantaneous forward voltage	I _F = 2 A	T _A = 25 °C	V _F ⁽¹⁾	0.86	0.90	V		
		T _A = 100 °C		0.76	0.83			
Reverse current	Rated V _R	T _A = 25 °C	I _R ⁽²⁾	-	10	μA		
		T _A = 100 °C		180	350			
Reverse recovery time	I _F = 0.5 A, I _R = 1.0 A, I _{rr} = 0.25 A	T _A = 25 °C	t _{rr}	-	20	ns		
	$I_{F} = 2.0 \text{ A, } dI/dt = 50 \text{ A/}\mu\text{s}, \\ V_{R} = 30 \text{ V, } I_{rr} = 0.1 I_{RM}$	T _A = 25 °C		27	-			
		T _A = 100 °C		35	-			
Storage charge	$I_{F}=2.0~\text{A},~\text{dI/dt}=50~\text{A/}\mu\text{s},\\ V_{R}=30~\text{V},~\text{I}_{rr}=0.1~\text{I}_{RM}$	T _A = 25 °C	Q _{rr}	9	-	nC		
		T _A = 100 °C		19	-			
Typical junction capacitance	4.0 V, 1 MHz		CJ	16	-	pF		

Notes

⁽¹⁾ Pulse test: 300 µs pulse width, 1 % duty cycle

⁽²⁾ Pulse test: Pulse width \leq 40 ms

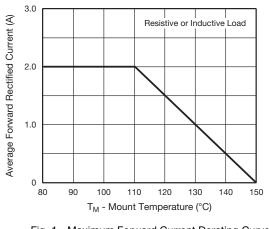
THERMAL CHARACTERISTICS ($T_A = 25 \text{ °C}$ unless otherwise noted)							
PARAMETER	SYMBOL	U2B	U2C	U2D	UNIT		
Typical thermal resistance	R _{0JA} ⁽¹⁾	105			°C/W		
	R _{0JM} ⁽¹⁾	18					

Note

⁽¹⁾ Free air, mounted on recommended copper pad area. Thermal resistance $R_{\theta JA}$ - junction to ambient, $R_{\theta JM}$ - junction to mount

ORDERING INFORMATION (Example)							
PREFERRED P/N	UNIT WEIGHT (g)	PREFERRED PACKAGE CODE	BASE QUANTITY	DELIVERY MODE			
U2D-E3/52T	0.099	52T	750	7" diameter plastic tape and reel			
U2D-E3/5BT	0.099	5BT	3200	13" diameter plastic tape and reel			
U2D-M3/52T	0.099	52T	750	7" diameter plastic tape and reel			
U2D-M3/5BT	0.099	5BT	3200	13" diameter plastic tape and reel			

RATINGS AND CHARACTERISTICS CURVES (T_A = 25 °C unless otherwise noted)



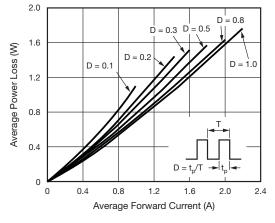
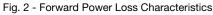


Fig. 1 - Maximum Forward Current Derating Curve



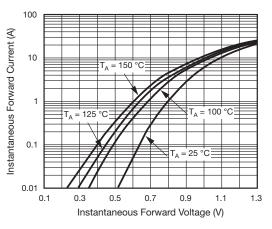
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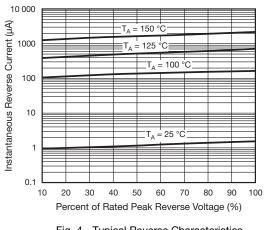
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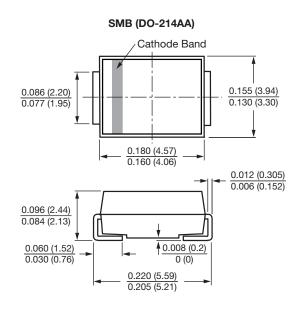
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Fig. 3 - Typical Instantaneous Forward Characteristics









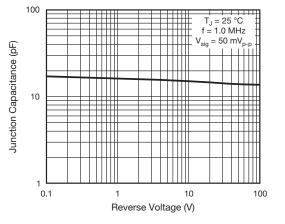


Fig. 5 - Typical Junction Capacitance

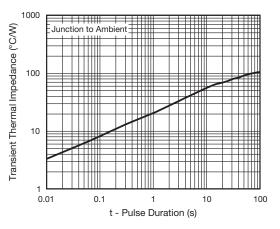
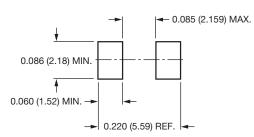


Fig. 6 - Typical Transient Thermal Impedance

Mounting Pad Layout



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