e5500 CORE

The T1 family is based on the 64-bit e5500 Power Architecture core, which uses a seven-stage pipeline for low latency response to unpredictable code execution paths, boosting single-threaded performance.

e5500 Core Features

- Supports up to 1.5 GHz core frequencies
- Tightly coupled low latency cache hierarchy
- 32 KB I/D (L1), 256 KB L2 per core
- Up to 256 KB of shared platform cache (L3)
- 3.0 DMIPS/MHz per core
- Up to 64 GB of addressable memory space
- Hybrid 32-bit mode to support legacy software and seamless transition to 64-bit architecture

VIRTUALIZATION

The T1 family includes support for hardware-assisted virtualization. The e5500 core offers an extra core privilege level (hypervisor). Virtualization software for the T1 family includes kernel-based virtual machine (KVM), Linux® OS containers, NXP hypervisor and commercial virtualization software from Green Hills® Software and Enea®.

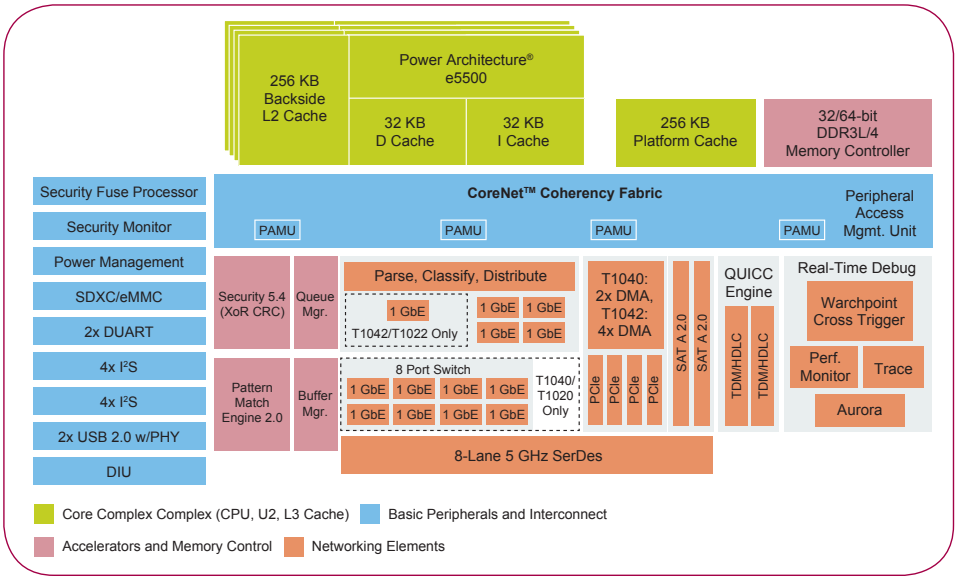
DATA PATH ACCELERATION ARCHITECTURE (DPAA)

The T1 family integrates the QorIQ DPAA, an innovative multicore infrastructure for scheduling work to cores (physical and virtual), hardware accelerators and network interfaces.

DPAA HARDWARE ACCELERATORS

Frame manager (FMAN)	13 Gb/s classify, parse and distribute
Buffer manager (BMAN)	64 buffer pools
Queue manager (QMAN)	Up to 2^{24} queues
Security (SEC)	5 Gb/s: 3DES, AES

QorIQ T1040 AND T1042 COMMUNICATIONS PROCESSORS



T1 FAMILY FEATURE LIST

Two or four e5500 single-threaded cores built on Power Architecture® technology	• Up to 1.5 GHz with 64-bit ISA support • Three levels of instructions: User, supervisor, hypervisor • Hybrid 32-bit mode to support legacy software and transition to a 64-bit architecture
CoreNet platform cache	• 256 KB shared platform cache
Hierarchical interconnect fabric	• CoreNet fabric supporting coherent and non-coherent transactions with prioritization and bandwidth allocation amongst CoreNet endpoints • QMAN fabric supporting packet-level queue management and quality of service
64-bit DDR3L/4 SDRAM memory controller with ECC support	• Up to 1600 MT/s
DPAA incorporating acceleration for the following functions	• Packet parsing, classification and distribution • Queue management for scheduling, packet sequencing and congestion management • Hardware buffer management for buffer allocation and de-allocation • Cryptography acceleration (SEC 5.x)
SerDes	• Eight lanes at up to 5 Gb/s • Supports SGMII, QSGMII, PCI Express® and SATA
Ethernet interfaces	• 8-port Gigabit Ethernet switch (available with T1040 and T1020 only) • Up to 5x 1 Gb/s Ethernet MACs
QUICC Engine module	• Support for legacy protocols TDM, HDLC, UART and ISDN
High-speed peripheral interfaces	• Four PCI Express 2.0 controllers
Additional peripheral interfaces	• Two serial ATA (SATA 2.0) controllers • Two High-Speed USB 2.0 controllers with integrated PHYs • Enhanced secure digital host controller (SD/MMC/eMMC) • Enhanced serial peripheral interface • Two I²C controllers • Four UARTS • Integrated flash controller supporting NAND and NOR flash memory
DMA	• Dual four channel
Support for hardware virtualization and partitioning enforcement	• Extra privileged level for hypervisor support
QorIQ trust architecture	• Secure boot, secure debug, tamper detection, volatile key storage

T1 FAMILY COMPARISON

	T1020	T1022	T1040	T1042	T2081
CPU	2 e5500	2 e5500	4 e5500	4 e5500	4 e6500 (dual threaded)
	1200–1500 MHz	1200–1500 MHz	1200-1500 MHz	1200-1500 MHz	1200–1800 MHz
DDR Interface	1x DDR3L/4 to 1600 MT/s	1x DDR3L/4 to 1600 MT/s	1x DDR3L/4 to 1600 MT/s	1x DDR3L/4 to 1600 MT/s	1x DDR3/3L to 2133 MT/s
10/100/1000 Ethernet (with IEEE® 1588v2)	8-port GbE switch + 4x 1 GbE	5x 1 GbE	I8-port GbE switch + 4x 1 GbE	5x 1 GbE	2x 1/10 GbE + 6x 1 GbE
SerDes	Eight lanes (5 GHz)	Eight lanes (5 GHz)	Eight lanes (5 GHz)	Eight lanes (5 GHz)	Eight lanes (10 GHz)
Package	Pin compatible				

The FMAN, a primary element of the DPAA, parses headers from incoming packets, then classifies and selects data buffers with optional policing and congestion management. The FMAN passes its work to the QMAN which assigns it to cores or accelerators with a multilevel scheduling hierarchy.

GIGABIT ETHERNET SWITCH

The T1040 and T1020 processors include an integrated gigabit Ethernet switch that supports wire-speed switching for all packet sizes. Other features include VLAN, QoS processing and ACLs.

SYSTEM PERIPHERALS AND NETWORKING

For networking, the FMAN supports up to five 1 Gb/s MAC controllers that connect to PHYs, switches and backplanes over RGMII and SGMII. The T1040 and T1020 processors also include an integrated 8-port Gigabit Ethernet switch, which supports QSGMII or SGMII interfaces. High-speed system expansion is supported through three PCI Express® V2.0 controllers that support a variety of lane widths. Other peripherals include SATA, SD/MMC, I²C, UART, SPI, NOR/NAND controller, GPIO and a 1600 MT/s DDR3L/4 controller.

SOFTWARE AND TOOL SUPPORT

NXP and our partner network deliver a wide range of tools, run-time software, reference solutions and services to accelerate your designs.

- QorIQ reference design boards
- CodeWarrior Development Studio for Power Architecture
- NXP Linux SDK
- Reference Platforms
  - Enterprise WLAN Access Point
  - VortiQa Application Software
  - AIS–Application Identification Software
  - Enterprise Software for Networking
  - ONS–Open Network Switch Software
  - OND–Open Network Director Software
- Professional Services & Support
  - Commercial Services
  - Linux SDK Support Package
  - Reference Design Software (RDS) Support Package
- Third Party Software and Tools
  - Enea, Green Hills, Mentor Graphics and Wind River

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